PRELIMINARY

DESCRIPTION

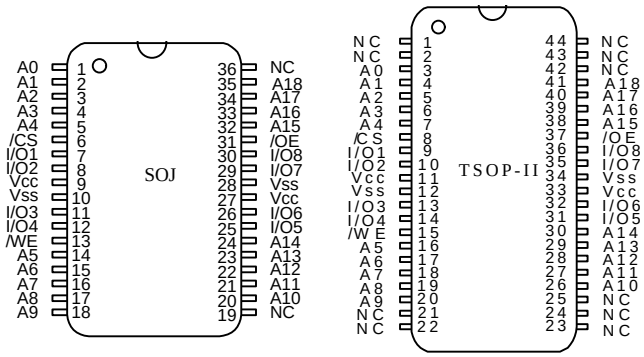
The HY63V8400 is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8-bits. The HY63V8400 uses eight common input and output lines and has an output enable pin which operates faster than. address access time at read cycle. The device is fabricated using Hyundai's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications

FEATURES

- Single 3.3V±0.3V Power Supply
- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Low data Retention Voltage:
  - 2.0V(min) –L-ver. Only
- Center Power/Ground Pin Configuration
- Standard pin configuration
  - 36pin 400mil SOJ
  - 44pin 400mil TSOP-II

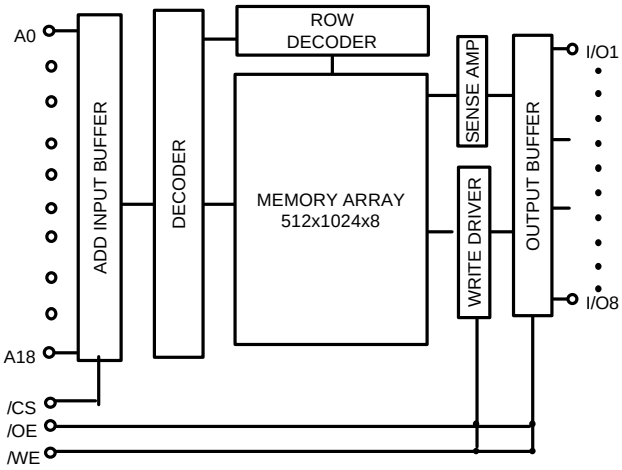
Product No.	Supply Voltage(V)	Speed (ns)	Operation Current(mA)	Standby Current(mA)	
					L
HY63V8400	3.3	10	200	10	1
HY63V8400	3.3	12	190	10	1
HY63V8400	3.3	15	180	10	1

PIN CONNECTION



SOJ TSOP-II

BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS	Chip Select	A0~A18	Address Input
/WE	Write Enable	Vcc	Power(+3.3V)
/OE	Output Enable	Vss	Ground
I/O1~I/O8	Data Input/Output	NC	No Connection

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter		Rating	Unit
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to Vss		-0.5 to 4.6	V
Vcc	Voltage on Vcc Supply Relative to Vss		-0.5 to 5.5	V
T_A	Operating Temperature	Commercial	0 to 70	°C
		Industrial	-40 to 85	°C
T_{STG}	Storage Temperature		-65 to 150	°C
P_D	Power Dissipation		1.0	W

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0°C to 70°C)

Symbol	Parameter	Min.	Type	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	-	Vcc+0.3(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	-	0.8	V

Note
1. $V_{IL\ (min)}$= -2.0V a.c(pulse width less than 8ns) for I ≤ 20mA
2. V_{IH}(max) = Vcc + 2.0V a.c(pulse width less than 8ns) for I ≤ 20mA

DC ELECTRICAL CHARACTERISTICS

(Vcc = 3.3V±0.3V, T_A = 0°C to 70°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		-2	-	2	uA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		-2	-	2	uA
I_{CC}	Operating Current	/CS = V_{IL}, V_{IN} = V_{IH}, $I_{I/O}$ = 0mA, Min. Duty Cycle = 100%	10ns	-	-	200	mA
			12ns	-	-	190	mA
			15ns	-	-	180	mA
I_{SB}	TTL Standby Current (TTL Inputs)	/CS = V_{IH}, V_{IN}=V_{IH} or V_{IL} Min. Cycle		-	-	60	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	/CS ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V		-	-	10	mA
			L	-		1	mA
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0mA		2.4	-	-	V

Note : Typical values are at Vcc = 3.3V, T_A = 25°C

AC CHARACTERISTICS

(Vcc = 3.3V ± 0.3V, T_A = 0°C to 70°C, unless otherwise specified.)

#	Symbol	Parameter	10ns		12ns		15ns		Unit
			Min	Max	Min	Max	Min	Max	
READ CYCLE									
1	tRC	Read Cycle Time	10	-	12	-	15	-	ns
2	tAA	Address Access Time	-	10	-	12	-	15	ns
3	tACS	Chip Select Access Time	-	10	-	12	-	15	ns
4	tOE	Output Enable to Output Valid	-	5	-	6	-	7	ns
5	tCLZ	Chip Select to Output in Low Z	3	-	3	-	3	-	ns
6	tOLZ	Output Enable to Output in Low Z	0	-	0	-	0	-	ns
7	tCHZ	Chip Deselecting to Output in High Z	0	5	0	6	0	7	ns
8	tOHZ	Out Disable to Output in High Z	0	5	0	6	0	7	ns
9	tOH	Output Hold from Address Change	3	-	3	-	3	-	ns
WRITE CYCLE									
10	tWC	Write Cycle Time	10	-	12	-	15	-	ns
11	tCW	Chip Select to End of Write	7	-	8	-	10	-	ns
12	tAW	Address Valid to End of Write	7	-	8	-	10	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width(/OE High)	7	-	8	-	10	-	ns
15	tWP1	Write Pulse Width(/OE Low)	10	-	12	-	15	-	ns
16	tWR	Write Recovery Time	0	-	0	-	0	-	ns
17	tWHZ	Write to Output in High Z	0	5	0	6	0	7	ns
18	tDW	Data to Write Time Overlap	5	-	6	-	7	-	ns
19	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
20	tOW	Output Active from End of Write	3	-	3	-	3	-	ns

NOTE : Above parameters are also guaranteed at industrial temperature range.

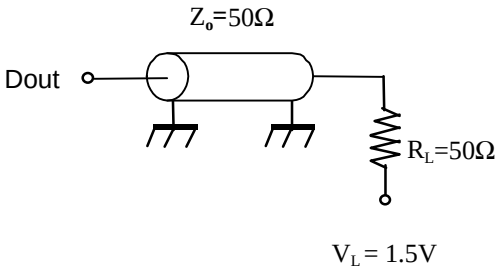
AC TEST CONDITIONS

(Vcc = 3.3V±0.3V, T_A = 0°C to 70°C, unless otherwise specified.)

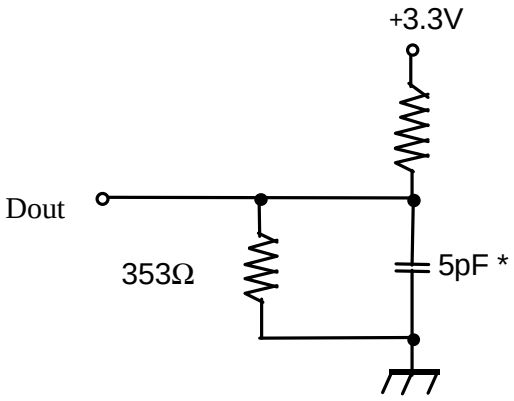
Parameter	Value
Input Pulse Level	0V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Level	1.5V
Output Load	See below

AC TEST CONDITIONS

Output Load (A)



Output Load (B)
(for tCHZ, tCLZ, tOHZ, tOLZ, tWHZ & tOW)



Note : *Including jig and scope capacitance

CAPACITANCE

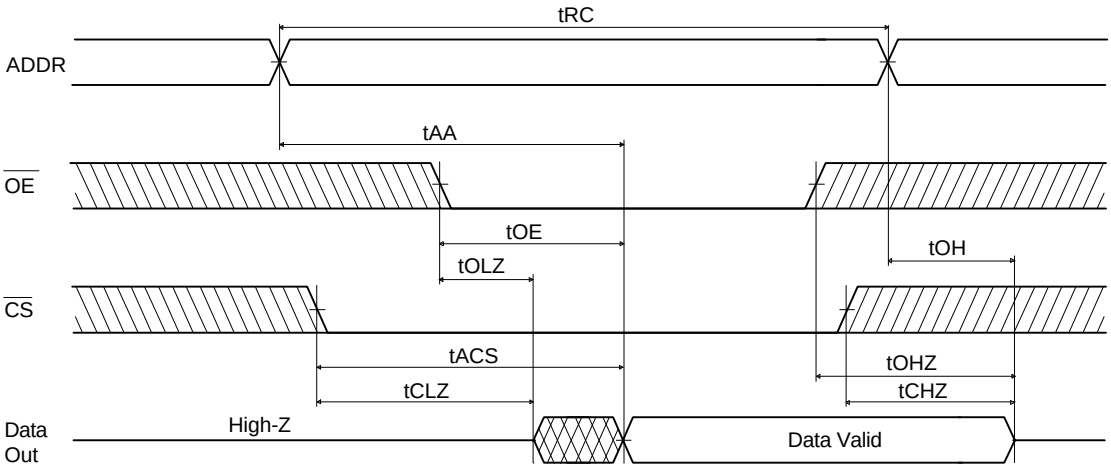
Temp = 25°C, f= 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : This parameter is sampled and not 100% tested

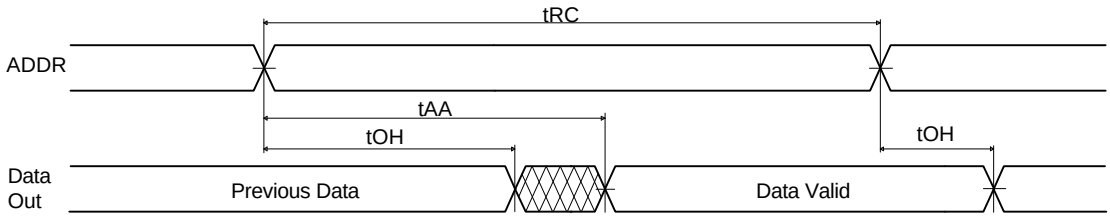
TIMING DIAGRAM

READ CYCLE 1



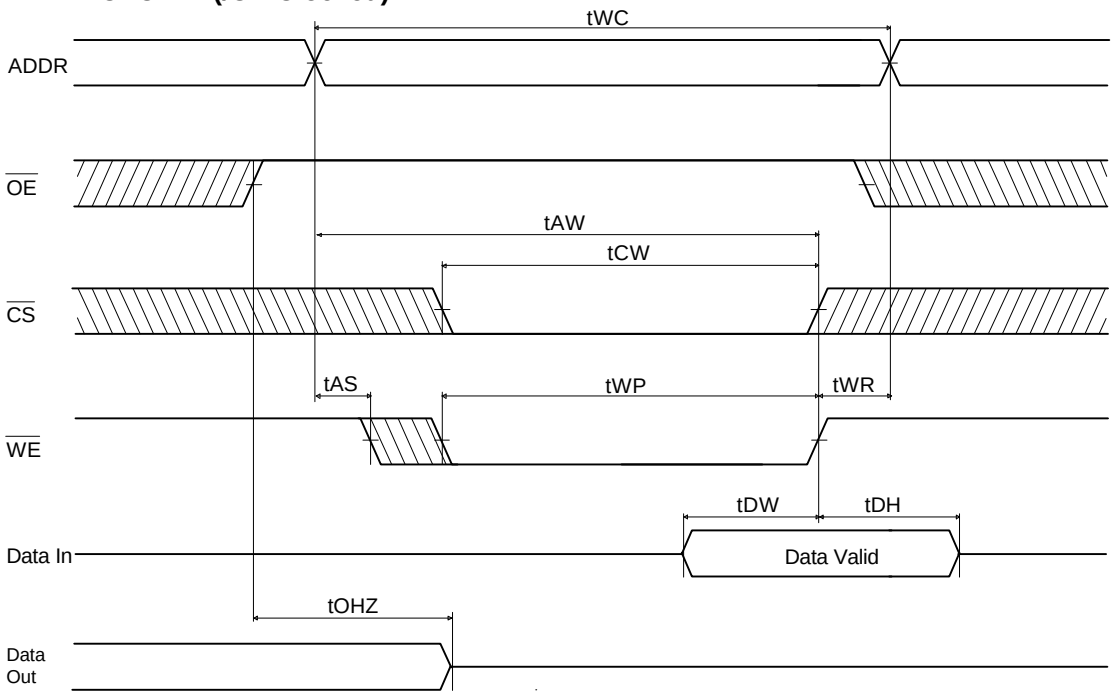
Note (Read Cycle)
1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for read cycle.

READ CYCLE 2

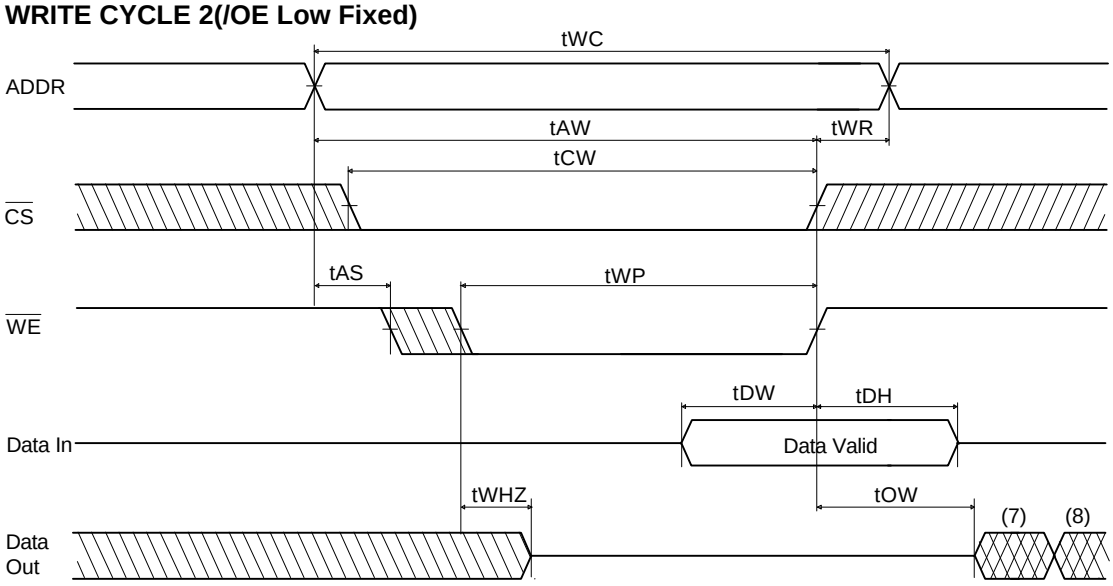


Note (Read Cycle)
1. /WE is high for read cycle.
2. Device is continuously selected /CS=V_{IL}.
3. /OE=V_{IL}.

WRITE CYCLE 1(/OE Clocked)



WRITE CYCLE 2(/OE Low Fixed)



Notes(Write Cycle)

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low, and /WE going low : A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS or /WE going high.
5. If /OE and /WE are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of latest written data in the write cycle.
8. DOUT is the read data of the new address.

FUNCTIONAL DESCRIPTION

/CS	/WE	/OE	/LB	/UB	MODE	I/O Pin		Supply Current
						I/O1 - I/O8	I/O9 - I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	Isb,Isb1
L	H	H	X	X	Output Disable	High-Z	High-Z	Icc
L	X	X	H	H				
L	H	L	L	H	Read	Dout	High-Z	Icc
			H	L		High-Z	Dout	
			L	L		Dout	Dout	
L	L	X	L	H	Write	Din	High-Z	Icc
			H	L		High-Z	Din	
			L	L		Din	Din	

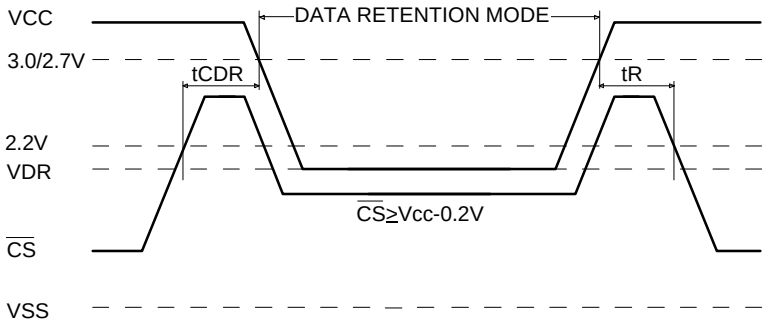
***** NOTE : X means Don,t Care

DATA RETENTION ELECTRIC CHARATERISTIC

(T_A = 0¡ Ëto 70¡ ÉE

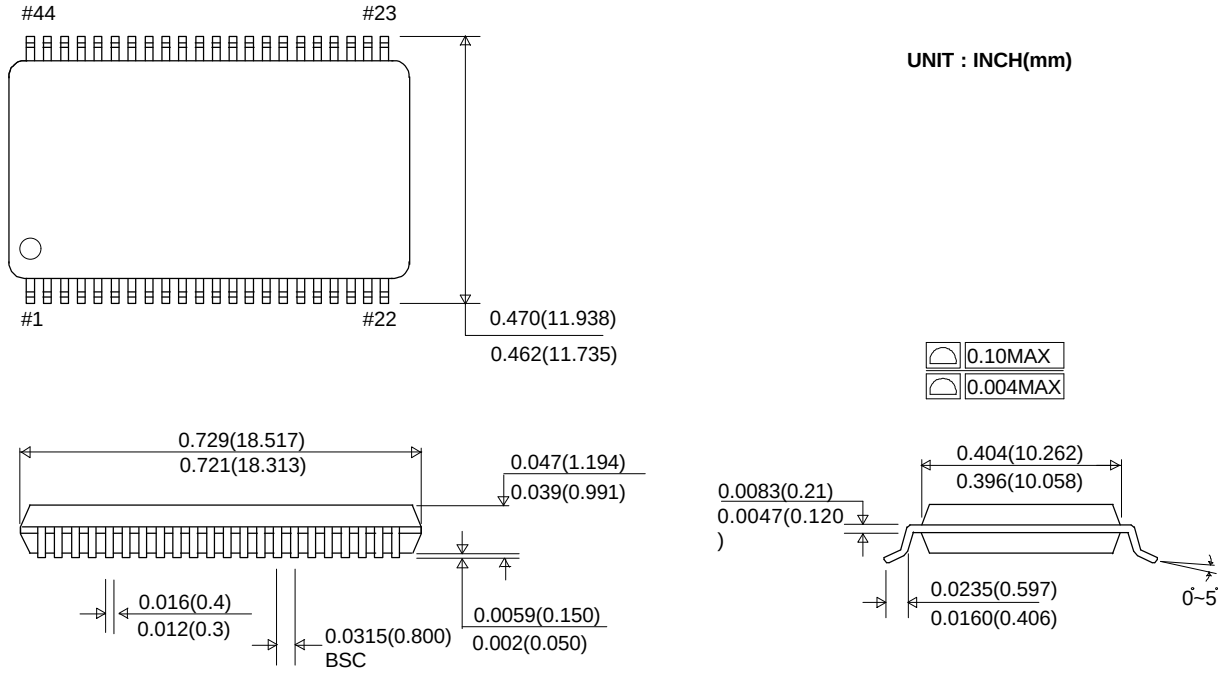
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention	/CS ≥ Vcc - 0.2V	2.0	-	3.6	V
I_{DR}	Data Retention Current	Vcc = 3.0V, /CS ≥ Vcc - 0.2V Vin ≥ Vcc - 0.2V or ≤ 2.0V	-	-	0.9	mA
		Vcc = 2.0V, /CS ≥ Vcc - 0.2V Vin ≥ Vcc - 0.2V or ≤ 2.0V	-	-	0.7	
tCDR	Data Retention Set-Up Time		0	-	-	ns
tR	Recovery Time		5	-	-	ms

DATA RETENTION TIMING DIAGRAM



PACKAGE INFORMATION

44pin 400mil Thin Small Outline Package (T2)



36pin 400mil Small Outline J-Form Package (J)