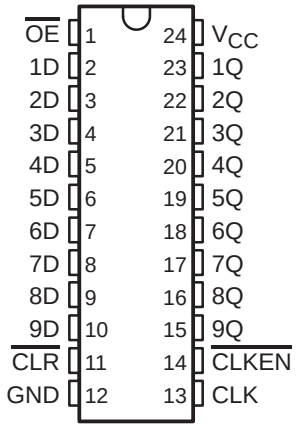
- **Functionally Equivalent to AMD's AM29823**
- **Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Outputs Have Undershoot-Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs Reduce dc Loading Effects**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54ALS29823 . . . JT PACKAGE
SN74ALS29823 . . . DW OR NT PACKAGE
(TOP VIEW)



description

These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing, and working registers.

With the clock-enable ($\overline{CLKEN}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock (CLK) input. Taking $\overline{CLKEN}$ high disables the clock buffer, latching the outputs. The ′ALS29823 have noninverting data (D) inputs. Taking the clear ($\overline{CLR}$) input low causes the nine Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input places the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs also are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

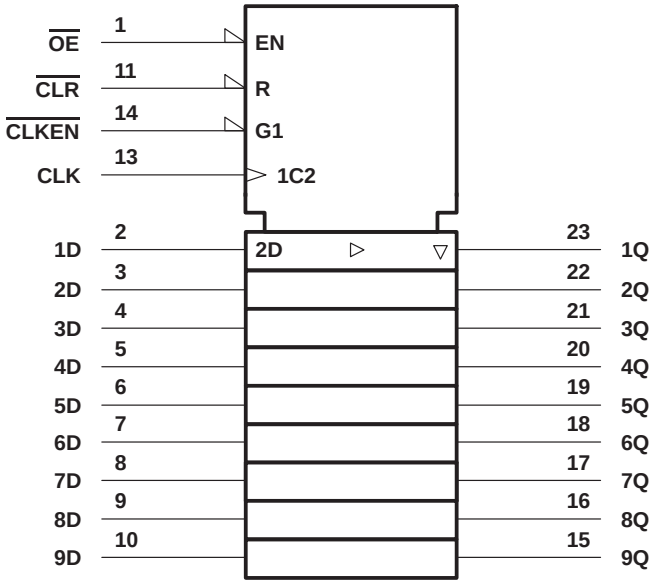
$\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS29823 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS29823 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

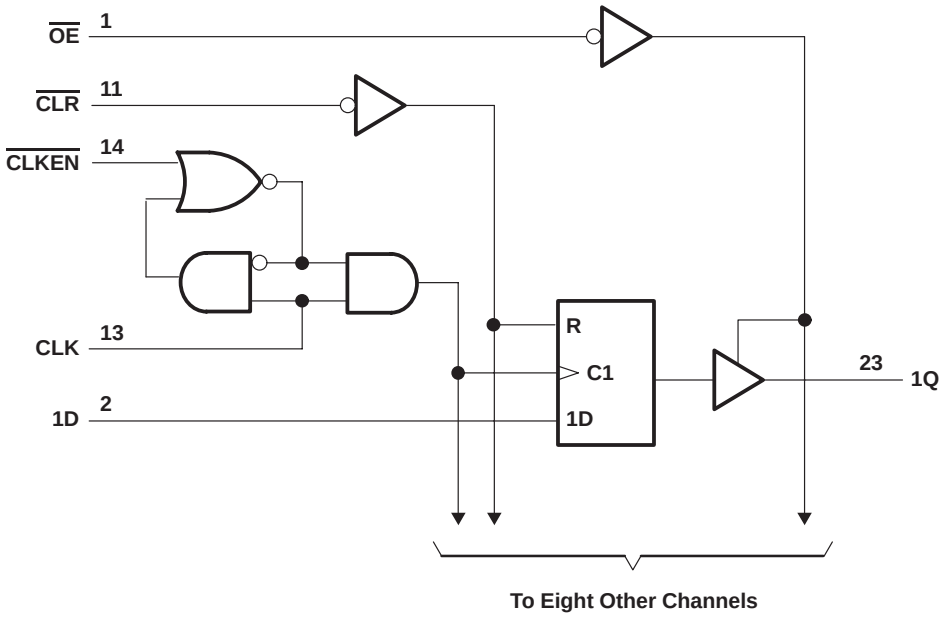
INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Voltage applied to a disabled high-impedance output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS29823 . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS29823			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–18	mA
I_{OL}	Low-level output current				32	mA
t_w	Pulse duration	$\overline{CLR}$ low	7			ns
		CLK high or low	8			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	7			ns
		Data	4			
		$\overline{CLKEN}$ high or low	8			
t_h	Hold time after CLK↑	$\overline{CLKEN}$	2			ns
		Data	4			
T_A	Operating free-air temperature		–55	25	125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS29823			UNIT
			MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –12 mA	2.4	3.3		V
		I_{OH} = –18 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.4 V			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–50	µA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	–75		–250	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high			90	mA
		Outputs low			105	
		Outputs open			115	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = MIN to MAX†, T_A = MIN to MAX†		UNIT
				SN54ALS29823		
				MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 50 pF	2	11.5	ns
t_{PHL}				2	11.5	
t_{PLH}	CLK	Any Q	C_L = 300 pF	2	21	ns
t_{PHL}				2	21	
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF	1	17.5	ns
t_{PZH}	$\overline{OE}$	Any Q	C_L = 50 pF	1	17	ns
t_{PZL}				1	17	
t_{PZH}	$\overline{OE}$	Any Q	C_L = 300 pF	1	25	ns
t_{PZL}				1	29.5	
t_{PHZ}	$\overline{OE}$	Any Q	C_L = 50 pF	1	16	ns
t_{PLZ}				1	14	
t_{PHZ}	$\overline{OE}$	Any Q	C_L = 5 pF	1	12	ns
t_{PLZ}				1	11	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN74ALS29823 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74ALS29823			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			ns
		CLK high or low	5			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	5			ns
		Data	2			
		$\overline{CLKEN}$ high or low	6			
t_h	Hold time after CLK↑	$\overline{CLKEN}$	0			ns
		Data	2			
T_A	Operating free-air temperature		0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS29823			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.75 V	I_{OH} = –15 mA	2.4	3.3		V
		I_{OH} = –24 mA	2	3.1		
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.4 V			20	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V			–20	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			–0.2	mA
I_{OS}‡	V_{CC} = 5.25 V,	V_O = 0	–75		–250	mA
I_{CC}	V_{CC} = 5.25 V,	Outputs open		80	115	mA

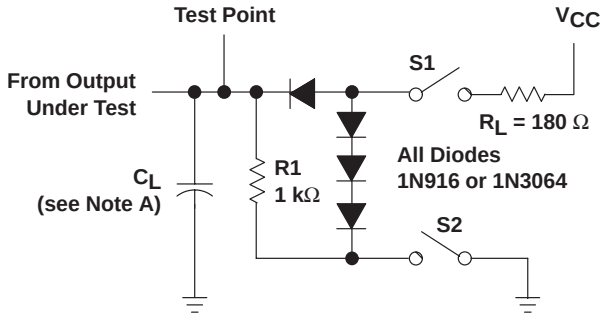
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = MIN to MAX§, T_A = MIN to MAX§		UNIT
				SN74ALS29823		
				MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 50 pF	2	10	ns
t_{PHL}				2	10	
t_{PLH}	CLK	Any Q	C_L = 300 pF		16	ns
t_{PHL}					16	
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF		12	ns
t_{PZH}	$\overline{OE}$	Any Q	C_L = 50 pF		14	ns
t_{PZL}					14	
t_{PZH}	$\overline{OE}$	Any Q	C_L = 300 pF		20	ns
t_{PZL}					23	
t_{PHZ}	$\overline{OE}$	Any Q	C_L = 50 pF		14	ns
t_{PLZ}					12	
t_{PHZ}	$\overline{OE}$	Any Q	C_L = 5 pF		9	ns
t_{PLZ}					9	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

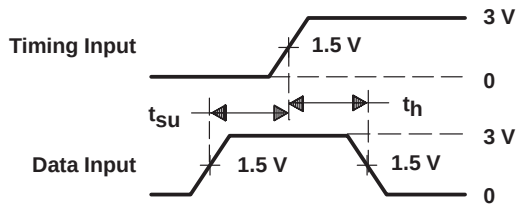
PARAMETER MEASUREMENT INFORMATION



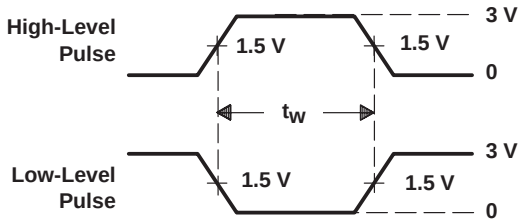
LOAD CIRCUIT

SWITCH POSITION TABLE

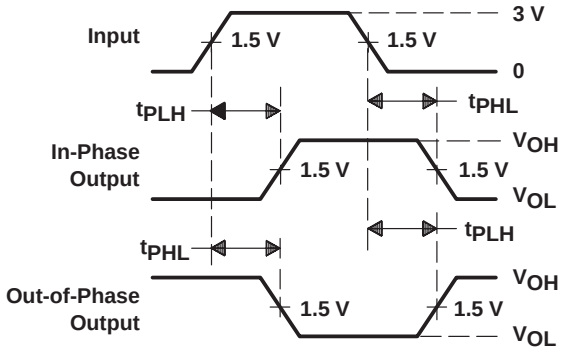
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



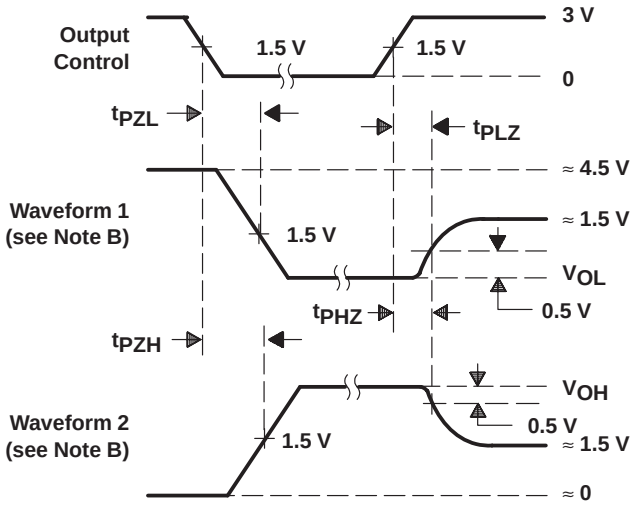
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY/PKG | APPLICATION NOTES | USER GUIDES | MORE LITERATURE

PRODUCT SUPPORT: TRAINING

SN54ALS29823, 9-Bit Bus-Interface Flip-Flops With 3-State Outputs
DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ALS29823
Voltage Nodes (V)	5
Vcc range (V)	4.75 to 5.25
Input Level	TTL
Output Level	TTL
No. of Outputs	9
Logic	True

FEATURES

Back to Top

- Functionally Equivalent to AMD's AM29823
- Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

DESCRIPTION

Back to Top

These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing, and working registers.

With the clock-enable ($\overline{\text{CLKEN}}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock (CLK) input. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, latching the outputs. The ´ALS29823 have noninverting data (D) inputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the nine Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{\text{OE}}$) input places the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs also are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{\text{OE}}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS29823 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS29823 is characterized for operation from 0°C to 70°C.

TECHNICAL DOCUMENTS

Back to Top

To view the following documents, Acrobat Reader 4.0 is required.

Product Folder: SN54ALS29823, 9-Bit Bus-Interface Flip-Flops With 3-State Outputs

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: sn54als29823.pdf (110 KB,Rev.B) (Updated: 01/01/1995)

APPLICATION NOTES

Back to Top

View Application Notes for Digital Logic

- Advanced Schottky (ALS and AS) Logic Families (SDAA010 - Updated: 08/01/1995)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

Back to Top

- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

Back to Top

- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/AVAILABILITY/PKG

Back to Top

DEVICE INFORMATION
Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
5962-9067501MLA	ACTIVE	CDIP (JT) | 24	-55 TO 125		View Contents	1KU | 11.94	1
SNJ54ALS29823JT	ACTIVE	CDIP (JT) | 24	-55 TO 125	5962-9067501MLA	View Contents	1KU | 11.94	1

TI INVENTORY STATUS
As Of 09:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME
0*	>10k | 20 May	8 WKS
674*	>10k | 20 May	8 WKS

REPORTED DISTRIBUTOR INVENTORY
As Of 09:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
None Reported View Distributors		
None Reported View Distributors		

Table Data Updated on: 4/17/2003