NX2415

TWO PHASE SYNCHRONOUS PWM CONTROLLER WITH INTEGRATED FET DRIVER AND DIFFERENTIAL CURRENT SENSE

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX2415 is a two-phase PWM controller with integrated FET driver designed for low voltage high current application. The two phase synchronous buck converter offers ripple cancelation for both input and output. The NX2415 uses differential remote sensing using either current sense resistor or inductor DCR sensing to achieve accurate current matching between the two channels. Differential sensing eliminates the error caused by PCB board trace resistance that is otherwise is present when using a single ended voltage sensing. In addition the NX2415 offers high drive current capability especially for keeping the synchronous MOSFET off during SW node transition, accurate programmable droop allowing to reduce number of output capacitors, accurate enable circuit provides programmable start up point for Bus voltage, PGOOD output, programmable switching frequency and hiccup current limiting circuitry.

FEATURES

- Differential inductor DCR sensing eliminates the problem with layout parasitic
- External programmable voltage droop
- Low Impedance On-board Drivers
- Hiccup current limit
- Power Good for power sequencing
- Enable Signal allows external shutdown as well as programming the BUS voltage start up threshold
- Programmable frequency
- Prebias start up
- Over voltage protection without negative spike at output
- Pb-free and RoHS compliant

APPLICATIONS

- Graphic card High Current Vcore Supply
- High Current +40A on board DC to DC converter applications

TYPICAL APPLICATION

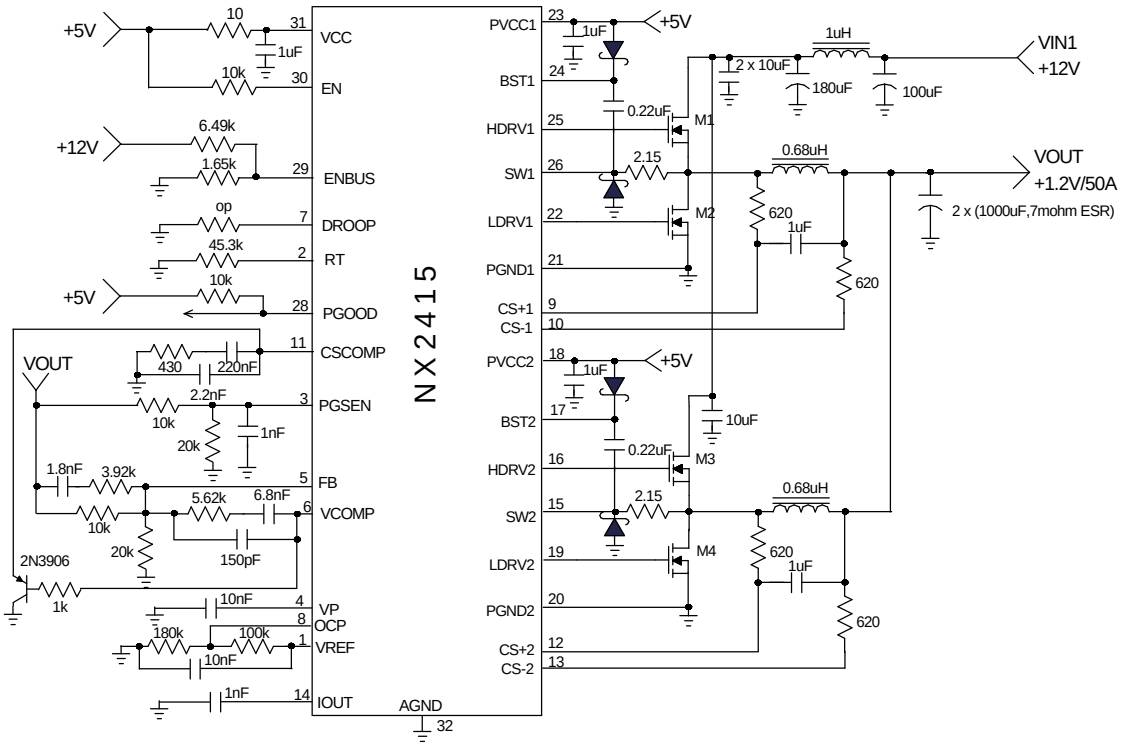

Figure1 - Typical application of NX2415

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX2415CMTR	0 to 70°C	MLPQ-32L	200kHz to 1MHz	Yes

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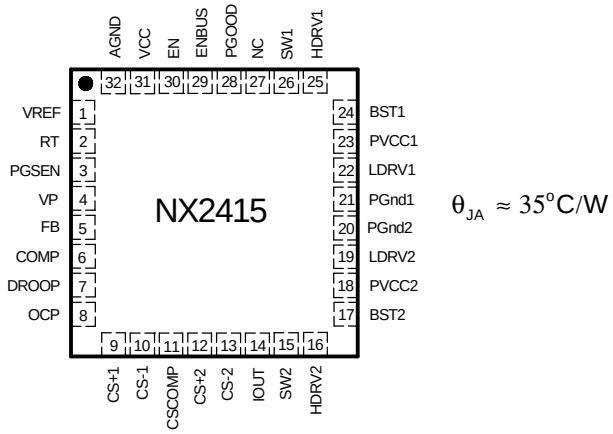
ABSOLUTE MAXIMUM RATINGS

Vcc to PGND & BST to SW voltage ..... -0.3V to 6.5V
BST to PGND Voltage ..... -0.3V to 35V
SW to PGND ..... -2V to 35V
All other pins ..... -0.3V to 6.5V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... -40°C To 125°C
Lead temperature(Soldering 5s) ..... 260°C

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

32-LEAD PLASTIC MLPQ 5 x 5



$\theta_{JA} \approx 35^{o}C/W$

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc = 5V, V_{BST}-V_{SW}=5V, EN=HIGH, and T_A = 0 to 70°C. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage(Vcc) V_{CC} ,PV_{CC} Voltage Range	V_{CC}		4.5	5	5.5	V
V_{CC} Supply Current (static)	I_{CC} (Static)	EN=LOW	-	6.6		mA
PV_{CC} Supply Current (Dynamic)	ICC (Dynamic)	EN&ENBUS HIGH, Freq=200Khz per phase C_{LOAD}=2200PF		4		mA
V_{BST} Voltage Range	V_{BST} to V_{SW}		4.5	5	5.5	V
V_{BST} Supply Current ((Dynamic))	V_{BST} (Dynamic)	EN&ENBUS HIGH, Freq=200Khz per phase C_{LOAD}=2200PF		4		mA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Under Voltage, Vcc , Enable(EN) & ENBUS						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising		4		V
V_{CC}-Hysteresis	V_{CC}_Hyst			0.2		V
EN Threshold		V_{cc} Rising		0.6		V
EN Hysteresis				0.1		V
ENBUS Threshold		V_{BUS} Rising		1.6		V
ENBUS Hysteresis				0.16		V
Reference Voltage						
Ref Voltage	V_{REF}	4.5V<Vcc<5.5V		0.8		V
Ref Voltage line regulation				1		%
Oscillator (Rt)						
Frequency for each phase	Fs	Rt=45kohm		400		KHz
Ramp-Amplitude Voltage	V_{RAMP}			1		V
Ramp Peak				2.5		V
Ramp Valley				1.5		V
Max Duty Cycle		200Khz/Phase		95		%
Min Duty Cycle					0	%
Transconductance Amplifiers(CSCOMP)						
Open Loop Gain			50	65		dB
Transconductance				1600		umoh
Voltage Mode Error Amplifier						
Open Loop Gain			50			dB
Input Offset Voltage	Vio_v			0		mV
Output Current Source			5			mA
Output Current Sink			5			mA
Output HI Voltage			Vcc-1.5			V
Output LOW Voltage					0.5	V
SS (Internal)						
Soft Start time	Tss	200Khz/Phase		20		mS
Power Good(Pgood)						
Threshold		V_{SEN} Falling		74		$\%V_{ID}$
Hysteresis				5		%
PGood Voltage Low		I_{PGood}=-5mA		0.5		V
High Side Driver(C_L=4700pF)						
Output Impedance , Sourcing Current	R_{source}(Hdrv)	I=200mA		1.1		ohm
Output Impedance , Sinking Current	R_{sink}(Hdrv)	I=200mA		0.8		ohm
Rise Time	THdrv(Rise)	V_{BST}-V_{SW}=4.5V		24		ns
Fall Time	THdrv(Fall)	V_{BST}-V_{SW}=4.5V		24		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10%-10%		30		ns

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PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Low Side Driver (C_l =4700pF) Output Impedance, Sourcing Current	R_{source}(Ldrv)	I=200mA		1.1		ohm
Output Impedance, Sinking Current	R_{sink}(Ldrv)	I=200mA		0.5		ohm
Rise Time	TLdrv(Rise)	10% to 90%		40		ns
Fall Time	TLdrv(Fall)	90% to 10%		36		ns
Deadband Time	Tdead(H to L)	SW going Low to Ldrv going High, 10% to 10%		30		ns
Current Sense Amplifier(CS+, CS-) Current Sense Amplifier Mismatch				0		mV
Voltage Gain	K		29.7	30	30.3	V/V
Droop Voltage Current Source(Droop) Droop Voltage Current Source		V(IOUT)=0.6V,feedback resistor=10kohm,Rdroop=60 kohm		100		uA
OCP Adjust Blank time before activating OCP		200Khz/Phase		15		uS
Vref Reference Voltage				1.6		V
Driving current ability				5		mA
OVP Threshold OVP Threshold				0.96		V

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PIN DESCRIPTIONS

PIN #	SYMBOL	PIN DESCRIPTION
31	VCC	IC's supply voltage. This pin biases the internal logic circuits. A minimum 1uF ceramic capacitor is recommended to connect from this pin to ground plane.
25, 16	HDRV1, HDRV2	High side gate driver outputs.
22, 19	LDRV1, LDRV2	Low side gate driver outputs.
30	EN	This pin is used to remotely turn off the controller. The pin has a threshold voltage of 0.6 volts.
24, 17	BST1,BST2	These pins supplies voltage to high side FET drivers.
26,15	SW1,SW2	These pins are connected to the source pins of the upper fets.
23, 18	PVCC1, PVCC2	These pins provide the supply voltage for the lower MOSFET drivers.
28	PGOOD	This pin is an open collector output. If used, it should be pulled to 5V with a resistor greater than or equal to 10k, otherwise it my be left open. Any fault or under voltage on the enable pins will cause the signal to be pulled low.
4	VP	Input to the positive pin of the error amplifier. A resistor is connected from the output of the DAC to this pin. Place a small capacitor from this pin to GND to filter any noise.
5	FB	This pin is the error amplifier inverting input. It is connected to the output voltage via a voltage divider.
2	RT	This pin programs the internal oscillator frequency using a resistor from this pin to ground. The frequency of each phase is 1/2 of this frequency.
9,12	CS+1,CS+2	Positive input of the differential current sense amplifiers. It is connected directly to the RC junction of the respective phase's output inductor.
10,13	CS-1,CS-2	Negative input of the differential current sense amplifiers. It is connected directly to the negative side of the respective phase's output inductor.
11	CSCOMP	The output of the transconductance op amp for current balance circuit. An external RC is connected from this pin to GND to stabilize the current loop.
6	VCOMP	This is the output pin of the error amplifier. The compensation network connection.
7	DROOP	A resistor from this pin to ground programs an internal current source that is fed into the FB pin. This current source is proportional to the output current of the regulator. The product of this current times the external resistor RFB provides a droop voltage.

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PIN #	SYMBOL	PIN DESCRIPTION
8	OCP	A resistor divider connected from this pin to Vref programs the current limit threshold. The outputs of the internal current sense differential amplifiers are summed together to represent the output current. This voltage is then compared to this threshold.
1	VREF	A 1.6V buffered reference is brought out.
29	ENBUS	This pin is used to program the under voltage lockout of the bus supply. A resistor divider from the bus voltage to this pin programs the under voltage lockout. When the voltage of this pin is greater than 1.6V, the bus voltage is assumed in operation. The pin has a 10% hysterisis.
21, 20	PGND1, PGND2	This is the ground connection for the power stage of the controller.
32	AGND	Controller analog ground pin.
14	IOUT	Input of OCP amplifier. Place a 10nF to 100nF capacitor from this pin to GND to filter any noise.
3	PGSEN	Output over voltage and Pgood sensing pin. A resistor divider plus a small capacitor should be connected to the this pin to set the OVP and Pgood.

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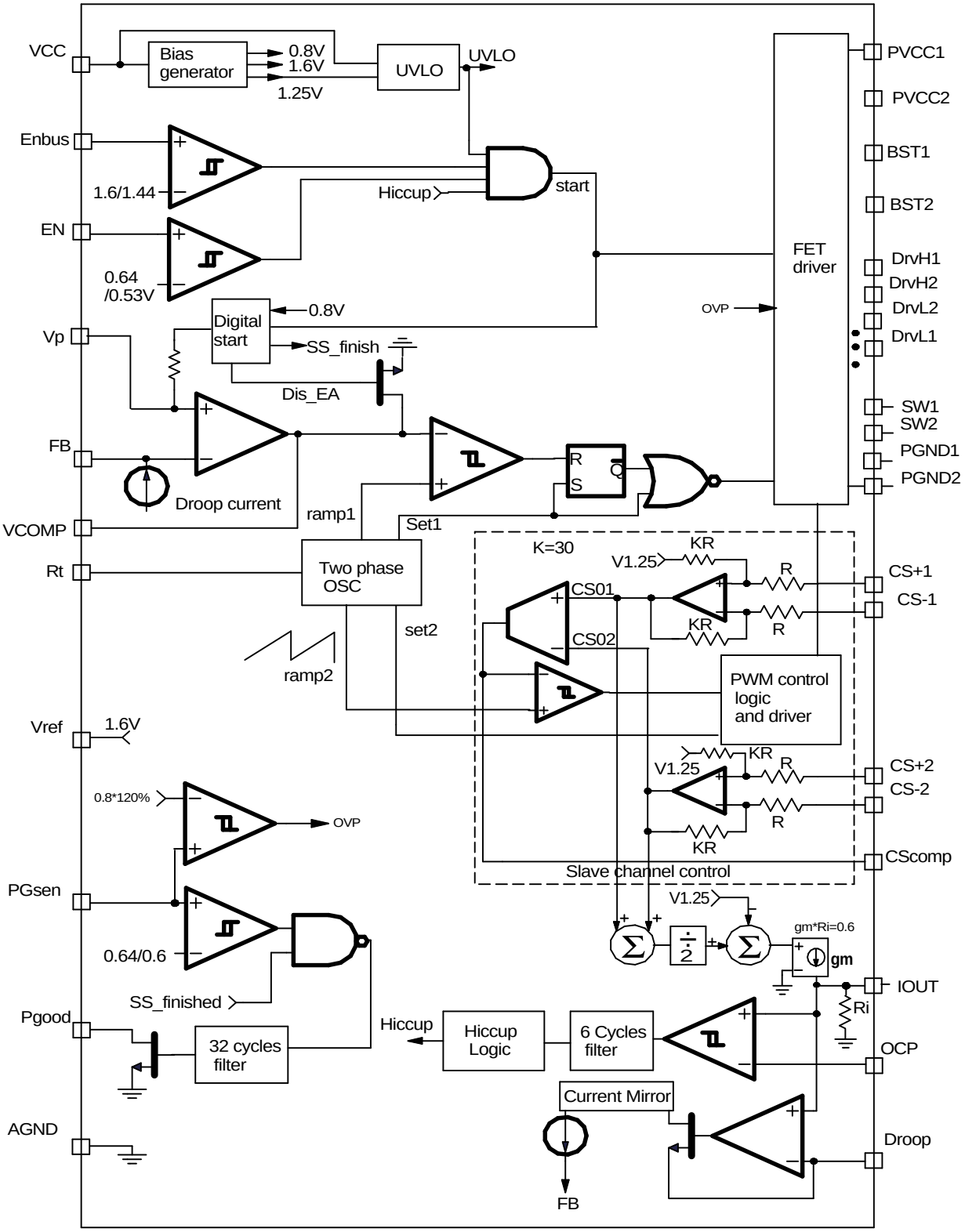
BLOCK DIAGRAM



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APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage

V_{OUT} - Output voltage

I_{OUT} - Output current

ΔV_{RIPPLE} - Output voltage ripple

F_S - Operation frequency for each channel

ΔI_{RIPPLE} - Inductor current ripple

Design Example

The following is typical application for NX2415.

V_{IN} = 12V

V_{OUT}=1.2V

I_{OUT}=50A

I_{OUT_max}=60A

ΔV_{RIPPLE} <=12mV

ΔV_{DROOP}<=120mV @30A step

F_S=400kHz

Phase number N=2

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{\Delta I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$

$$\Delta I_{RIPPLE}=k\times\frac{I_{OUTPUT}}{N} \quad ...(1)$$

where k is between 0.2 to 0.4.

Select k=0.2, then

$$L_{OUT}=\frac{12V-1.2V}{0.2\times\frac{50A}{2}}\times\frac{1.2V}{12V}\times\frac{1}{400kHz}$$

L_{OUT}=0.54uH

Choose inductor from Vishay IHLP_5050FD-01 with L=0.68uH DCR=1.4mΩ.

Current Ripple is recalculated as

$$\Delta I_{RIPPLE}=\frac{V_{IN}-V_{OUT}}{L_{OUT}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$

$$=\frac{12V-1.2V}{0.68uH}\times\frac{1.2V}{12V}\times\frac{1}{400kHz}=3.97A \quad ...(2)$$

Output Capacitor Selection

Output capacitor value is basically decided by the output voltage ripple, capacitor RMS current rating and load transient.

Based on Voltage Ripple

For electrolytic, POSCAP bulk capacitor, the ESR (equivalent series resistance) and inductor current typically determines the output voltage ripple.

$$ESR_{desire}=\frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}=\frac{12mV}{3.97A}=3.022m\Omega \quad ...(3)$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. For example, for 12mV output ripple, SANYO OSCON capacitors 2R5SEPC1000MX(1000uF 7mΩ) are chosen.

$$N=\frac{ESR_E\times\Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(4)$$

Number of Capacitor is calculated as

$$N=\frac{7m\Omega\times3.97A}{12mV}$$

N =2.3

For ceramic capacitor, the current ripple is determined by the number of capacitor instead of ESR

$$C_{OUT}=\frac{\Delta I_{RIPPLE}}{8\times F_S\times\Delta V_{RIPPLE}} \quad ...(5)$$

Typically, the calculated capacitance is so small that the output voltage droop during the transient can not meet the spec although ripple is small.

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Based On Transient Requirement

Typically, the output voltage droop during transient is specified as:

$\Delta V_{DROOP} < \Delta V_{TRAN}$ @ step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One Section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, overshoot caused by ΔI_{STEP} transient load which is from high load to low load, can be estimated as the following equation,if assuming the bandwidth of system is high enough.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(6)$$

where t is the a function of capacitor, etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L_{EFF} \le L_{crit} \\ \dfrac{L_{EFF} \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L_{EFF} \ge L_{crit} \end{cases} \quad ...(7)$$

where

$$L_{EFF} = \frac{L_{OUT}}{N} = \frac{0.68uH}{2} = 0.34uH$$

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(8)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is dependent on the ESR of capacitor.

In most cases, the output capacitors are multiple capacitors in parallel. The number of capacitors can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(9)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L_{EFF} \le L_{crit} \\ \dfrac{L_{EFF} \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L_{EFF} \ge L_{crit} \end{cases} \quad ...(10)$$

For example, assume voltage droop during transient is 120mV for 30A load step.

If the OS-CON capacitors (1000uF, 7mΩ) is used, the critical inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} = \frac{7m\Omega \times 1000\mu F \times 1.2V}{30A} = 0.28\mu H$$

The effective inductor value is 0.34uH which is bigger than critical inductance. In that case, the output voltage transient not only dependent on the ESR, but also capacitance.

number of capacitors is

$$\tau = \frac{L_{EFF} \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E = \frac{0.34\mu H \times 30A}{1.2V} - 7m\Omega \times 1000\mu F = 1.5us$$

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L_{EFF} \times C_E \times \Delta V_{tran}} \times \tau^2 = \frac{7m\Omega \times 30A}{120mV} + \frac{1.2V}{2 \times 0.34\mu H \times 1000\mu F \times 120mV} \times (1.5us)^2 = 1.78$$

The number of capacitors has to satisfied both ripple and transient requirement. Overall, we can choose N=2.

It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to be chosen after the test. Typically, for high frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% to 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitic can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

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Control Loop Compensator Design

NX2415 can control and drive two channel synchronous bucks with 180° phase shift between each other. One of two channels is called master, the other is called slave. They are connected together by sharing the same output capacitors. Voltage loop is designed to regulate output voltage. In order to achieve the current balance in these two synchronous buck converters, current loop compensation network is employed to to make sure the currents in slave is following the master.

Voltage Loop Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response,compensator is employed to provide highest possible bandwidth and enough phase margin. Ideally, the Bode plot of the closed loop system has crossover frequency between 1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo OSCON and POSCAP, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator.

In design example, six electrolytic capacitors are used as output capacitors. The system is compensated with type III compensator. The following figures and equations show how to realize the this type III compensator with electrolytic capacitors.

$$F_{Z1} = \frac{1}{2\times\pi\times R_4\times C_2} \quad ...(11)$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R_2+R_3)\times C_3} \quad ...(12)$$

$$F_{P1} = \frac{1}{2\times\pi\times R_3\times C_3} \quad ...(13)$$

$$F_{P2} = \frac{1}{2\times\pi\times R_4\times\frac{C_1\times C_2}{C_1+C_2}} \quad ...(14)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator.

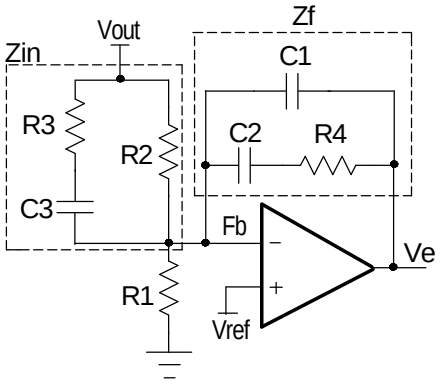

Figure 2 - Type III compensator

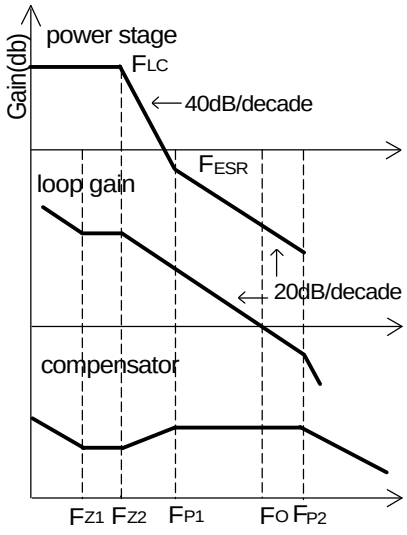

Figure 3 - Bode plot of Type III compensator

The transfer function of type III compensator is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1}{sR_2\times(C_2+C_1)}\times\frac{(1+sR_4\times C_2)\times[1+s(R_2+R_3)\times C_3]}{(1+sR_4\times\frac{C_2\times C_1}{C_2+C_1})\times(1+sR_3\times C_3)}$$

Use the same power stage requirement as demo board. The crossover frequency has to be selected as $F_{LC}<F_{ESR}<F_O$, and usually $F_O<=1/10\sim1/5F_S$.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{L_{EFF}\times C_{OUT}}} = \frac{1}{2\times\pi\times\sqrt{0.34uH\times 2000uF}} = 6.1kHz$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}} = \frac{1}{2\times\pi\times 3.5m\Omega\times 2000uF} = 22.7kHz$$

2.Set R_2 equal to10kΩ.

$$R_1 = \frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}} = \frac{10k\Omega\times 0.8V}{1.2V-0.8V} = 20k\Omega$$

Choose R_1= 20kΩ.

3. Calculate C_3 by setting $F_{Z2} = F_{LC}$ and $F_{p1} = F_{ESR}$.

$$C_3 = \frac{1}{2\times\pi\times R_2}\times(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}) = \frac{1}{2\times\pi\times 10k\Omega}\times(\frac{1}{6.1kHz}-\frac{1}{22.7kHz}) = 1.9nF$$

Choose C_3=1.8nF.

5. Calculate R_3 by equation (13).

$$R_3 = \frac{1}{2\times\pi\times F_{P1}\times C_3} = \frac{1}{2\times\pi\times 22.7kHz\times 1.8nF} = 3.89k\Omega$$

Choose R_3=3.92kΩ.

6. Calculate R_4 by choosing F_O=40kHz.

$$R_4 = \frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L_{EFF}}{ESR}\times\frac{R_2\times R_3}{R_2+R_3} = \frac{1V}{12V}\times\frac{2\times\pi\times 40kHz\times 0.34uH}{3.5m\Omega}\times\frac{10k\Omega\times 3.92k\Omega}{10k\Omega+3.92k\Omega} = 5.73k\Omega$$

Choose R_4=5.62kΩ.

7. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2 = \frac{1}{2\times\pi\times F_{Z1}\times R_4} = \frac{1}{2\times\pi\times 0.75\times 6.1kHz\times 5.62k\Omega} = 6.2nF$$

Choose C_2=6.8nF.

8. Calculate C_1 by equation (14) with pole F_{p2} at half the switching frequency.

$$C_1 = \frac{1}{2\times\pi\times R_4\times F_{P2}} = \frac{1}{2\times\pi\times 5.62k\Omega\times 200kHz} = 141pF$$

Choose C_1=150pF.

B. Type II compensator design

If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 4. R3 and C1 introduce a zero to cancel the double pole effect. C2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain = \frac{R_3}{R_2} \quad \text{... (15)}$$

$$F_z = \frac{1}{2\times\pi\times R_3\times C_1} \quad \text{... (16)}$$

$$F_p \approx \frac{1}{2\times\pi\times R_3\times C_2} \quad \text{... (17)}$$

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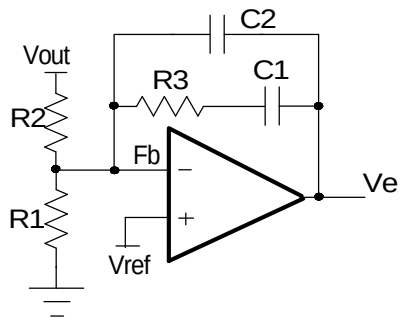

Figure 4 - Type II compensator

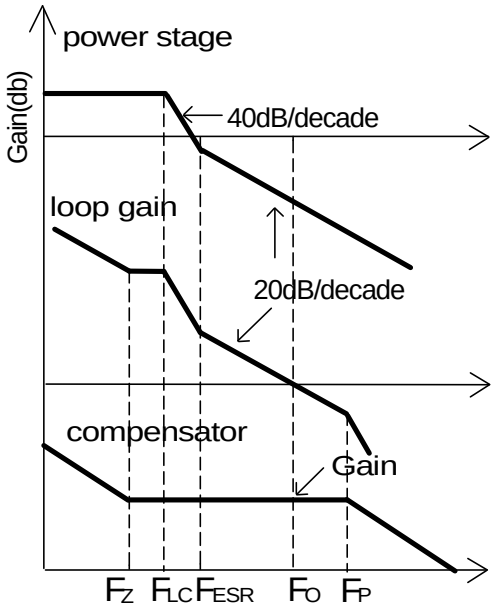

Figure 5 - Bode plot of Type II compensator

For this type of compensator, F_O has to satisfy $F_{LC}<F_{ESR}<< F_O$ and $F_O<=1/10~1/5F_s$.

Here a type II compensator is designed for the case which has six electrolytic capacitors(1800uF, 13mΩ) and two 1.5uH inductors.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{EFF}\times C_{OUT}}}$$
$$=\frac{1}{2\times\pi\times\sqrt{0.75uH\times 10800uF}}$$
$$=1.768kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$=\frac{1}{2\times\pi\times 13m\Omega\times 1800uF}$$
$$=6.801kHz$$

2.Set R_2 equal to10kΩ and calculate R_1.

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{10k\Omega\times 0.8V}{1.2V-0.8V}=20k\Omega$$

3. Set crossover frequency F_O=15kHz.

4.Calculate R_3 value by the following equation.

$$R_3=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L_{EFF}}{ESR}\times R_2$$
$$=\frac{1V}{12V}\times\frac{2\times\pi\times 15kHz\times 0.75uH}{2.16m\Omega}\times 10k\Omega$$
$$=27.3k\Omega$$

Choose R_3 =27.4kΩ.

5. Calculate C_1 by setting compensator zero F_Z at 75% of the LC double pole.

$$C_1=\frac{1}{2\times\pi\times R_3\times F_z}$$
$$=\frac{1}{2\times\pi\times 27.4k\Omega\times 0.75\times 1.768kHz}$$
$$=4.4nF$$

Choose C_1=4.7nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2=\frac{1}{\pi\times R_3\times F_s}$$
$$=\frac{1}{\pi\times 27.4k\Omega\times 100kHz}$$
$$=116pF$$

Choose C_2=100pF.

Current Loop Compensator Design

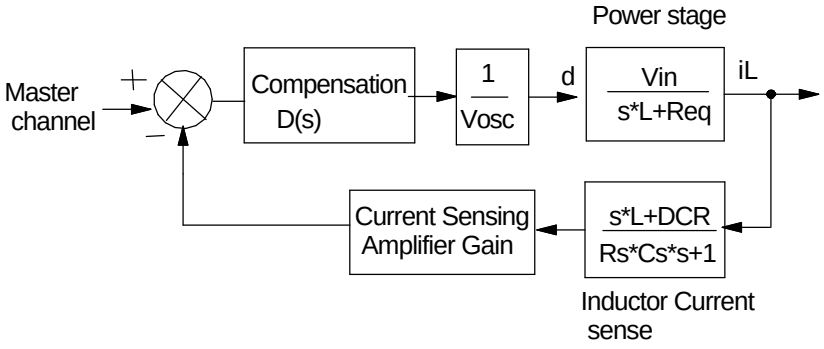

Figure 6 - Current loop control diagram

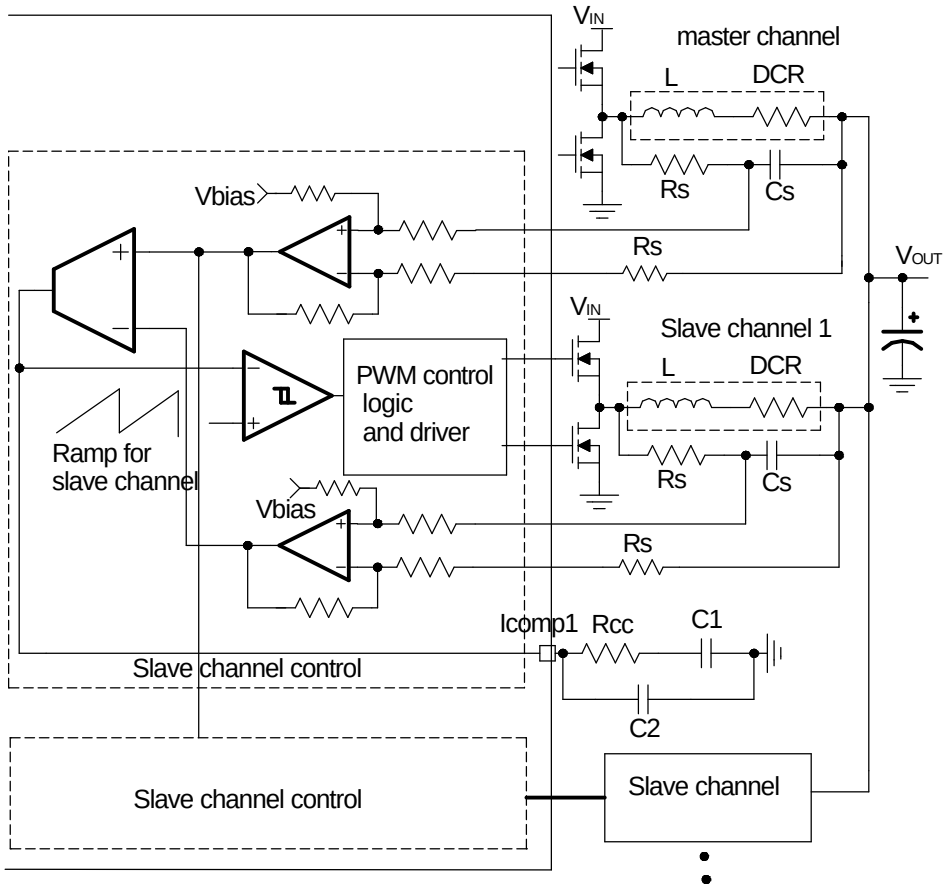

Figure 7 - Function diagram of current loop

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Inductor Current Sensing

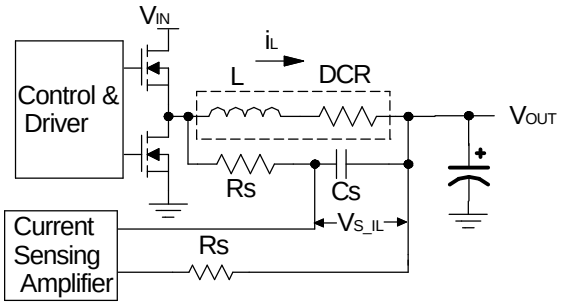

Figure 8 - Inductor current sensing using RC network.

The inductor current can be sensed through a RC network as shown above. The advantage of the RC network is the lossless comparing with a resistor in series with output inductor.

The selection of the resistor sensing network is chosen by the following equation:

$$R_S \times C_S = \frac{L}{DCR} \qquad ...(18)$$

If the above equation is satisfied, the voltage across the sensing capacitor Cs will be equal to the inductor current times DCR of inductor for all frequency domain.

$$V_{S\_IL} = DCR \times i_L$$

If the sensing capacitor is chosen

$$C_S = 1\mu F$$

C_S must be X7R or COG ceramic capacitor.

The sensing resistor is calculated as

$$R_S = \frac{L}{DCR \times C_S}$$

For example, for 0.68uH inductor with 1.4mΩ DCR, we have

$$R_S = \frac{0.68\mu H}{1.4m\Omega \times 1\mu F} = 486\Omega$$

In most of cases, the selection of sensing resistor based on the above equation will be sufficient. However, for some inductor such as toroid coiled inductor with micrometal, even the product of sensing resistor and capacitor is perfectly match with L/DCR, the voltage across the capacitor still has overshoot due to the nonlinearity of inductor. This will affect the droop accuracy during the transient if droop function is required. The illustration is shown in the following figure.

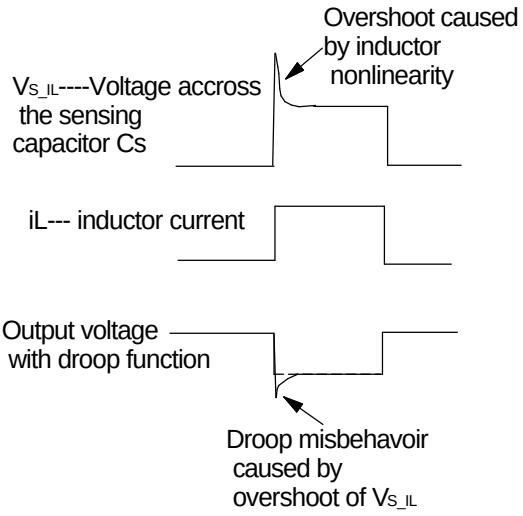

Figure 9 - Droop accuracy affected by the nonlinearity of inductor.

In this case, the sensing resistor has to be chosen

$$R_S \geq \frac{L}{DCR \times C_S}$$

to compensate the overshoot. This selection only affects the small signal mode of current loop. For DC accuracy, there is no effect since the DC voltage across the sensing capacitor will equal to the DCR times inductor current at DC load no matter what Rs is. In this example, Rs=620Ω.

R_S value is preferred to be less than 400Ω in NX2415's application, therefore we need to reiterate the calculation, choose C_S 2.2uF instead. R_S value is finally chosen as 301Ω .

Powe dissipation of Rs resistor is calculated as followed:

$$P_D(R_S) = \frac{(V_{IN} - V_{OUT})^2}{R_S} \times D + \frac{V_{OUT}^2}{R_S} \times (1 - D)$$

$$= \frac{(12V - 1.2V)^2}{301\Omega} \times 0.1 + \frac{(1.2V)^2}{301\Omega} \times (1 - 0.1)$$

$$= 0.04W$$

The power rating of Rs should be over 0.04W.

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Current Loop Compensation

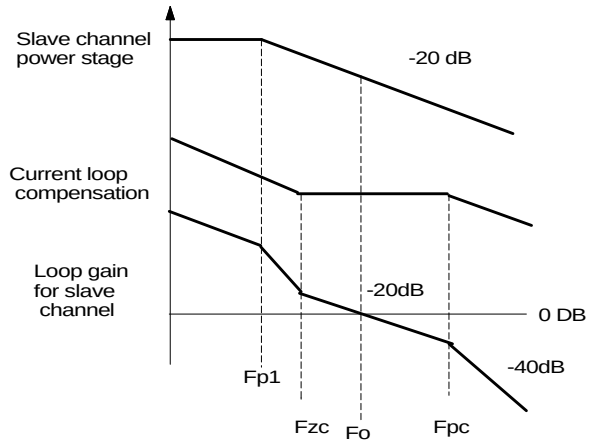

Figure 10 - Bode plot of current loop

The diagram and bode plot for current loop of NX2415 is shown in above figures. The current signal through inductor sensing is amplified by current sensing differential amplifier. The amplified slave current signal is compared with the amplified inductor current from master channel (channel 1 for NX2415) through a transconductance amplifier, the difference between channel current will change the output of transconductance amplifier, which will compare with a internal ramp signal and changes the duty cycle of slave channel buck converter. If the inductor are perfectly matched and the PWM controller has no offset, the DC current in slave channel will equal to the DC current of master channel (channel 1) due to the gain of current loop.

From the bode plot, the power stage has one pole located at

$$F_{P1} = \frac{R_{eq}}{2\times\pi\times L}$$

where R_{eq} is the equivalent resistor and it is given by

$$R_{eq} \approx DCR + R_{dson\_con}\times\frac{V_{OUT}}{V_{IN}} + R_{dson\_syn}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

R_{dson_con} is the Rdson of control FET and R_{dson_syn} is the Rdson of synchronous FET. For this example,

$$R_{eq} = 7.4m\Omega$$

The pole is located as

$$F_{P1} = \frac{R_{eq}}{2\times\pi\times L} = \frac{7.4m\Omega}{2\times\pi\times 0.68\mu H} = 1.7kHz$$

The current compensation transfer function is given as

$$D(s) = \frac{g_m}{s\times(C_1+C_2)}\times\frac{1+s\times R_{cc}\times C_1}{1+s\times\frac{R_{cc}\times C_1\times C_2}{C_1+C_2}}$$

It has one zero and one pole. The ideal is to choose resistor Rcc to achieve desired loop gain such as 50kHz. Rcc can be calculated as

$$R_{cc} = \frac{2\times\pi\times F_o\times L\times V_{osc}}{g_m\times V_{IN}\times K_C\times DCR} \quad ...(19)$$

where

$$K_C \approx \frac{60\cdot k\Omega}{2k\Omega+R_S} = 22.9$$

60kΩ and 2kΩ is the internal resistance for the current sensing amplifier.

For fast response, we can set the current loop cross-over frequency one and half times of voltage loop cross-over frequency. Since the voltage loop cross-over frequency is typically selected as 1/10 of switching frequency, we choose F_O=50kHz.

$$R_{cc} = \frac{2\times\pi\times 50kHz\times 0.68\mu H\times 1V}{1.6mA/V\times 12V\times 22.9\times 1.4m\Omega} = 442\Omega$$

Select

$R_{cc} = 430\Omega$.

The selection of capacitor C_1 is such that the zero of compensation will cancel the pole of power stage, therefore,

$$C_1 = \frac{L}{R_{eq}\times R_{cc}} = \frac{0.68\mu H}{7.4m\Omega\times 430\Omega} = 214nF$$

Typically, the capacitor C_1 is so big that the current loop may start slowly during the start up. Therefore, smaller capacitor can be selected. However, the selected capacitor can not reduce too much to cause phase droop.

Select C_1=220nF.

The capacitor C_2 is an option and it is used to filter out the switching noise. C_2 can be calculated as

$$C_2 = \frac{1}{\pi \times R_{cc} \times F_S} = \frac{1}{\pi \times 430\Omega \times 400kHz} = 1.85nF$$

Select C_2=2.2nF.

Frequency Selection

The frequency can be set by external Rt resistor. The relationship between frequency per phase and RT pin is shown as follows.

$$R_T \approx \frac{18600000}{F_S} \quad ...(20)$$

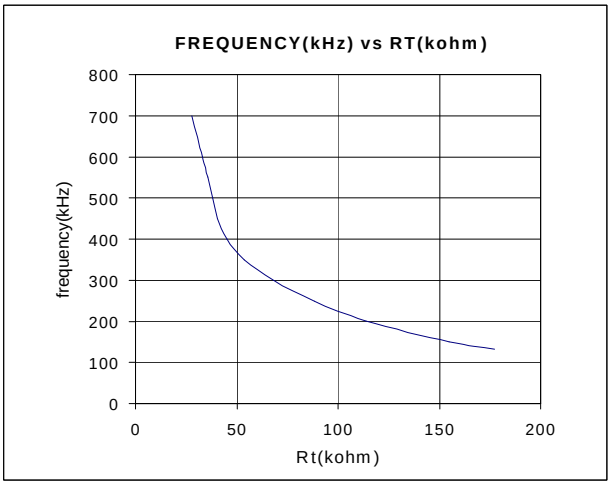

Figure 11 - Frequency vs Rt chart

Over Current/Short Circuit Protection

The converter will go into hiccup mode if the output current reaches a programmed limit V_{OCP} determined by the voltage at pin OCP.

$$V_{OCP} = 0.6 \frac{60k\Omega}{2k\Omega + R_S} \frac{DCR}{2} I_{OCP}$$

$$R_{OCP} = \frac{V_{OCP}}{V_{REF} - V_{OCP}} \times 100k\Omega \quad ...(21)$$

Where I_{ocp} is the desired over current protection level,100kΩ is the resistor connecting V_{REF} pin and I_{OCP} pin. R_S is the current sensing matching resistor when using DCR sensing method.

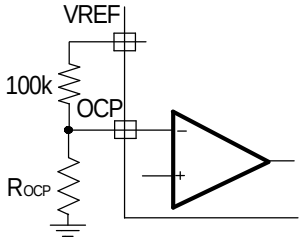

Figure 12 - Over current protection

Output Voltage Droop Operation

The effective output impedance of the controller must be adjusted to maximize the output voltage fluctuation range. A program resistor attached to the Droop pin R_{DROOP} will program this value. The function works by an internal current source connected to the FB pin. This current flows output of the FB pin and through the Rin resistance from the FB pin to the output.

This current source is a function of the sensed output current. As the output current increases, the droop current will increase and causes the output voltage todroop proportionately. The droop current is programmed by a resistor attached to the Droop pin. The value of the resistor is chosen as follows.

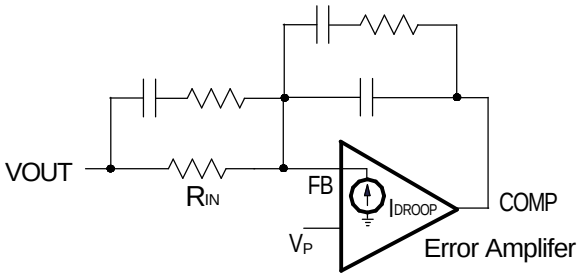

Figure 13 - Output voltage droop funciton

$$\Delta V_{OUT} = I_{DROOP} \times R_{IN} = \Delta I_{LOAD} \times R_{LL} \quad ...(22)$$

Where R_{LL} is desired load impedance. For example, if we want Vout droops 60mV @ 20A,

$$R_{LL} = \frac{60mV}{20A} = 3m\Omega$$

$$I_{DROOP} = \frac{V(IOUT)}{R_{DROOP}} = \frac{0.6 \times \frac{60k\Omega}{2k\Omega + R_S} \times \frac{DCR}{2} \times I_{LOAD}}{R_{DROOP}} \quad ...(23)$$

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Combine equation 22 and 23,

$$R_{DROOP} = \frac{0.6}{2}\frac{60k\Omega}{2k\Omega + R_S}\frac{DCR I_{LOAD} R_{IN}}{\Delta V_{OUT}} \quad ...(24)$$

Where DCR is the sense resistor or the DCR of the output inductor. R_S is the current sensing matching resistor when using DCR sensing method. I_{LOAD} is the load current. R_{IN} is the input DC resistor of the master phase compensator which connect FB pin and PGSEN pin. For example, to have the ΔV_{OUT}=60mV when the load current is 20A, DCR is 1.4mΩ, R_{IN} is 10kΩ, R_S is 620Ω.

$$R_{DROOP} = \frac{0.6}{2} \times \frac{60k\Omega}{2k\Omega + 0.62k\Omega} \times \frac{1.4m\Omega \times 20A \times 10k\Omega}{60mV}$$

$$= 32k\Omega$$

Choose R_{DROOP}= 32kΩ.

Over Voltage Protection

Over voltage protection is achieved by sensing the output voltage through resistor divider. The sensed voltage on PGSEN pin is compared with 120%*0.8V to generate the OVP signal. A small value capacitor is required to connect to PGSEN pin also.

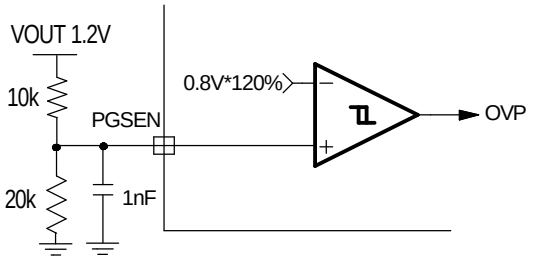

Figure 14 - Over voltage protection

Input Filter Selection

The selection criteria of input capacitor are voltage rating and the RMS current rating. For conservative consideration, the capacitor voltage rating should be 1.5 times higher than the maximum input voltage. The RMS current rating of the input capacitor for multi-phase converter can be estimated from the above Figure 15.

First, determine the duty cycle of the converter (V_O/V_{IN}). The ratio of input RMS current over output current can be obtained. Then the total input RMS current can be calculated. From this figure, it is obvious that a multi-phase converter can have a much smaller input RMS current, which results in a lower amount of input capacitors that are required.

For example, Vin=12V, Vout=1.2V. The duty cycle is D=Vout/Vin=1.2/12=10%. From the figure, for two phase, the normlized RMS current is 0.2*Iout=0.2*50A=10A.

A combination of ceramic and electrolytic(SANYO WG or WF series) or OSCON type capacitors can achieve both ripple current capability together with having enough capacitance such that input voltage will not sag too much. In this application, one OSCON SVPC180M(180uF, 16V, 2.8A) and three 10uF(4A rms current, X5R) ceramic capacitors are selected.

A 1uH input inductor is recommended to slow down the input current transient. Suppose power stage efficiency is 0.8, then input current can estimated by

$$I_{INPUT} = \frac{I_{OUT} \times V_{OUT}}{\eta \times V_{IN}} = \frac{60A \times 1.2V}{0.8 \times 12V} = 7.5A$$

In this application, Coilcraft DO3316P_102HC with RMS rating 10A is chosen.

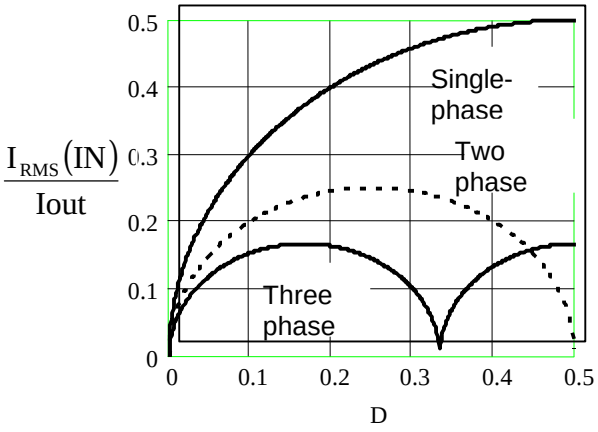

Figure 15 - Normalized input RMS current vs. duty cycle.

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Power MOSFETs Selection

The NX2415 requires two N-Channel power MOSFETs for each channels. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. In this design example, eight NTD60N02 are used. They have the following parameters: V_{DS}=25V, I_D=62A,R_{DSON}=12mΩ,Q_{GATE}=9nC.

There are three factors causing the MOSFET power loss:conduction loss, switching loss and gate driver loss.

Gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits. It is proportional to frequency and is defined as:

$$P_{gate} = (Q_{HGATE} \times V_{HGS} + Q_{LGATE} \times V_{LGS}) \times F_S \quad ...(24)$$

where Q_{HGATE} is the high side MOSFETs gate charge,Q_{LGATE} is the low side MOSFETs gate charge,V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage. This power dissipation should not exceed maximum power dissipation of the driver device.

Conduction loss is simply defined as:

$$P_{HCON} = I_{OUT}^2 \times D \times R_{DS(ON)} \times K$$
$$P_{LCON} = I_{OUT}^2 \times (1-D) \times R_{DS(ON)} \times K \quad ...(25)$$
$$P_{TOTAL} = P_{HCON} + P_{LCON}$$

Where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency and should be selected for the worst case. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times T_{SW} \times F_S \quad ...(26)$$

T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, I_{OUT} is output current, and F_S is switching frequency. Swithing loss P_{SW} is frequency dependent.

Soft Start and Enable Signal Operation

The NX2415 will start operation only after Vcc and PVcc have reached their threshold voltages and EN and ENBUS have been enabled. The ENBUS pin can be programmed to turn on the converter at any input voltage. The ENBUS pin has a threshold voltage of 1.6V.

Once the converter starts, there is a soft start sequence of 4082 steps between 0 and Vp. The ramp rate is determined by the switching frequency.

$$\frac{dV_O}{dt} = \frac{V_O}{4082 \times F_S} \quad ...(27)$$

The softstart time is calculated as followed:

$$T_{startup} = \frac{4082}{F_S} \quad ...(28)$$

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

There are two sets of components considered in the layout which are power components and small signal components. Power components usually consist of input capacitors, high-side MOSFET, low-side MOSFET, inductor and output capacitors. A noisy environment is generated by the power components due to the switching power. Small signal components are connected to sensitive pins or nodes. A multilayer layout which includes power plane, ground plane and signal plane is recommended .

Layout guidelines:

1. First put all the power components in the top layer connected by wide, copper filled areas. The input capacitor, inductor, output capacitor and the MOSFETs should be close to each other as possible. This helps to reduce the EMI radiated by the power loop due to the high switching currents through them.

2. Low ESR capacitor which can handle input RMS ripple current and a high frequency decoupling ceramic cap which usually is 1uF need to be practically touching the drain pin of the upper MOSFET, a plane connection is a must.

3. The output capacitors should be placed as close

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as to the load as possible and plane connection is required.

4. Drain of the low-side MOSFET and source of the high-side MOSFET need to be connected thru a plane ans as close as possible. A snubber nedds to be placed as close to this junction as possible.

5. Source of the lower MOSFET needs to be connected to the GND plane with multiple vias. One is not enough. This is very important. The same applies to the output capacitors and input capacitors.

6. Hdrv and Ldrv pins should be as close to MOSFET gate as possible. The gate traces should be wide and short. A place for gate drv resistors is needed to fine tune noise if needed.

7. Vcc capacitor, BST capacitor or any other bypassing capacitor needs to be placed first around the IC and as close as possible. The capacitor on comp to GND or comp back to FB needs to be place as close to the pin as well as resistor divider.

8. The output sense line which is sensing output back to the resistor divider should not go through high frequency signals.

9. All GNDs need to go directly thru via to GND plane.

10. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC.

11. In multilayer PCB, separate power ground and analog ground. These two grounds must be connected together on the PC board layout at a single point. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function.

12. Inductor current sense line should be connected directly to the inductor solder pad.

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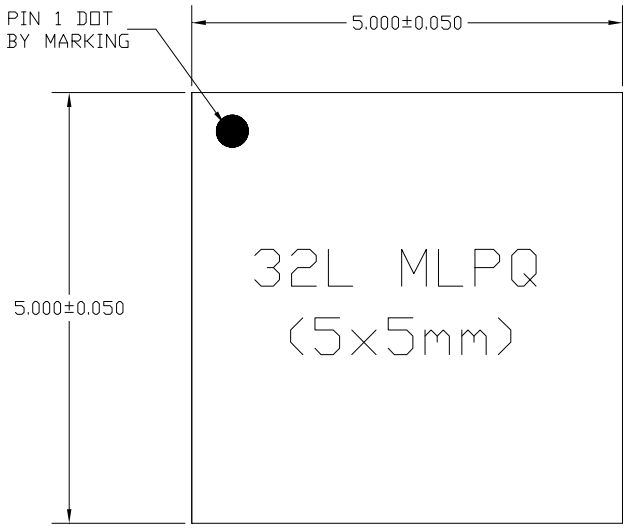
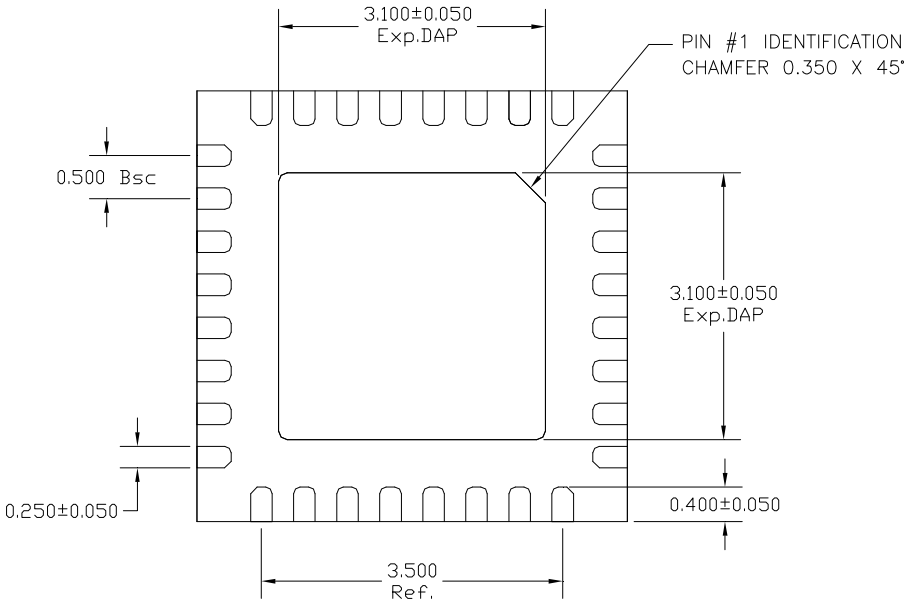
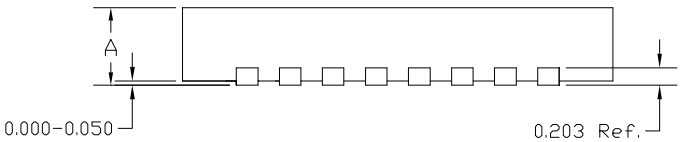
MLPQ 32 PIN 5 x 5 PACKAGE OUTLINE DIMENSIONS



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE: ALL DIMENSIONS ARE DISPLAYED IN MILLIMETERS.

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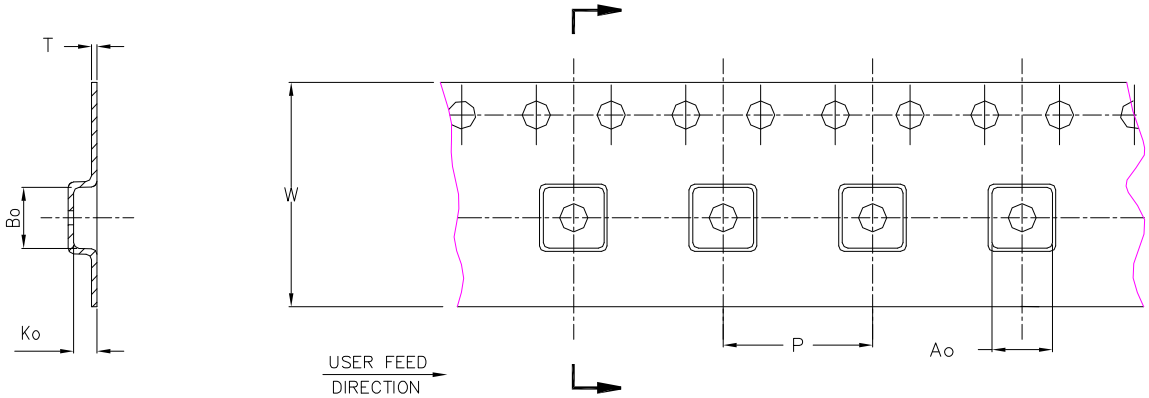
MLPQ 32 PIN 5 x 5 TAPE AND REEL INFORMATION



Dimension	MLPQ 05X05
Ao	5.30 +/− 0.1
Bo	6.30 +/− 0.1
Ko	1.2 +/− 0.1
P	8 +/− 0.1
W	12 +/− 0.3
T	0.3 +/− 0.05
R7/Quantity	1000
R13/Quantity	3000

NOTE:

1. R7 = 7 INCH LOCK REEL, R13 = 13 INCH LOCK REEL.
2. ALL DIMENSIONS ARE DISPLAYED IN MILLIMETERS.

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