SRAM MODULE

128K x 8 SRAM

FEATURES

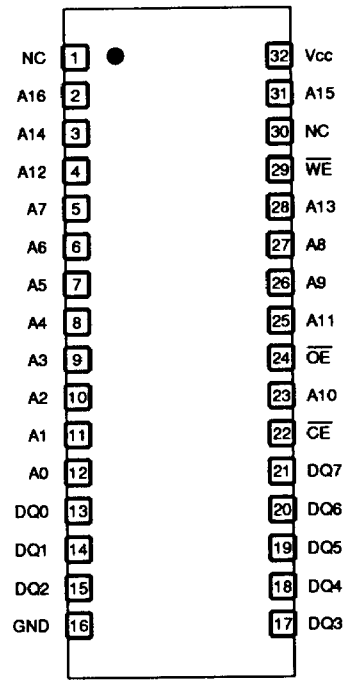
- High speed: 30ns, 35ns and 45ns
- High performance, low power, CMOS process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ function
- All inputs and outputs are TTL compatible

OPTIONS

	MARKING
• Timing	
30ns access	-30
35ns access	-35
45ns access	-45
• Packages:	
32-pin DIP (600 mil)	None
• Two Volt Data Retention	L

PIN ASSIGNMENT (Top View)

32 PIN DIP
(MR)



GENERAL DESCRIPTION

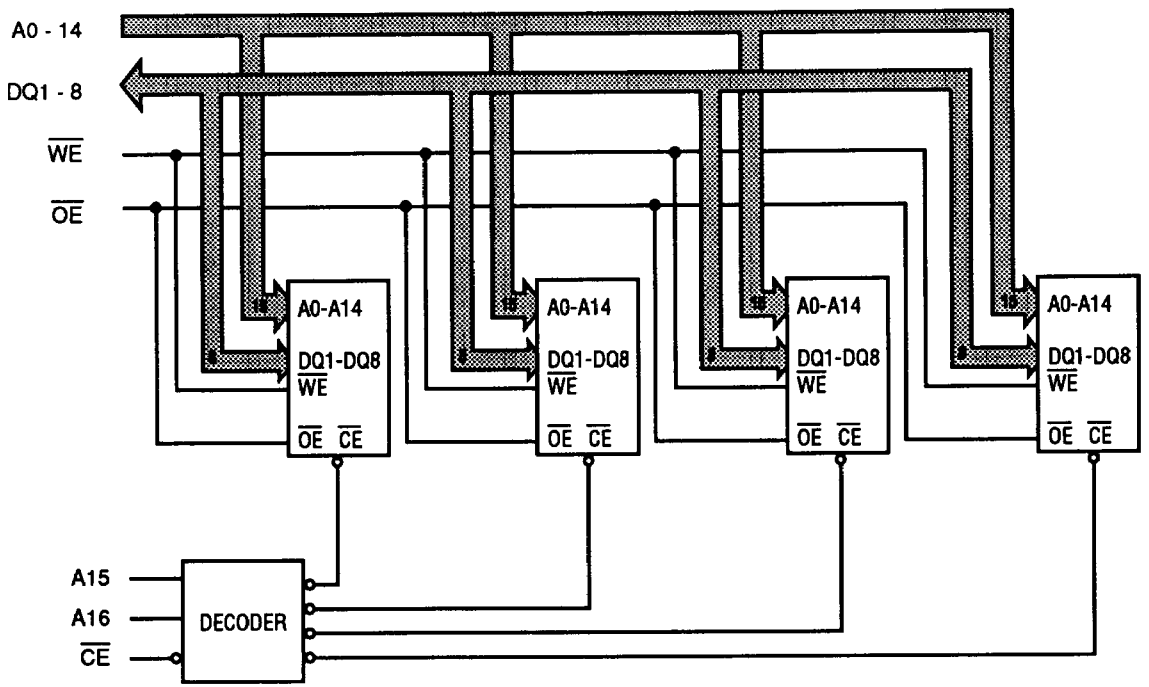
The MT85C8128 is a high speed SRAM memory module containing 131,072 words organized in a x8-bit configuration. The Micron DIP style module is manufactured using four 32Kx8 fast static RAMs together with a TTL (30ns and 35ns) or CMOS (45ns) decoder mounted on a FR4 printed circuit board.

The Micron SRAM family employs high speed, low power CMOS designs using a 4-transistor memory cell. They are fabricated using double layer metal, double layer polysilicon technology.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and chip enable $\overline{CE}$ inputs are both LOW. The CMOS decoder is used to interpret the higher order address bits (A15-16) to select one of the four fast static RAMs. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. $\overline{CE}$ can place the output in a high impedance state for additional flexibility in system design. Memory expansion is accomplished by use of the output enable ($\overline{OE}$) funtion.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible. The L option offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	OE	CE	WE	DQ	POWER
STANDBY	X	H	X	HIGH Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Storage Temperature ..... -55°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	-30, -35	-45	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.2	Vcc+1	Vcc+1	V	1
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	A0-A14	I_{LI}	-10	10	10	µA	
		A15, A16, $\overline{CE}$		-10	600	10	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$		I_{LO}	-10	10	10	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		10	V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	0.4	V	1

				MAX			
DESCRIPTION	CONDITIONS	SYMBOL	MIN	-30, -35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$, V_{CC} = Max., Outputs Open	I_{CC}		180	160	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$, V_{CC} = Max.	I_{SB1}		110	110	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2, V_{CC} = Max., $V_{IL} \le V_{SS}$ + 0.2, $V_{IH} \ge V_{CC}$ - 0.2, f = 0	I_{SB2}		40	20	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 5V	C_I		32	pF	4
Output Capacitance		C_O		32	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C, Vcc = 5V ± 10%)

DESCRIPTION	SYM	-30		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle									
READ cycle time	t_{RC}	30		35		45		ns	
Address access time	t_{AA}		30		35		45	ns	
Chip Enable access time	t_{ACE}		30		35		45	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip Enable LOW to output in low Z	t_{LZCE}	5		5		5		ns	7
Chip Enable to output in high Z	t_{HZCE}		20		20		25	ns	6, 7
Chip Enable LOW to power up time	t_{PU}	0		0		0		ns	
Chip Enable HIGH to power down time	t_{PD}		30		35		45	ns	
Output Enable Access Time	t_{AOE}		20		20		25	ns	
Output Enable LOW to output in low Z	t_{LZOE}	0		0		0		ns	
Output Enable HIGH to output in high Z	t_{HZOE}		20		20		30	ns	
WRITE Cycle									
WRITE cycle time	t_{WC}	30		35		45		ns	
Chip enable to end of write	t_{CW}	25		30		30		ns	
Address Valid to end of write	t_{AW}	25		25		30		ns	
Address set-up time	t_{AS}	0		0		0		ns	
Address hold from end of write	t_{AH}	2		2		2		ns	
Write pulse width	t_{WP}	25		25		30		ns	
Data set-up time	t_{DS}	15		15		18		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write Enable LOW to output in low Z	t_{LZWE}	0		0		0		ns	
Write Enable HIGH to output in high Z	t_{HZWE}	0	20	0	15	0	15	ns	6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

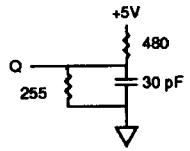


Fig. 1 OUTPUT LOAD EQUIVALENT

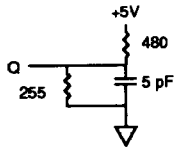


Fig. 2 OUTPUT LOAD EQUIVALENT

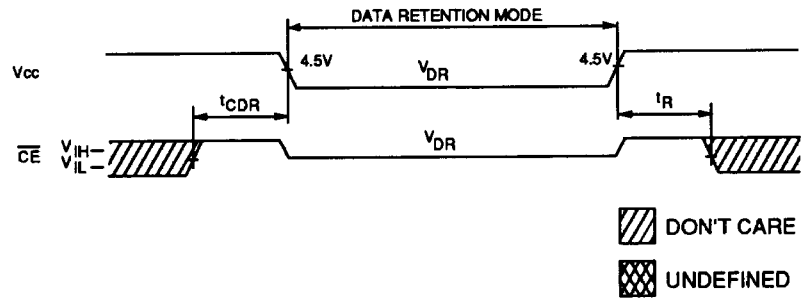
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.

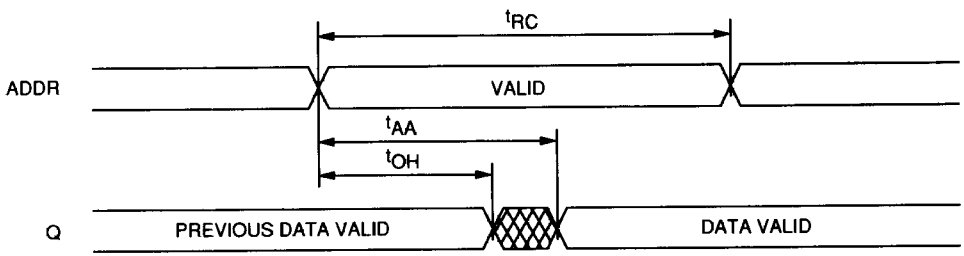
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) V_{IN} ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc=2v	I_{CCDR}		.9	4	mA	
		Vcc=3v			1.9	5	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

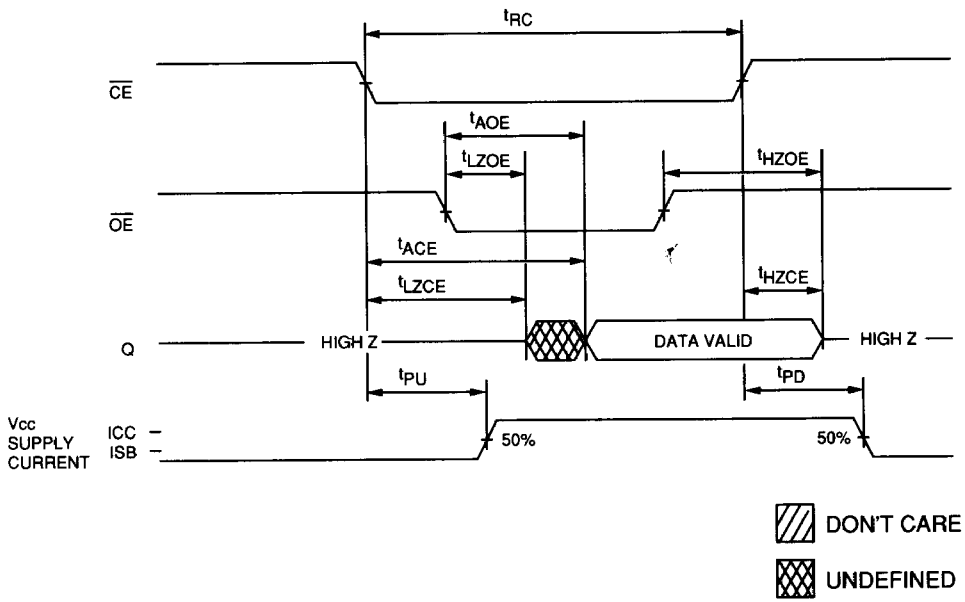
LOW Vcc DATA RETENTION WAVEFORM



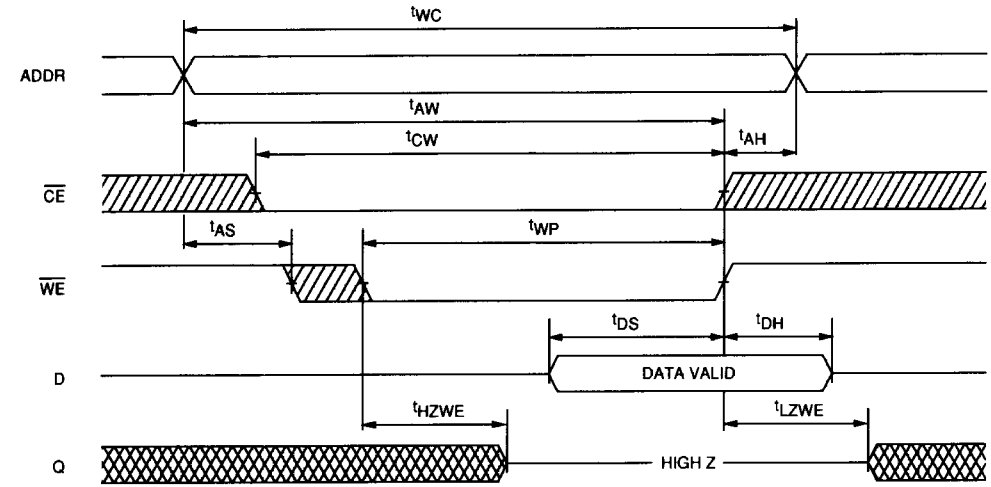
READ CYCLE NO. 1 (Notes 8, 9)



READ CYCLE NO. 2 (Notes 7, 8, 10)



WRITE CYCLE NO. 1
(Write Enable Controlled)



WRITE CYCLE NO. 2
(Chip Enable Controlled)