PARADIGM®

PRELIMINARY

1 Megabit Static RAM 256K x 4-Bit with Fast Sequential Access Mode

PSM44028S
PSM44028L

Features

- ☐ MIPS R4000 support
- ☐ High speed access times
  Com'l: 20, 25, and 35ns
  Mil : 20, 25, 35, and45ns
- ☐ Low power operation
  - PSM44028S
    Active: 400mW (typ.)
    Standby: 150 mW (typ.)
  - PSM44028L
    Active: 350mW (typ.)
    Standby: 100 mW (typ.)
- ☐ Single +5V (±10%) power supply
- ☐ TTL compatible inputs and outputs
- ☐ Military product MIL-STD-883, Rev. C
- ☐ Packages
  Sidebraze DIP(400 mil) - TC,
  Plastic SOJ(300 mil) - TSO,
  Plastic SOJ(400 mil) - SO

Description

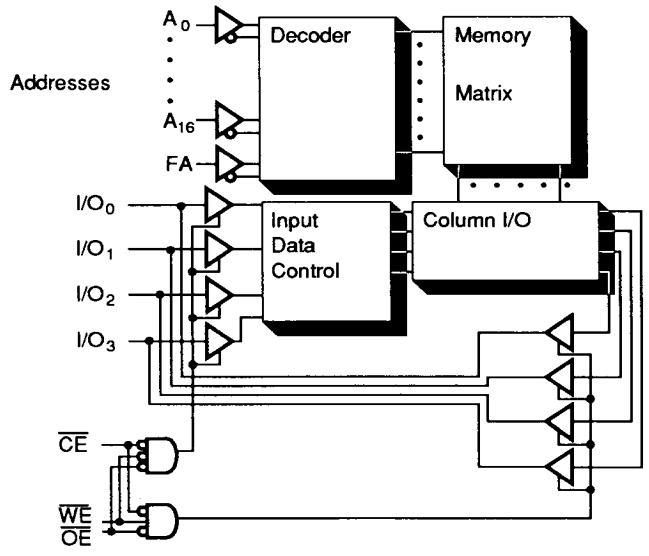
The PSM44028 is a high performance CMOS static RAM organized as 262144 x 4 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing to this device is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go to LOW. The PSM44028 has a feature which allows for a very fast sequential read. This mode will increase the efficiency of servicing primary cache misses when designing with the MIPS R4000 RISC processors.

The PSM44028 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PSM44028 comes in two versions, the standard power version PSM44028S and a low power version the PSM44028L. The two versions are functionally the same and only differ in their power consumption.

The PSM44028 is available in a 28-pin 400 mil DIP. The PSM44028 will also be available in a 28-pin 400 mil and 300 mil SOJ for surface mount applications.

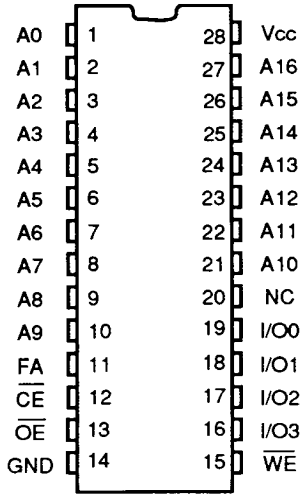
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Rev. C, making the PSM44028 ideally suited for military temperature applications.

Functional Block Diagram

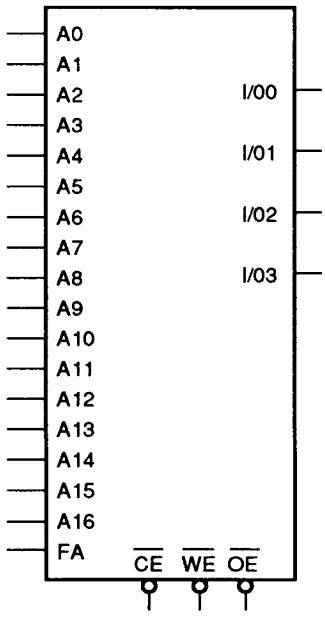


Pin Configuration

400 DIP
400 SOJ
300 SOJ



Logic Symbol



Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} (min) = -3.0V for pulse width less than 20ns.

Truth Table(1)

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D_{OUT}	Read
X	L	L	D_{IN}	Write
H	H	L	Hi-Z	Output Disable

NOTE:
1. H = V_{IH}, L = V_{IL}, X = DON'T CARE.

Pin Description

Symbol	Description
A0–A16	Address lines
FA	Fast sequence address
I/O–I/O3	Input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
V_{CC}	+5V power supply
GND	Ground
$\overline{WE}$	Write enable

Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions		PSM44028S Min.	PSM44028S Max.	PSM44028L Min.	PSM44028L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			Com'l	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CE} = V_{IH}$, V_{OUT} = GND to V_{CC}	MIL.	—	10	—	5	µA
			Com'l	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

DC Electrical Characteristics[1] ($V_{CC} = 5.0V \pm 10\%$, $V_{LC} \le 0.2V$, $V_{HC} \ge V_{CC} - 0.2$)

Symbol	Parameter	Power	Function	20, Com'l.	20, Mil.	25, Com'l.	25, Mil.	35, 45 [3]ns Com'l.	35, 45 [3]ns Mil.	Unit
I_{CC}	Dynamic Operating Current $\overline{CE} = V_{IL}$,	S	Read	170	180	160	170	150	160	mA
	V_{CC} = Max., f = f_{MAX}[2] I_{OUT} = 0mA	L	Read	170	180	160	170	150	160	mA
I_{SB}	Standby Power Supply Current (TTL Level)	S	—	50	50	40	40	30	30	mA
	$\overline{CE} \ge V_{IH}$, V_{CC} = Max., f = f_{MAX}[2]	L	—	40	40	35	35	30	30	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level)	S	—	10	10	10	10	10	10	mA
	$\overline{CE} \ge V_{HC}$, V_{CC} = Max., f = 0[2], $V_{IN} \ge V_{HC}$ or $\le V_{LC}$	L	—	5	5	5	5	5	5	mA

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
3. The 45ns speed grade is available in Military grade product only.

Capacitance[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input pulse levels	GND to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

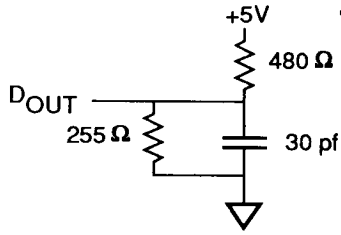


Fig. 1 Output Load Eqivalent

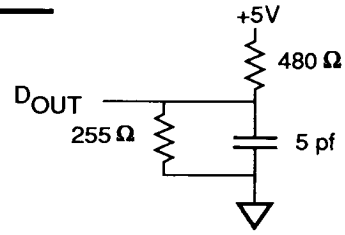
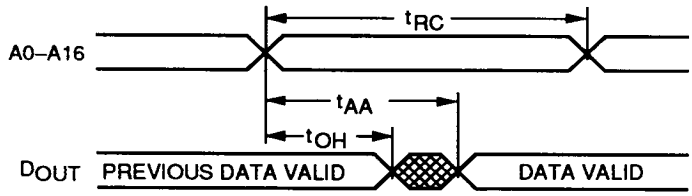
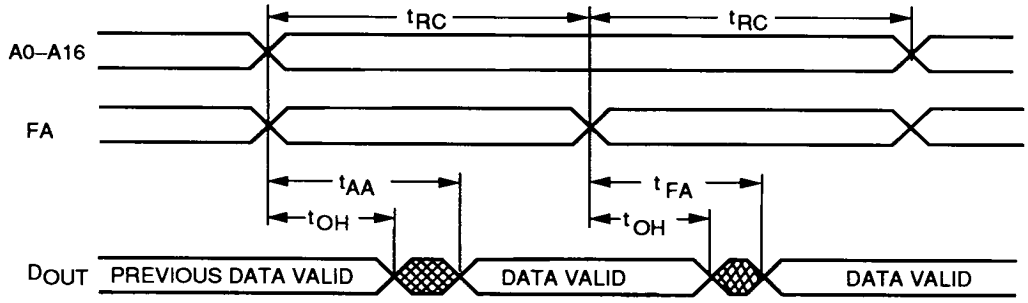


Fig. 2 Output Load Equivalent (for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE}, t_{LZOE}, t_{HZOE})

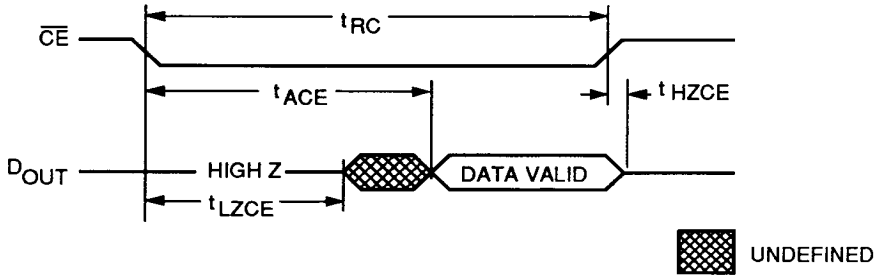
Read Cycle No. 1[6, 7]



Fast Sequential Read Cycle[6, 7]



Read Cycle No. 3[3, 6, 8]

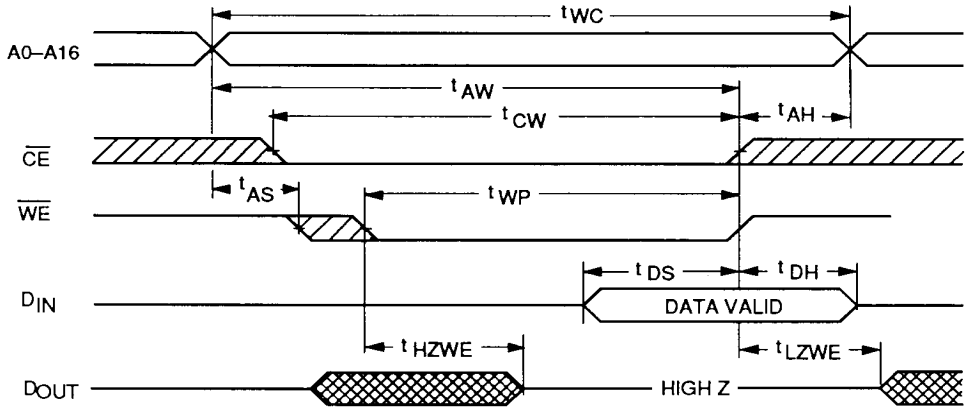


AC Electrical Characteristics V_{CC} = 5V ± 10%, All Temperature Ranges

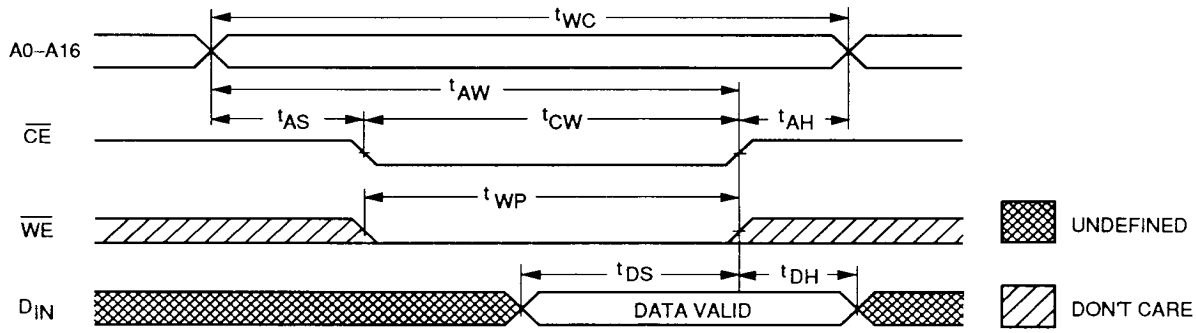
Description		-20		-25		-35		-45[1]		
READ Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
READ cycle time	t_{RC}	20		25		35		45		ns
Address access time	t_{AA}		20		25		35		45	ns
Chip enable access time	t_{ACE}		20		25		35		45	ns
Output hold from address change	t_{OH}	0		0		0		0		ns
Chip enable to output in low Z[4]	t_{LZCE}	5		5		5		5		ns
Chip disable to output in high Z[2, 3, 4]	t_{HZCE}		10		15		20		20	ns
Chip enable to power up time[4]	t_{PU}	0		0		0		0		ns
Chip disable to power downtime[4]	t_{PD}		20		25		30		40	ns
Output enable access time	t_{AOE}		10		12		15		20	ns
Output Enable to output in low Z[4]	t_{LZOE}	0		0		0		0		ns
Output disable to output in high Z[2, 4]	t_{HZOE}		8		10		10		15	ns
Fast Address Access Time	t_{FA}		5		6		7		10	ns

Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



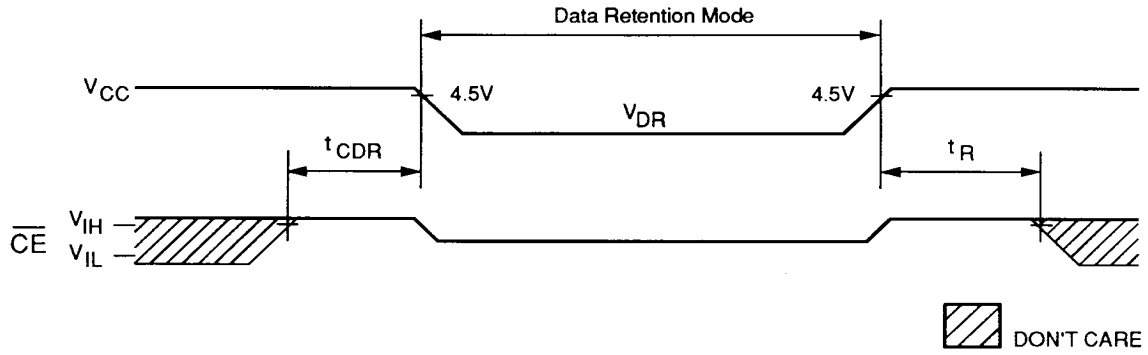
Write Cycle No. 2 (Chip Enable Controlled)



AC Electrical Characteristics V_{CC} = 5V ± 10%, All Temperature Ranges

Description		-20		-25		-35		-45[1]		
WRITE Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
WRITE cycle time	t_{WC}	20		25		35		45		ns
Chip enable to end of write	t_{CW}	17		20		30		40		ns
Address Valid to end of write	t_{AW}	17		20		30		40		ns
Address set-up time	t_{AS}	0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		ns
Write pulse width	t_{WP}	17		17		25		30		ns
Data set-up time	t_{DS}	12		12		15		20		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write disable to output in low Z[4]	t_{LZWE}	0		0		0		0		ns
Write enable to output in high Z[2, 4]	t_{HZWE}		8		10		15		20	ns

Low V_{CC} Data Retention Waveform

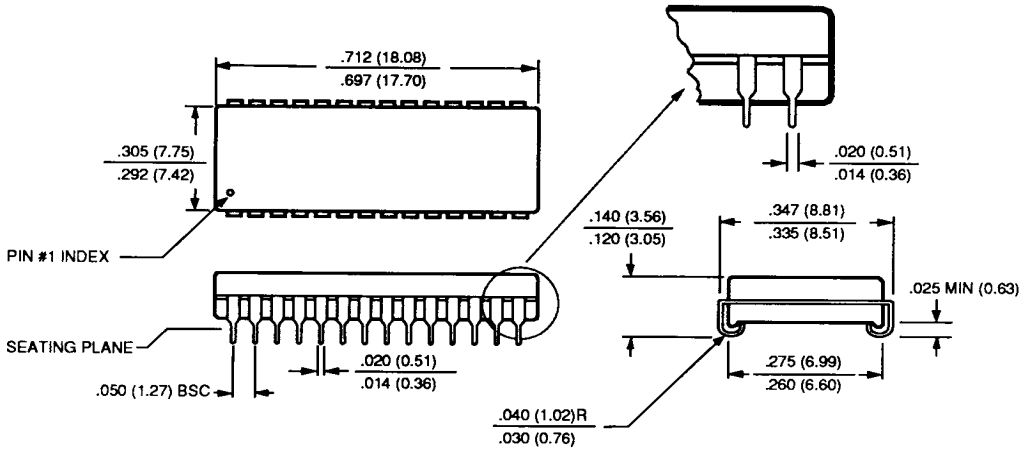


Data Retention Electrical Characteristics (L Version Only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$	$V_{CC} = 2V$	—	95	500	µA
		$V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 3V$	—	350	750	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(4)	Operation Recovery Time			t_{RC}(5)	—	—	ns

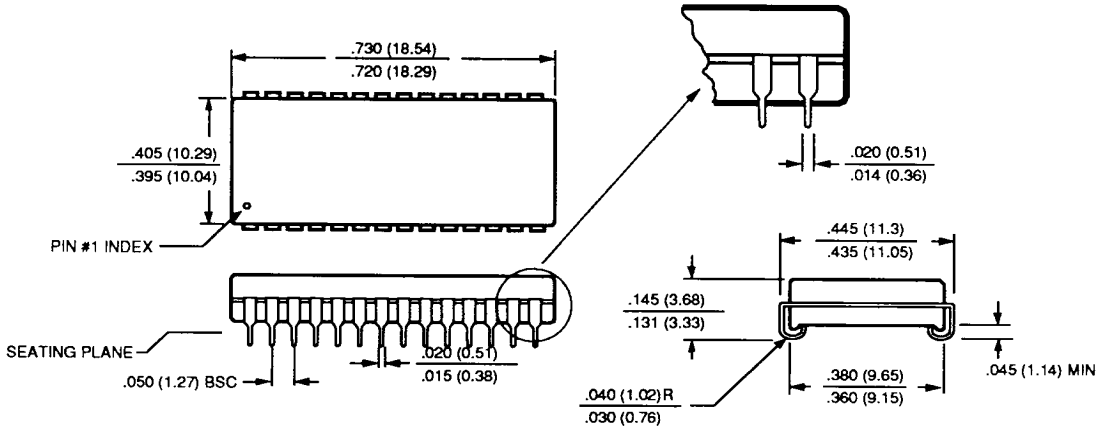
NOTES: (For 3 previous Electrical Characteristics tables)
1. -55°C to +125°C temperature range only.
2. t_{HZCE} and t_{HZWE} are tested with CL = 5pF as shown in Fig. #2. Transition is measured ±200mV from steady state voltage.
3. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
4. This parameter is sampled.
5. t_{RC} = Read cycle time.
6. $\overline{WE}$ is high for a READ cycle.
7. The device is continuously selected. All the Chip Enables are held in their active state.
8. The address is valid prior to or coincident with the latest occuring Chip Enable.

28 pin Plastic SOJ 300 mil



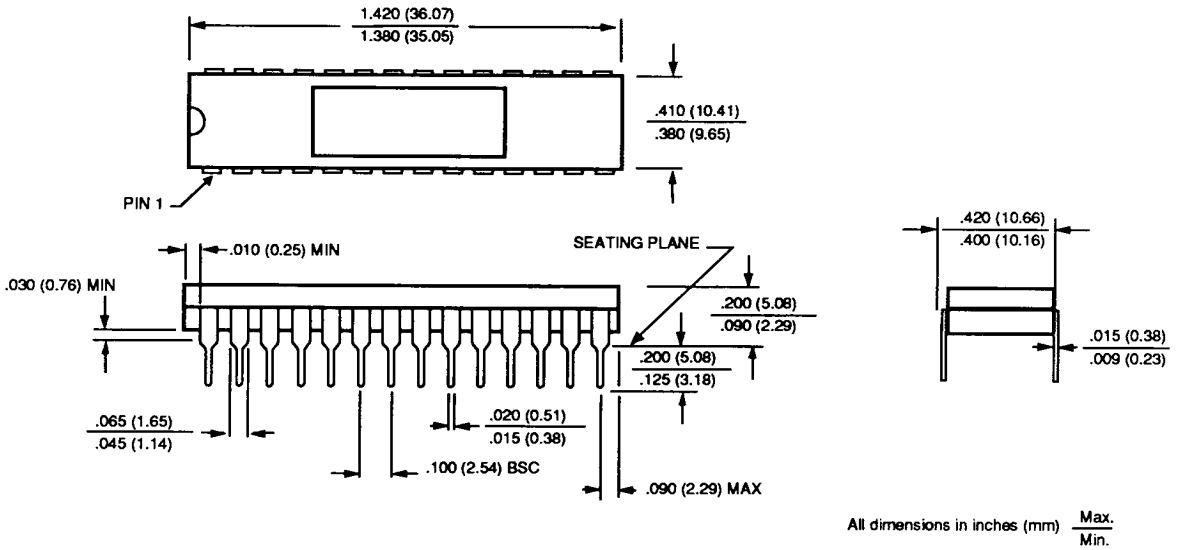
All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min}}$

28 pin Plastic SOJ 400 mil

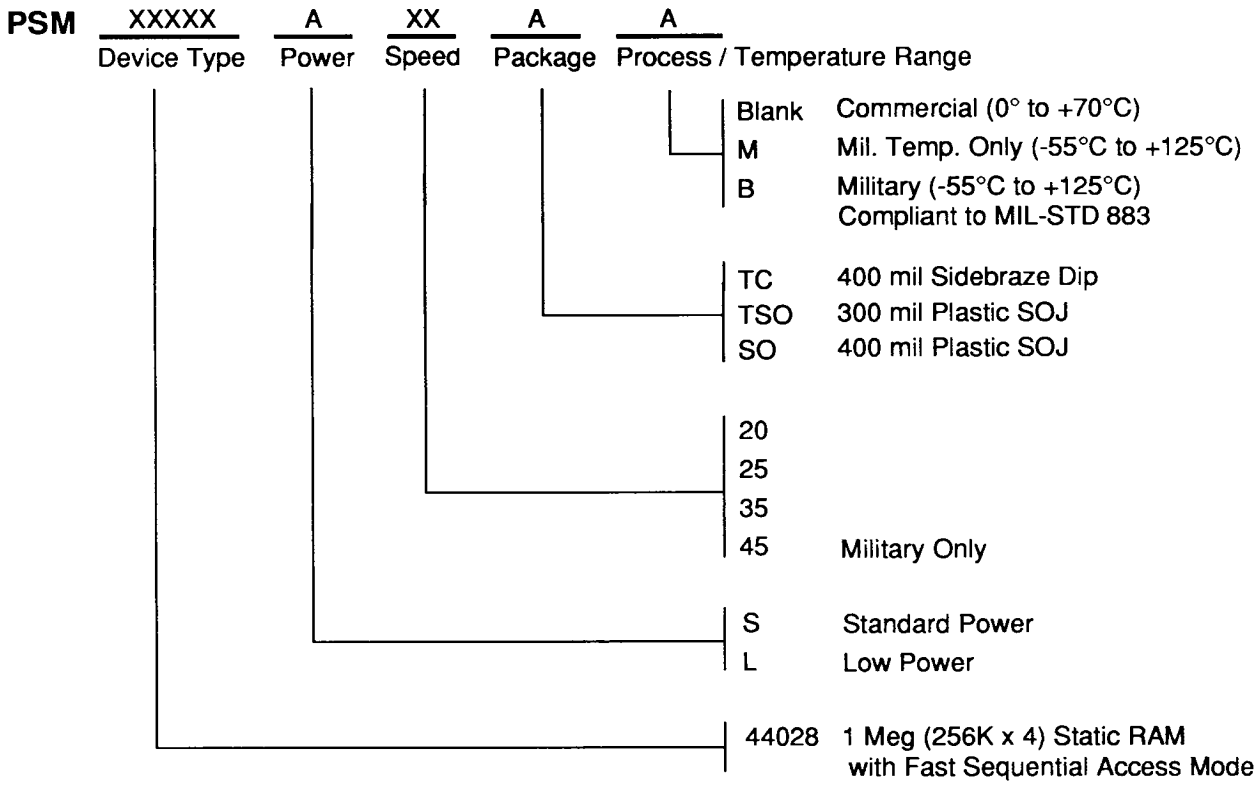


All dimensions in inches (millimeters) $\frac{\text{Max.}}{\text{Min}}$

28 pin 400 mil Sidebraze DIP



Ordering Information



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