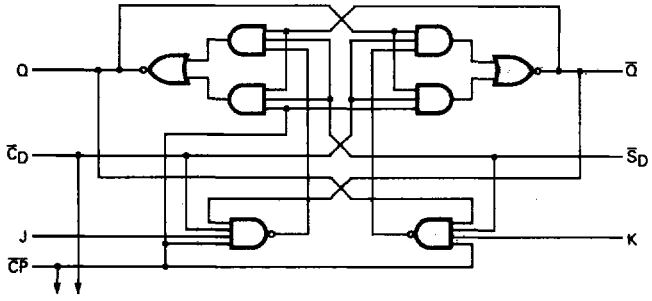
MOTOROLA

Product Preview

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP (WITH COMMON CLOCKS AND CLEARS)

DESCRIPTION — MC54F/74F114 contains two high-speed JK flip-flops with common clock and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

LOGIC DIAGRAM (one half shown)



TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_n - 1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse
t_n + 1 = Bit time after clock pulse

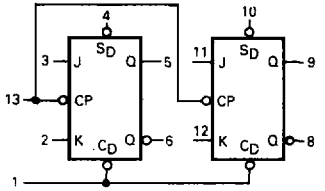
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54F/74F114

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

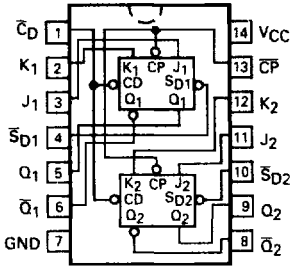
FAST™ SCHOTTKY TTL

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)
D Suffix — Case 751A-02 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage*	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

*74F devices may be operated over the 4.5 to 5.5 V supply range where they will meet the specifications of 54F devices over the 0° to 70°C temperature range.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	*Input Clamp Diode Voltage*				−1.2	V	I_{IN} = −18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.5 V
		74	2.7	3.4		V	I_{OH} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage			0.35	0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					100	μA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current (J and K Inputs)				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
	($\overline{CP}$ Inputs)				−2.4	mA		
	($\overline{C}_D$ and $\overline{S}_D$ Inputs)				−3.0	mA		
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current			12	19	mA	V_{CC} = MAX, V_{CP} = 0 V	

NOTES:
1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF MIN	54/74F MAX	54F T_A = −55 to +125°C, V_{CC} = 5.0 V ±10%, C_L = 50 pF MIN	54F MAX	74F T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%, C_L = 50 pF MIN	74F MAX	UNITS
f_{max}	Maximum Clock Frequency	110						MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	3.3 3.3	6.5 7.5			3.3 3.3	7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.0 2.0	6.5 6.5			2.0 2.0	7.5 7.5	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$, $V_{CC} = -5.0$ V			54F $T_A = -55$ to $+125°C$, $V_{CC} = 5.0$ V ±10%		74F $T_A = 0$ to $+70°C$, $V_{CC} = 5.0$ V ±10%		UNITS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_s (H) t_s (L)	Set up Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	4.0 3.0					4.0 3.0		ns
t_h (H) t_h (L)	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	0 0					0 0		
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width, HIGH or LOW	4.5 4.5					4.5 4.5		ns
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.5					4.5		ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $\overline{CP}$	4.0					5.0		ns

AC TEST CIRCUIT

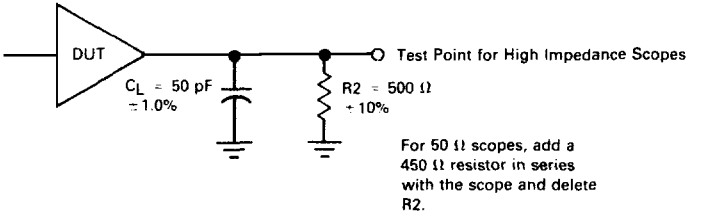


Fig. 1