

LH538300C

CMOS 8M (1M × 8) MROM

FEATURES

- 1,048,576 words × 8 bit organization
- Access time: 150 ns (MAX.)
- Low-power consumption:
 - Operating: 275 mW (MAX.)
 - Standby: 550 μW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
 - 32-pin, 600-mil DIP
 - 32-pin, 525-mil SOP
 - 32-pin, 400-mil TSOP (Type II)

DESCRIPTION

The LH538300C is a mask-programmable ROM organized as 1,048,576 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

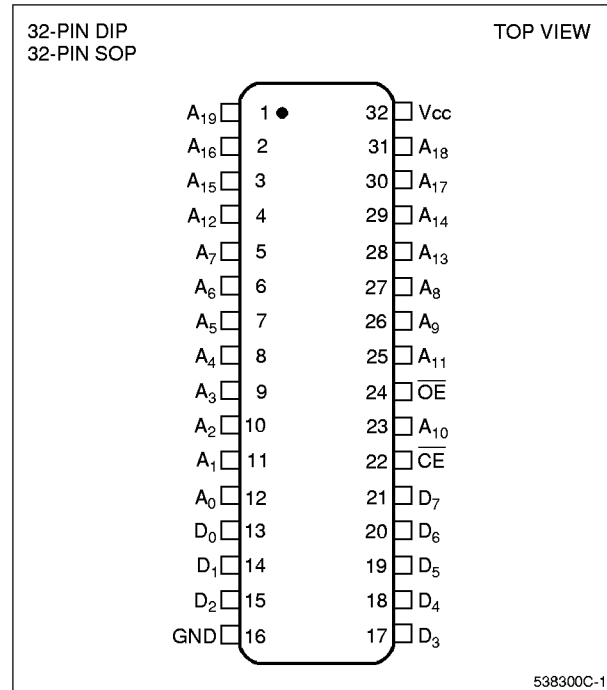


Figure 1. Pin Connections for DIP and SOP Packages

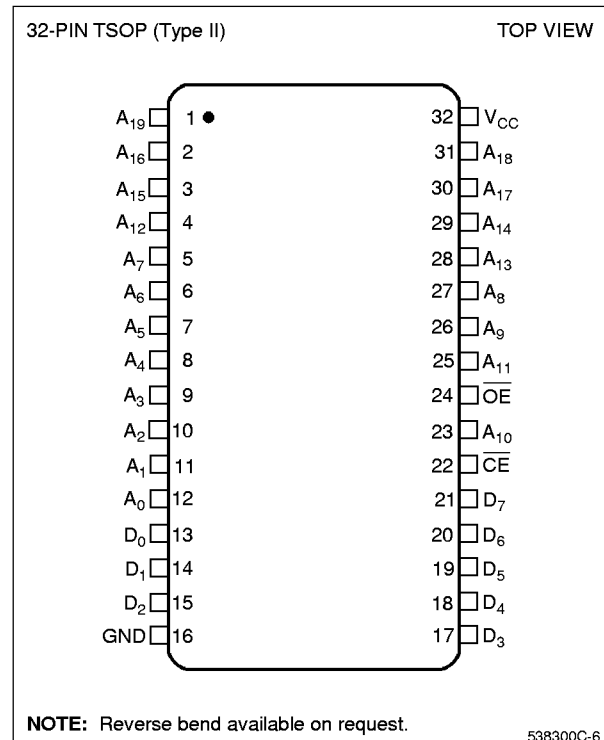
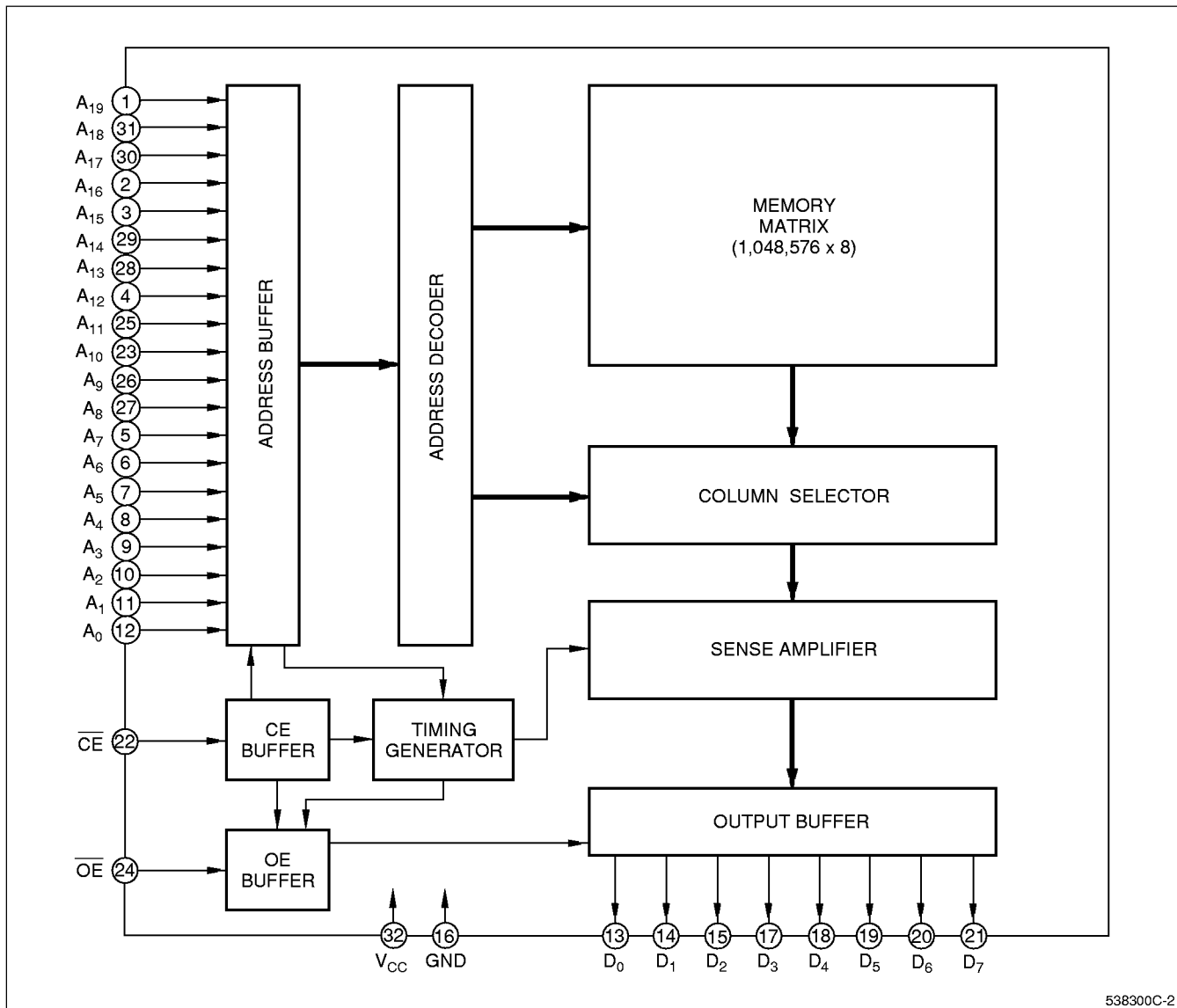


Figure 2. Pin Connections for TSOP Package



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Figure 3. LH538300C Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ – A ₁₉	Address input
D ₀ – D ₇	Data output
$\overline{\text{CE}}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{\text{OE}}$	Output Enable input
V _{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

\overline{CE}	\overline{OE}	D ₀ – D ₇	SUPPLY CURRENT	NOTE
H	X	High-Z	Standby (I _{SB})	1
L	H	High-Z	Operating (I _{CC})	
L	L	D _{OUT}	Operating (I _{CC})	

NOTE:

- X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	–0.3 to +7.0	V
Input voltage	V _{IN}	–0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	–0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V _{IL}		–0.3		0.8	V	
Input 'High' voltage	V _{IH}		2.2		V _{CC} + 0.3	V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V _{OH}	I _{OH} = –400 μA	2.4			V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}			10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}			10	μA	1
Operating current	I _{CC1}	t _{RC} = 150 ns			50	mA	2
	I _{CC2}	t _{RC} = 1 μs			40		
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$			3	mA	
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$			100		
Input capacitance	C _{IN}	f = 1 MHz			10	pF	
Output capacitance	C _{OUT}	T _A = 25°C			10	pF	

NOTES:

- $\overline{CE}/\overline{OE} = V_{IH}$
- V_{IN} = V_{IH} or V_{IL}, $\overline{CE} = V_{IL}$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable delay time	t_{OE}			70	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			60	ns	1
OE to output in High-Z	t_{OHZ}			60	ns	

NOTE:

1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected be-

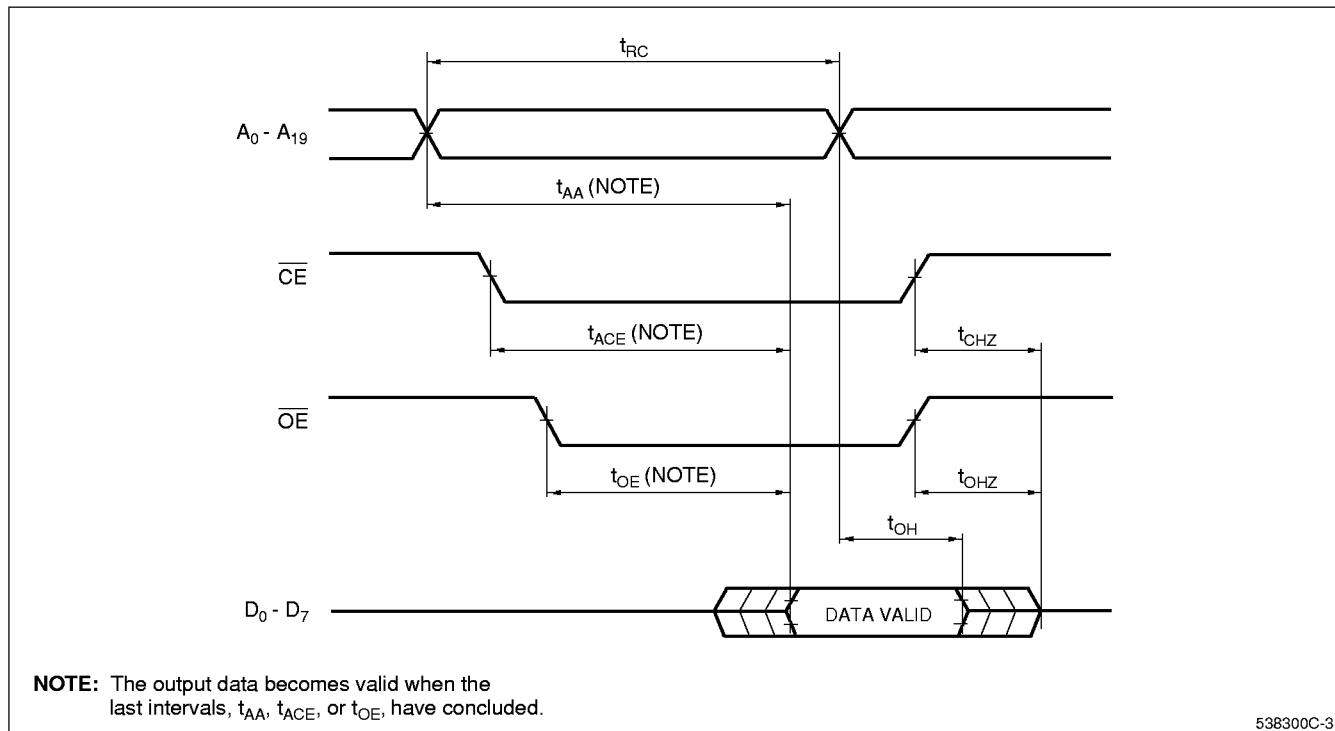
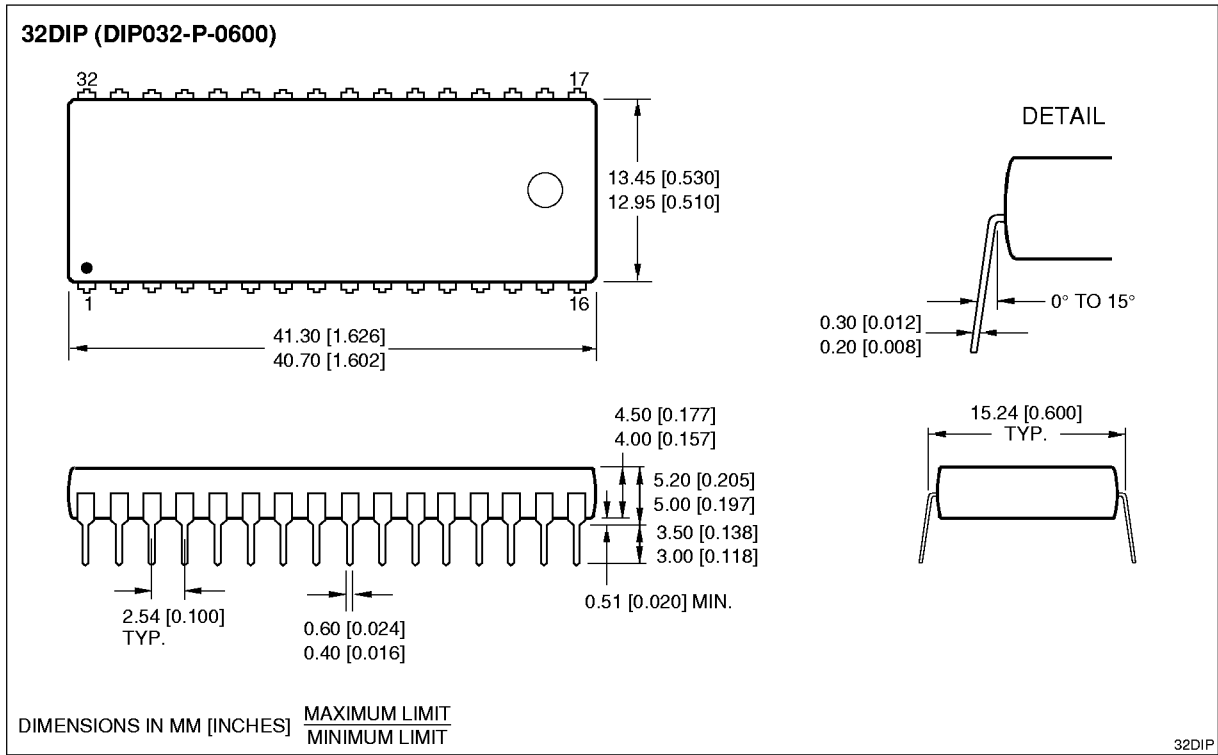


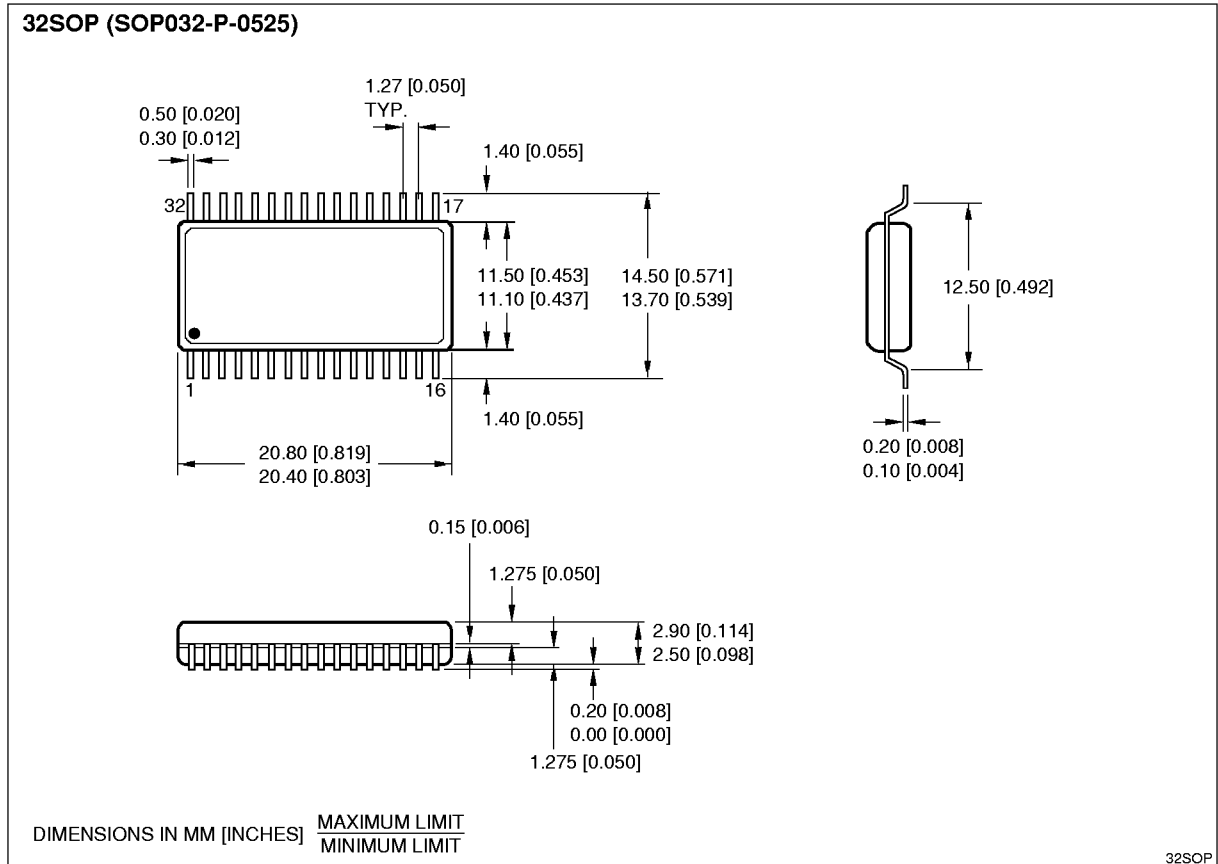
Figure 4. Timing Diagram

tween the V_{CC} pin and the GND pin.

PACKAGE DIAGRAMS

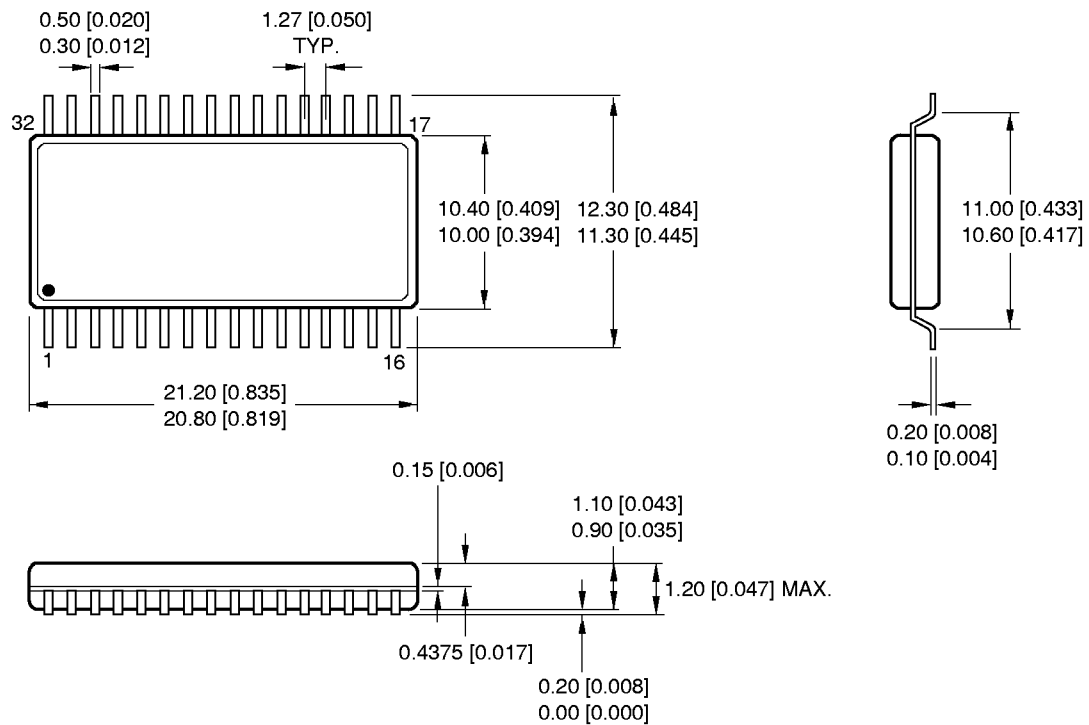


32-pin, 600-mil DIP



32-pin, 525-mil SOP

32TSOP (Type II) (TSOP032-P-0400)



DIMENSIONS IN MM [INCHES]

MAXIMUM LIMIT
MINIMUM LIMIT

32TSOP400

32-pin, 400-mil TSOP (Type II)

ORDERING INFORMATION

LH538300C

Device Type

X

Package

- { D 32-pin, 600-mil DIP (DIP032-P-0600)
- { N 32-pin, 525-mil SOP (SOP032-P-0525)
- { S 32-pin, 400-mil TSOP (Type II) (TSOP032-P-0400)
- { SR 32-pin, 400-mil TSOP (Type II) Reverse bend (TSOP032-P-0400)

CMOS 8M (1M x 8) Mask-Programmable ROM

Example: LH538300CD (CMOS 8M (1M x 8) Mask-Programmable ROM, 32-pin, 600-mil DIP)

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