

CRYSTAL-TO-3.3V LVPECL CLOCK SYNTHESIZER

ICS843S1333

General Description



The ICS843S1333 is a high frequency clock generator and is a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS843S1333 uses an external 20MHz crystal to synthesize 1333.33MHz. The

ICS843S1333 has excellent cycle-to-cycle and RMS period jitter performance.

The ICS843S1333 operates at 3.3V operating supply and is available in a fully RoHS compliant 8-lead TSSOP package.

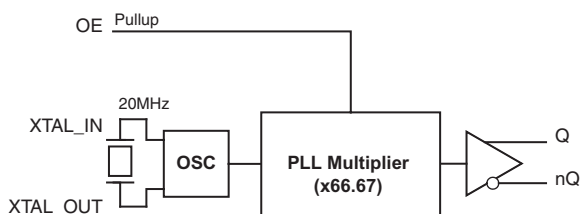
Features

- One differential LVPECL output
- Crystal oscillator interface designed for 18pF, 20MHz parallel resonant crystal
- Cycle-to-Cycle Jitter: 20ps (typical)
- Period Jitter, RMS: TBDps (typical)
- Output Duty Cycle: 48 - 52% (design target)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

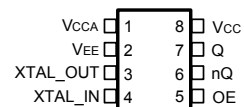
Table 1. Frequency Table

Crystal Frequency (MHz)	Multiplication Value	Output Frequency (MHz)
20	66.67	1333.33

Block Diagram



Pin Assignment



ICS843S1333

8 Lead TSSOP

4.40mm x 3.0mm x 0.925mm package body

G Package

Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 2. Pin Descriptions

Number	Name	Type		Description
1	V _{CCA}	Unused		Analog supply pin.
2	V _{EE}	Power		Negative supply pin.
3, 4	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	OE	Input	Pullup	Active high output enable. When logic HIGH, the outputs are enabled and active. When logic LOW, the outputs are disabled and the device is in the power down mode. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential output pair. LVPECL interface levels.
8	V _{CC}	Power		Power supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 3. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to $V_{CC} + 0.5V$
Outputs, I_O Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, θ_{JA}	115.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		$V_{CC} - 0.10$	3.3	3.465	V
I_{EE}	Power Supply Current			75		mA
I_{CCA}	Analog Supply Current			10		mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{CC} = V_{IN} = 3.465$			5	μA
I_{IL}	Input Low Current	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			μA

Table 4C. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	μA
V_{OL}	Output Low Current; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	μA
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to $V_{CC} - 2V$.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			20		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				TBD	mW

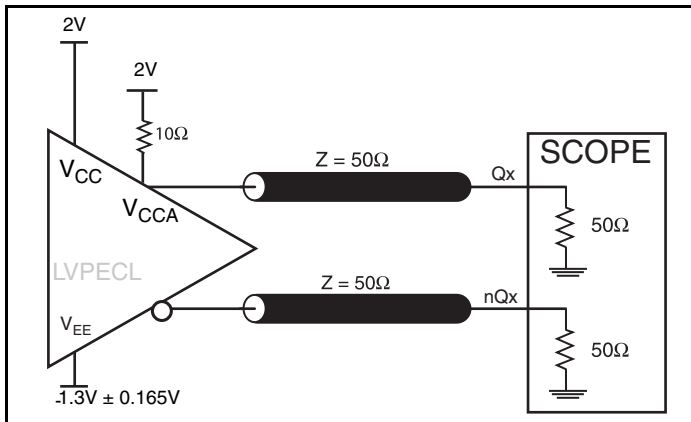
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

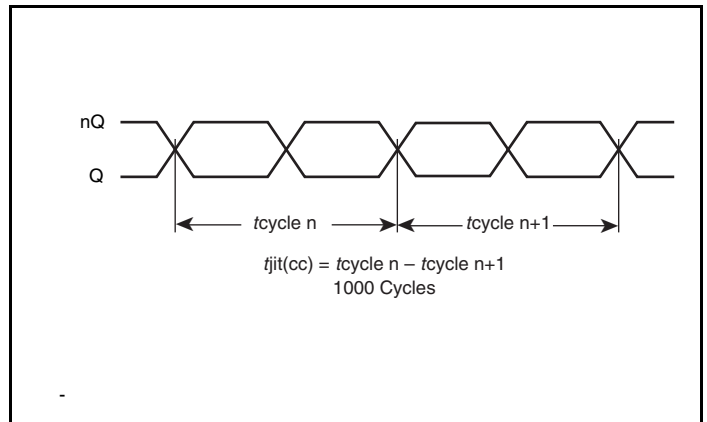
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			1333.33		MHz
$f_{jit(cc)}$	Cycle-to-Cycle Jitter			20		ps
$f_{jit(per)}$	Period Jitter, RMS			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		200		ps
odc	Output Duty Cycle			50		%

NOTE 1: Please refer to Phase Noise Plot.

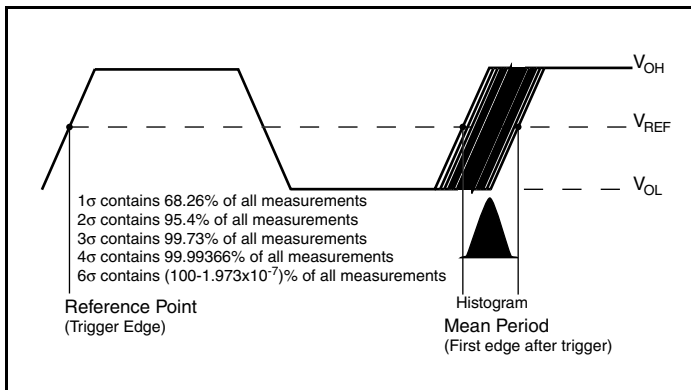
Parameter Measurement Information



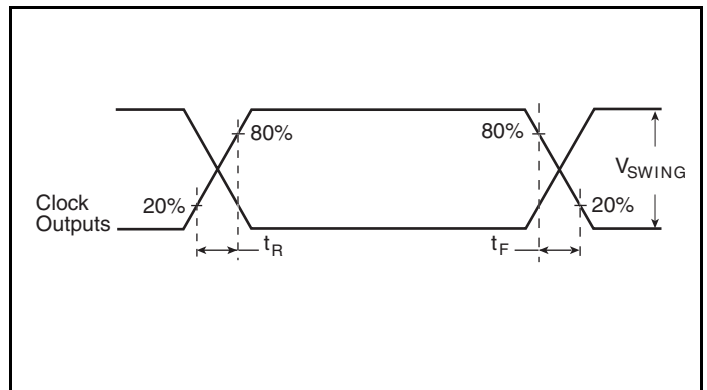
3.3V LVPECL Output Load AC Test Circuit



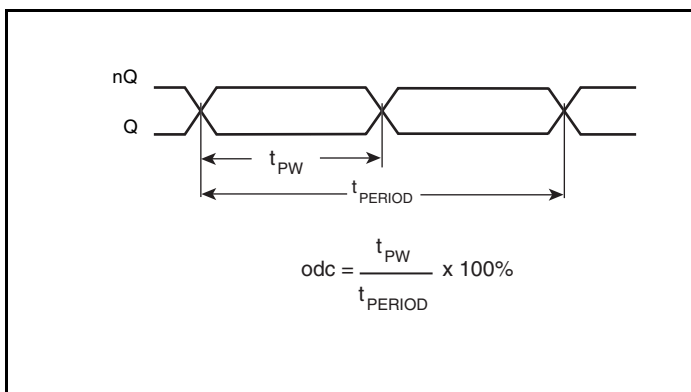
Cycle-to-Cycle Jitter



Period Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843S1333 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{CCA} pin.

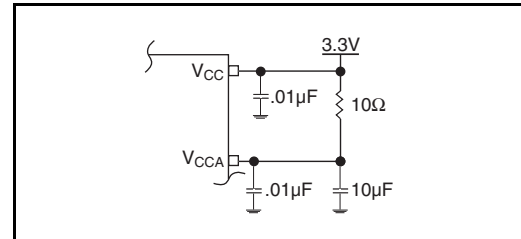


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS843S1333 has been characterized with 18pF parallel resonant crystals. The capacitor values, $C1$ and $C2$, shown in *Figure 2* below were determined using a 20MHz , 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum $C1$ and $C2$ values can be slightly adjusted for different board layouts.

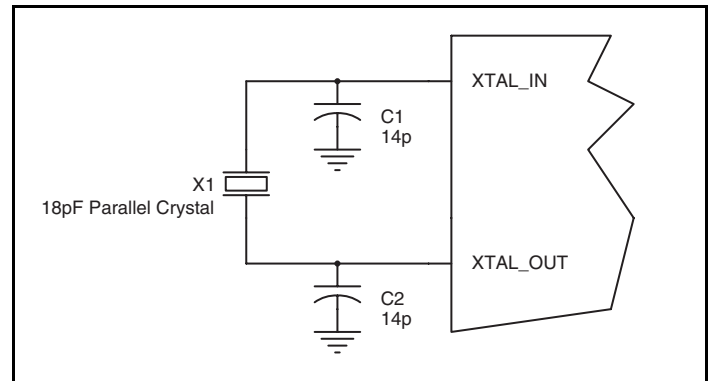


Figure 2. Crystal Input Interface

LVC MOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and making R_2 50Ω.

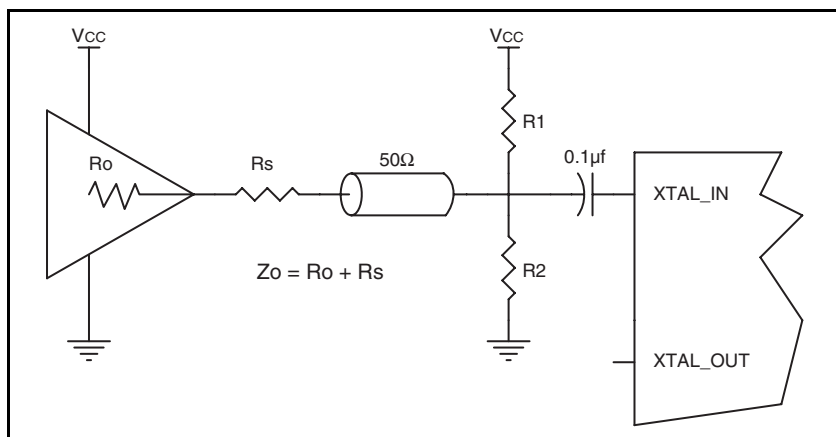


Figure 3. General Diagram for LVC MOS Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

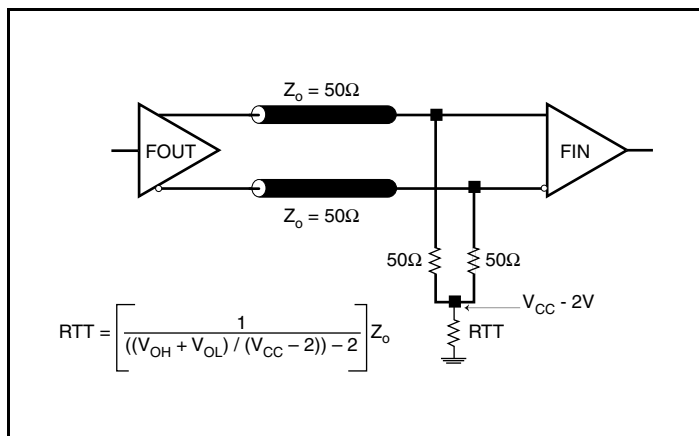


Figure 4A. 3.3V LVPECL Output Termination

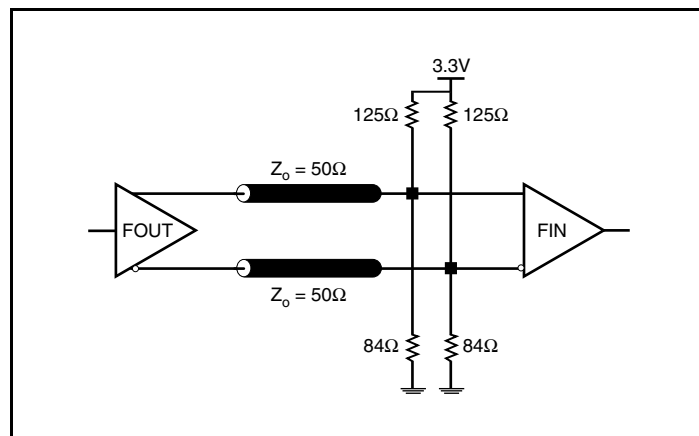


Figure 4B. 3.3V LVPECL Output Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843S1333. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843S1333 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 75mA = 259.875mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**

Total Power_{MAX} (3.3V, with all outputs switching) = $259.875mW + 30mW = 289.875mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 115.2°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$70^\circ C + 0.290W * 115.2^\circ C/W = 103.4^\circ C$. This is well below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

Meters per Second	θ_{JA} by Velocity		
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	115.2°C/W	110.9	108.8

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5*.

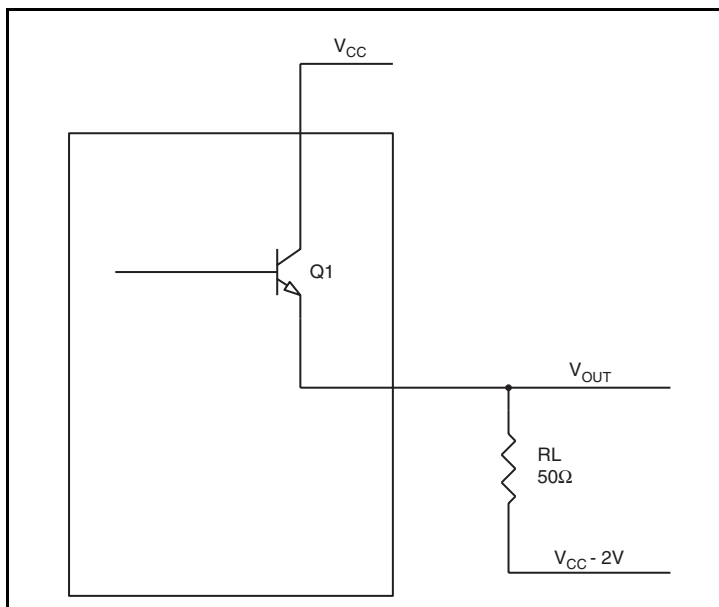


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$
 $(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$
 $(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{30mW}$$

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	115.2°C/W	110.9	108.8

Transistor Count

The transistor count for ICS843S1333 is: 1023

Package Outline and Package Dimension

Package Outline - G Suffix for 8 Lead TSSOP

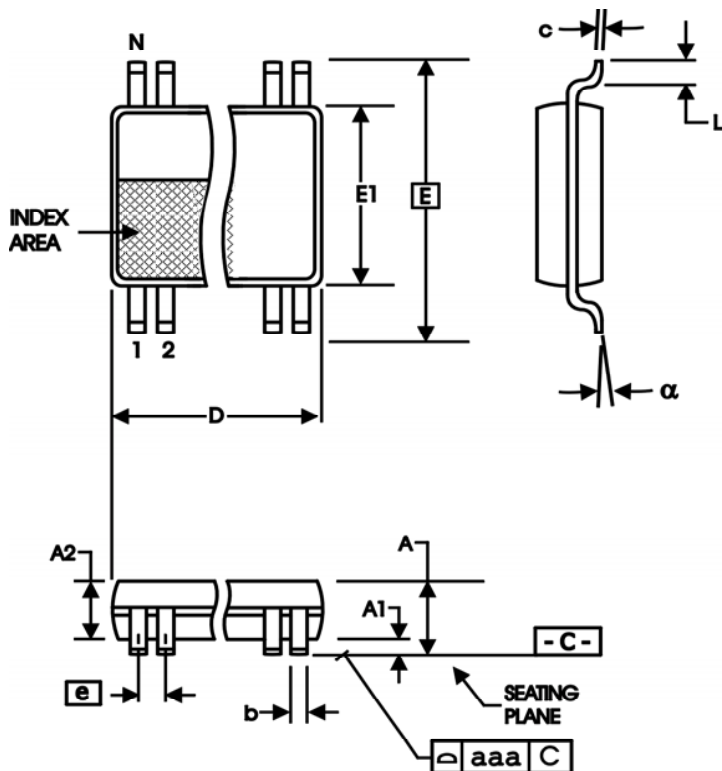


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843S1333CGLF	33CL	"Lead-Free" 8 Lead TSSOP	Tube	0°C to 70°C
ICS843S1333CGLFT	33CL	"Lead-Free" 8 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications, such as those requiring extended temperature ranges, high reliability or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

netcom@idt.com
480-763-2056

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan

Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe

IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

