16-BIT SYNCHRONOUS 2:1 MUX/DEMUX SWITCH

IDT74FST163232

FEATURES:

- **Bus switches provide zero delay paths**
- **Low switch on-resistance**
- **TTL-compatible input and output levels**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Hot insertion capability**
- **Very low power dissipation**
- **Available in SSOP and TSSOP packages**

DESCRIPTION:

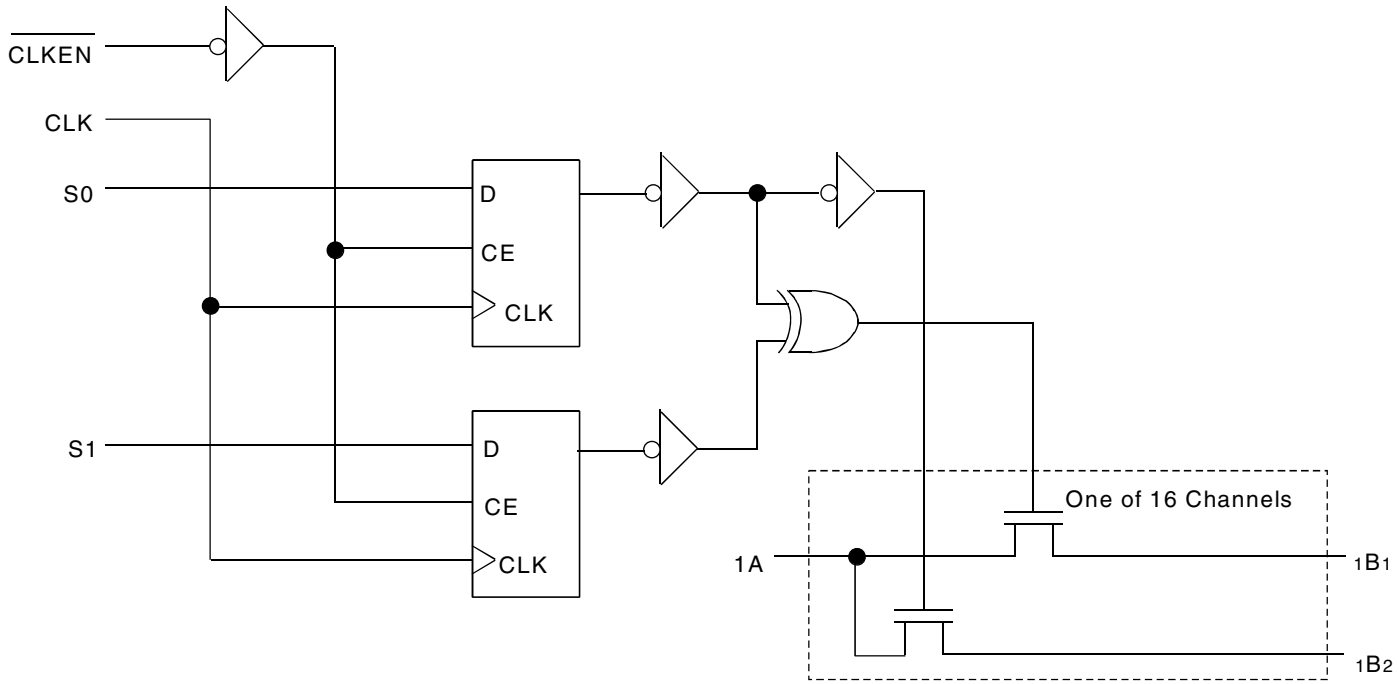
The FST163232 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no V_{CC} applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

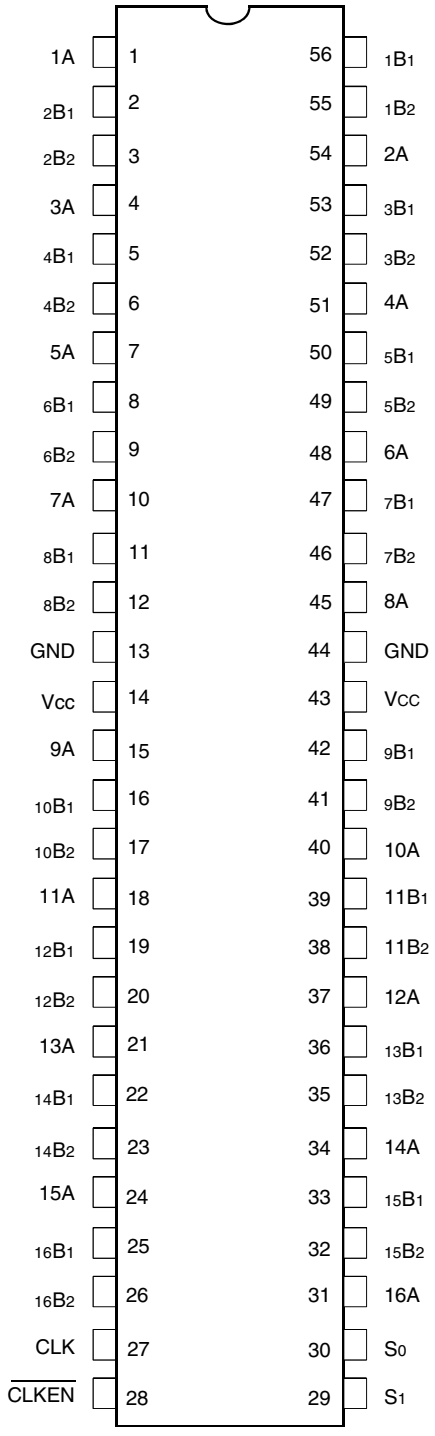
The FST163232 provides three 16-bit TTL- compatible ports that support 2:1 multiplexing. The $S_{0,1}$ pins control mux select and switch enable/disable. The $S_{0,1}$ inputs are synchronous and clocked on the rising edge of CLK when $\overline{CLKEN}$ is low.

Port A can be connected to port B1 or port B2 or both ports B1 and B2.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Maximum Continuous Channel Current	128	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc, Control, and Switch terminals.

CAPACITANCE(1)

Symbol	Parameter		Conditions(2)	Typ.	Unit
C_{IN}	Control Input Capacitance			6	pF
$C_{I/O}$	Switch Input/Output Capacitance	A Port	Switch Off	17	pF
		B Port	Switch Off	12	

NOTES:
1. Capacitance is characterized but not tested.
2. T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V.

PIN DESCRIPTION

Pin Names	I/O	Description
A_1	I/O	Bus A_1
B_1, B_2	I/O	Buses B_1, B_2
$S_{0,1}$	I	Control Pins
CLK	I	Clock Input. Clocks $S_{0,1}$ on Rising Edge.
$\overline{CLKEN}$	I	Clock Enable Input

FUNCTION TABLE(1)

S_1	S_0	CLK	$\overline{CLKEN}$	Description
X	X	X	H	Last State
L	L	↑	L	Disconnect
L	H	↑	L	A to B_1 and A to B_2
H	L	↑	L	A to B_1 or B_1 to A
H	H	↑	L	A to B_2 or B_2 to A

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Control Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2	—	—	V
V_{IL}	Control Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Control Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Control Input LOW Current		V_I = GND	—	—	±1	
I_{OZH}	Current During	V_{CC} = Max., V_O = 0 to 5V		—	—	±1	µA
I_{OZL}	Bus Switch Disconnect			—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OFF}	Switch Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 5.5V		—	—	±1	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.1	3	µA

BUS SWITCH IMPEDANCE OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Unit
R_{ON}	Switch On Resistance[2]	Vcc = Min., V_{IN} = 0V, I_{ON} = 64mA	—	4	7	Ω
		Vcc = Min., V_{IN} = 0V, I_{ON} = 30mA	—	4	7	
		Vcc = Min., V_{IN} = 2.4V, I_{ON} = 15mA	—	6	15	
I_{OS}	Short Circuit Current, A to B[3]	A(B) = 0V, B(A) = Vcc	100	—	—	mA

NOTES:
1. Typical values are at Vcc = 5.0V, +25°C ambient.
2. The voltage drop between the indicated ports divided by the current through the switch.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4,5]	V_{CC} = Max. Clock Pin Toggling 50% Duty Cycle 16 Switches Toggling One Select Toggling at 50% of CLK Frequency	V_{IN} = V_{CC} V_{IN} = GND				µA/ MHz/
I_{CCD}	Dynamic Power Supply Current[4,5]	V_{CC} = Max. Clock Pin Toggling 50% Duty Cycle 32 Switches Toggling Two Select Pins Toggling at 50% of CLK Frequency	V_{IN} = V_{CC} V_{IN} = GND				µA/ MHz/
I_C	Total Power Supply Current[6]	V_{CC} = Max. f_{CP} = 10MHz (CLK) 50% Duty Cycle $\overline{CLKEN}$ = LOW S_0 = HIGH or LOW f_i = 2.5MHz (S_1) 16 Switches Toggling	V_{IN} = V_{CC} V_{IN} = GND				mA
			V_{IN} = V_{CC} V_{IN} = 3.4V				
		V_{CC} = Max. f_{CP} = 10MHz (CLK) 50% Duty Cycle $\overline{CLKEN}$ = LOW S_1 = HIGH f_i = 2.5MHz (S_0) 16 MUXes Exchanging	V_{IN} = V_{CC} V_{IN} = GND				
			V_{IN} = V_{CC} V_{IN} = 3.4V				
		V_{CC} = Max. f_{CP} = 10MHz (CLK) 50% Duty Cycle $\overline{CLKEN}$ = LOW S_1 = LOW f_i = 2.5MHz (S_0) 32 Switches Toggling	V_{IN} = V_{CC} V_{IN} = GND				
			V_{IN} = V_{CC} V_{IN} = 3.4V				

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type. T_A = –40°C to +85°C
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND. Switch inputs do not contribute to ΔI_{CC}.
4. This parameter represents the current required to switch the internal capacitance of the control inputs at the specified frequency.
   Switch inputs generate no significant power supply currents as they transition. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. C_{PD} = I_{CCD}/V_{CC}
   C_{PD} = Power Dissipation Capacitance
6. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} ($f_i N$)
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Control Input Frequency
   N = Number of Control Inputs Toggling at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

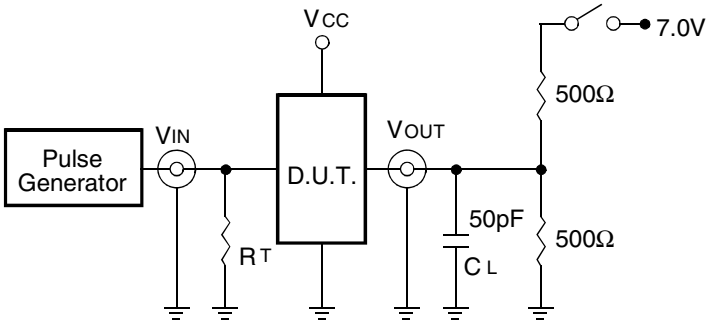
Industrial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%

Symbol	Description[1]	V_{CC} = 5V ± 10%			V_{CC} = 4V		Unit
		Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Data Propagation Delay A to B, B to A[2]	—	—	0.25	—	0.25	ns
t_{PZH} t_{PZL}	Switch CONNECT Delay CLK↑ to A-B_1 or A-B_2	1.5	—	5.8	—	6.1	ns
t_{PZH} t_{PZL}	Switch CONNECT Delay CLK↑ to B_1-B_2	1.5	—	7.9	—	8.5	ns
t_{PHZ} t_{PLZ}	Switch DISCONNECT Delay CLK↑ to A, B	1.9	—	6.2	—	5.8	ns
t_{BX}	Switch EXCHANGE Delay CLK↑ from A-B_1(B_2) to A-B_2(B_1)	1.8	—	6.2	—	6.8	ns
t_{SU}	Clock Enable Set-Up Time $\overline{CLKEN}$ to CLK↑	1.9	—	—	2.2	—	ns
t_H	Clock Enable Hold Time $\overline{CLKEN}$ after CLK↑	1	—	—	1.9	—	ns
t_{SU}	Select Set-Up Time S_0, S_1 to CLK↑	1.9	—	—	2.2	—	ns
t_H	Select Hold Time S_0, S_1 after CLK↑	1	—	—	0.5	—	ns
$\|Q_{CI}\|$	Charge Injection During Switch DISCONNECT CLK↑ to A, B[3]	—	1.5	—	—	—	pC
$\|Q_{DCI}\|$	Charge Injection During Switch Exchange CLK↑ to A, B[3]	—	0.5	—	—	—	pC

NOTES:

1. See test circuits and waveforms.
2. The bus switch contributes no Propagation Delay other than the RC Delay of the load interacting with the RC of the switch.
3. $|Q_{CI}|$ is the charge injection for a single switch DISCONNECT and applies to either single switches or multiplexers. $|Q_{DCI}|$ is the charge injection for a multiplexer as the multiplexed port switches from one path to another. Charge injection is reduced because the injection from the DISCONNECT of the first path is compensated by the CONNECT of the second path.

TEST CIRCUITS AND WAVEFORMS



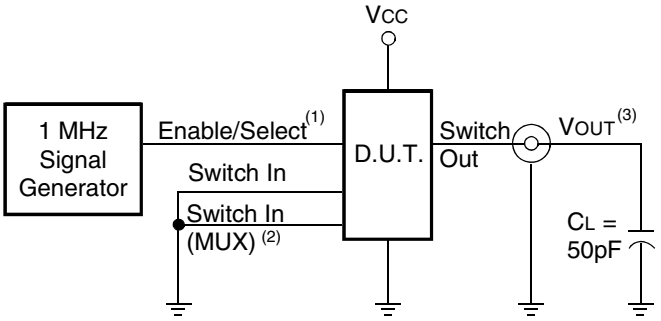
Test Circuits for All Outputs

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

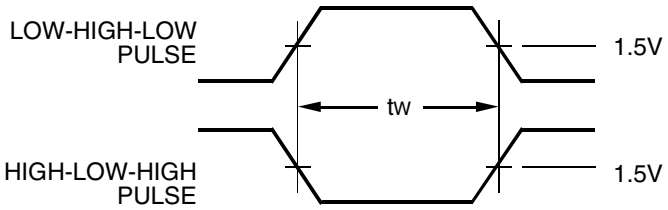
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



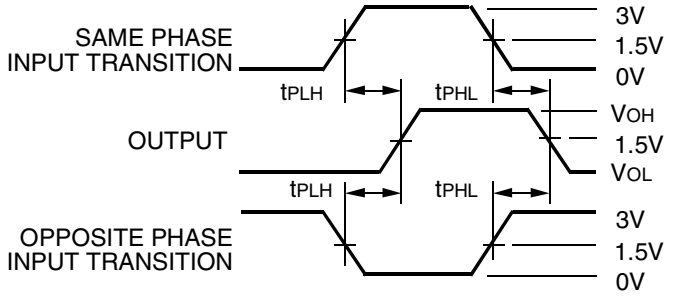
Charge Injection

NOTES:

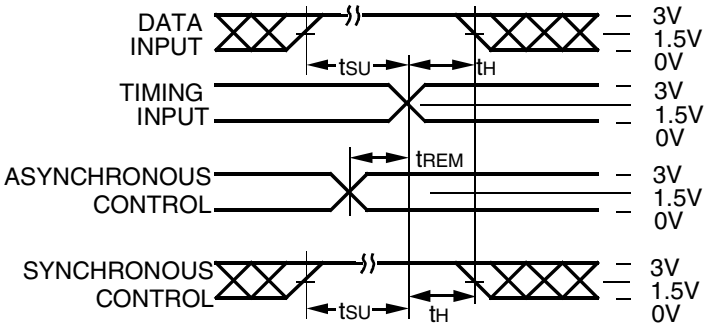
1. Select is used with multiplexers for measuring I_{QDCI} during multiplexer select. During all other tests Enable is used.
2. Used with multiplexers to measure I_{QDCI} only.
3. Charge Injection = $\Delta V_{OUT} C_L$, with Enable toggling for I_{QCI} or Select toggling for I_{QDCI}. ΔV_{OUT} is the change in V_{OUT} and is measured with a 10MΩ probe.



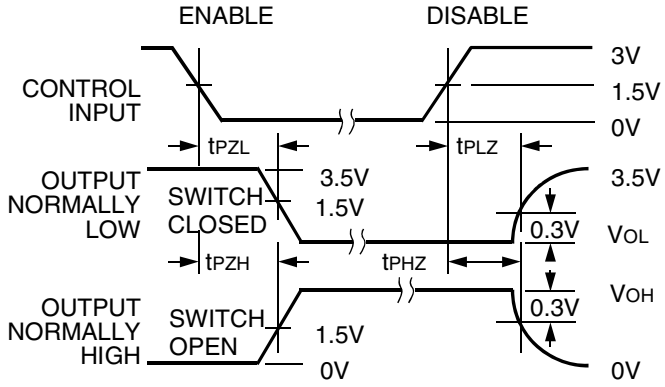
Pulse Width



Propagation Delay



Set-up, Hold, and Release Times

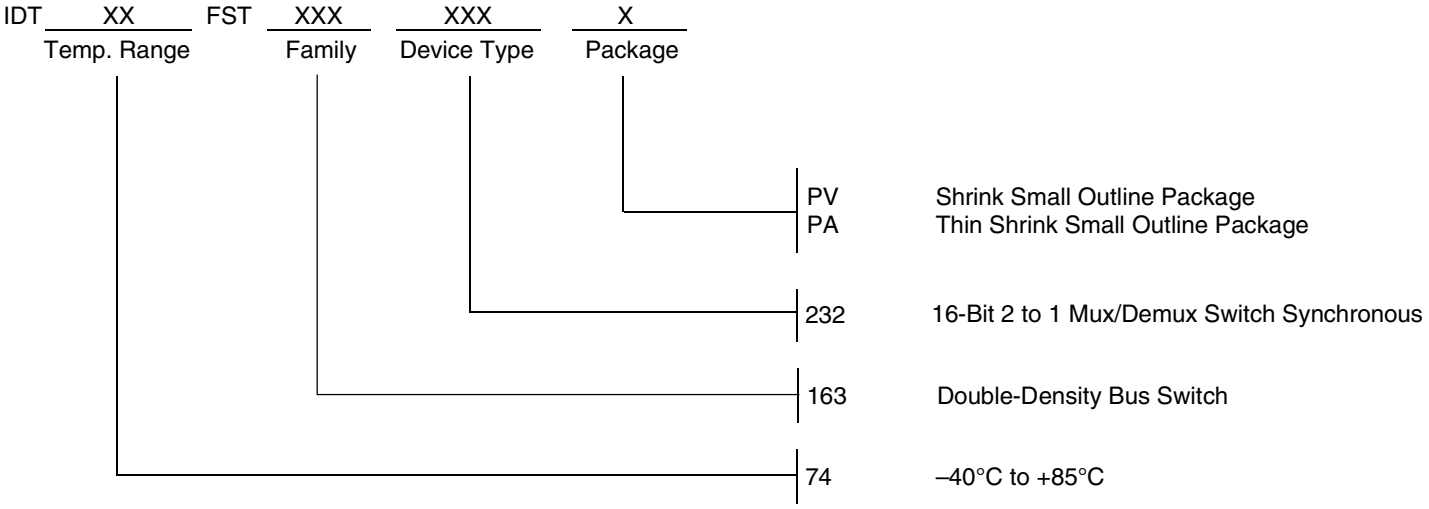


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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