Document Title

64Kx36/x32 & 128Kx18-Bit Synchronous Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial draft	Jan. 17. 2002	Preliminary

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2Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
128Kx18	K7B201825B-QC(I)65/75/80	SB	3.3	6.5/7.5/8.0 ns	Q (100TQFP)	C (Commercial Temperature Range) I: (Industrial Temperature
	K7A201800B-QC(I)25/22/20/16/14	SPB(2E1D)	3.3	250/225/200/167/138 MHz		
64Kx32	K7B203225B-QC(I)65/75/80	SB	3.3	6.5/7.5/8.0 ns		
	K7A203200B-QC(I)25/22/20/16/14	SPB(2E1D)	3.3	250/225/200/167/138 MHz		
64Kx36	K7B203625B-QC(I)65/75/80	SB	3.3	6.5/7.5/8.0 ns		
	K7A203600B-QC(I)25/22/20/16/14	SPB(2E1D)	3.3	250/225/200/167/138 MHz		

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K7B203625B
K7B203225B
K7B201825B

64Kx36/x32 & 128Kx18 Synchronous SRAM

64Kx36/x32 & 128Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- V_{DD}= 3.3V+0.3V/-0.165V Power Supply.
- V_{DDQ} Supply Voltage 3.3V+0.3V/-0.165V for 3.3V I/O
  or 2.5V+0.4V/-0.125V for 2.5V I/O.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, ADSC, ADV Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- TTL-Level Three-State Output.
- 100-TQFP-1420A
- Operating in commeical and industrial temperature range.

FAST ACCESS TIMES

PARAMETER	Symbol	-65	-75	-80	Unit
Cycle Time	t_{CYC}	7.5	8.5	10	ns
Clock Access Time	t_{CD}	6.5	7.5	8.0	ns
Output Enable Access Time	t_{OE}	3.5	3.5	4.0	ns

GENERAL DESCRIPTION

The K7B203625B, K7B203225B and K7B201825B are 2,359,296 bits Synchronous Static Random Access Memory designed to support zero wait state performance for advanced Pentium/Power PC based system. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signals.

It can be organized as 64K(128K) words of 36(32/18) bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.
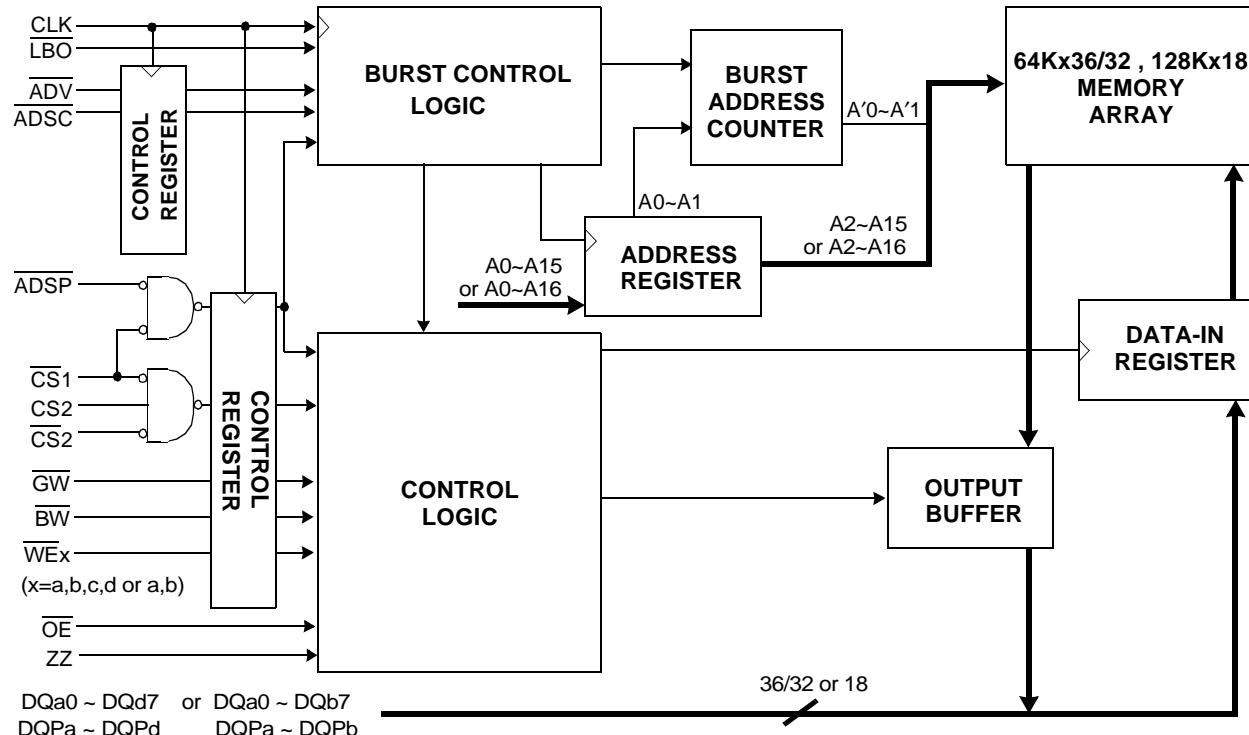
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B203625B, K7B203225B and K7B201825B are implemented with SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.
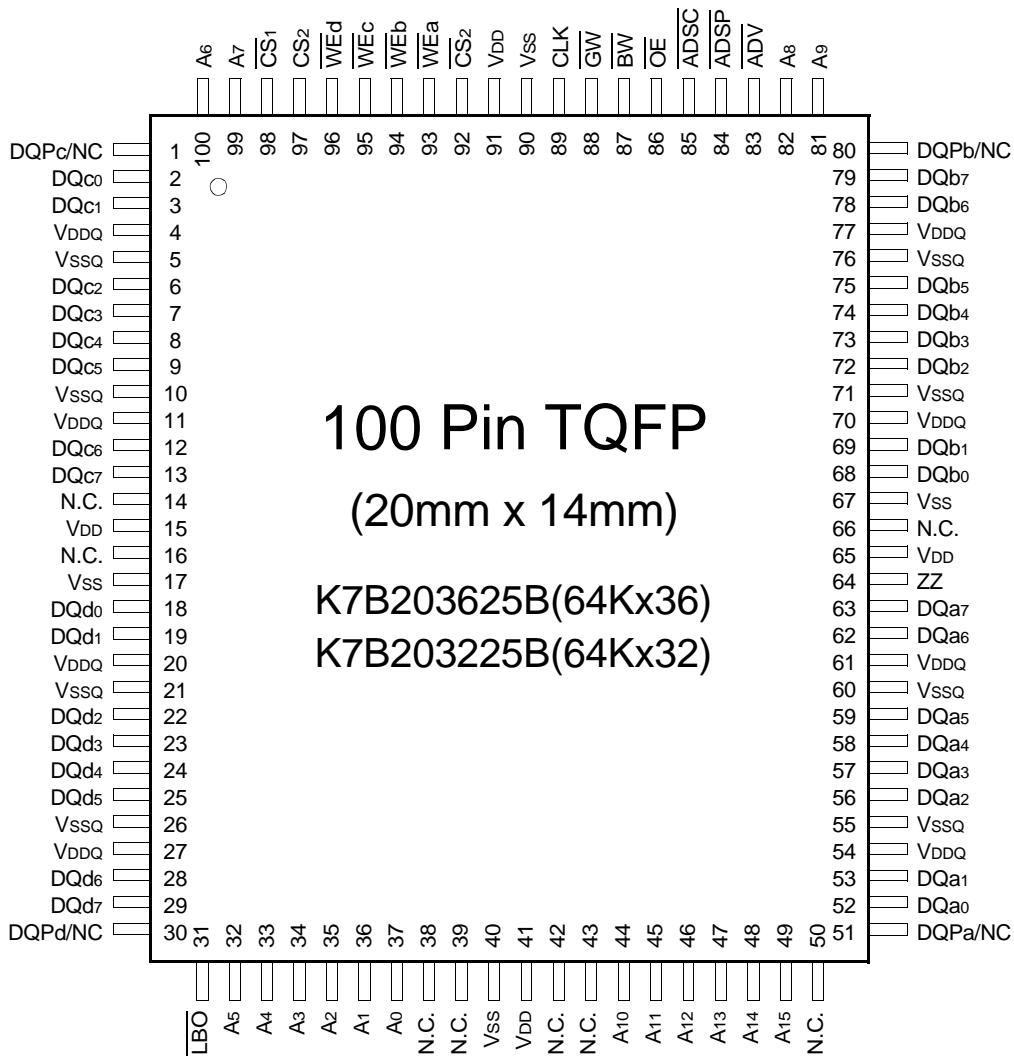
LOGIC BLOCK DIAGRAM

Jan 2002
Rev 0.0

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K7B203625B
K7B203225B
K7B201825B
64Kx36/x32 & 128Kx18 Synchronous SRAM

PIN CONFIGURATION(TOP VIEW)

Top pins (left to right): A6, A7, CS1, CS2, WEd, WEc, WEb, WEa, CS2, VDD, VSS, CLK, GW, BW, OE, ADSC, ADSP, ADV, A8, A9

Left side (pins 1-30):
- 1 DQPc/NC
- 2 DQc0
- 3 DQc1
- 4 VDDQ
- 5 VSSQ
- 6 DQc2
- 7 DQc3
- 8 DQc4
- 9 DQc5
- 10 VSSQ
- 11 VDDQ
- 12 DQc6
- 13 DQc7
- 14 N.C.
- 15 VDD
- 16 N.C.
- 17 VSS
- 18 DQd0
- 19 DQd1
- 20 VDDQ
- 21 VSSQ
- 22 DQd2
- 23 DQd3
- 24 DQd4
- 25 DQd5
- 26 VSSQ
- 27 VDDQ
- 28 DQd6
- 29 DQd7
- 30 DQPd/NC

Center:
100 Pin TQFP
(20mm x 14mm)
K7B203625B(64Kx36)
K7B203225B(64Kx32)

Right side (pins 51-80):
- 80 DQPb/NC
- 79 DQb7
- 78 DQb6
- 77 VDDQ
- 76 VSSQ
- 75 DQb5
- 74 DQb4
- 73 DQb3
- 72 DQb2
- 71 VSSQ
- 70 VDDQ
- 69 DQb1
- 68 DQb0
- 67 VSS
- 66 N.C.
- 65 VDD
- 64 ZZ
- 63 DQa7
- 62 DQa6
- 61 VDDQ
- 60 VSSQ
- 59 DQa5
- 58 DQa4
- 57 DQa3
- 56 DQa2
- 55 VSSQ
- 54 VDDQ
- 53 DQa1
- 52 DQa0
- 51 DQPa/NC

Bottom pins (pins 31-50): LBO, A5, A4, A3, A2, A1, A0, N.C., N.C., VSS, VDD, N.C., N.C., A10, A11, A12, A13, A14, A15, N.C.

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37 44,45,46,47,48,49 81,82,99,100	VDD VSS	Power Supply(+3.3V) Ground	15,41,65,91 17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,42,43,50,66
ADSP	Address Status Processor	84			
ADSC	Address Status Controller	85	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb0~b7		68,69,72,73,74,75,78,79
CS1	Chip Select	98	DQc0~c7		2,3,6,7,8,9,12,13
CS2	Chip Select	97	DQd0~d7		18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd /NC		51,80,1,30
WEx (x=a,b,c,d)	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
GW	Global Write Enable	88			
BW	Byte Write Enable	87	VSSQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

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PIN CONFIGURATION(TOP VIEW)

100 Pin TQFP
(20mm x 14mm)
K7B201825B(128Kx18)

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{16}	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,49, 80,81,82,99,100	V_{DD} V_{SS} N.C.	Power Supply(+3.3V) Ground No Connect	15,41,65,91 17,40,67,90 1,2,3,6,7,14,16,25,28,29,
$\overline{ADV}$	Burst Address Advance	83			30,38,39,42,43,50,51,52,
$\overline{ADSP}$	Address Status Processor	84			53,56,57,66,75,78,79,95,
ADSC	Address Status Controller	85			96
CLK	Clock	89			
$\overline{CS_1}$	Chip Select	98	DQa_0~a_7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
$\overline{CS_2}$	Chip Select	97	DQb_0~b_7		8,9,12,13,18,19,22,23
CS_2	Chip Select	92	DQPa, Pb		74,24
$\overline{WEx}$	Byte Write Inputs	93,94			
(x=a,b)			V_{DDQ}	Output Power Supply	4,11,20,27,54,61,70,77
$\overline{OE}$	Output Enable	86		(2.5V or 3.3V)	
$\overline{GW}$	Global Write Enable	88	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
LBO	Burst Mode Control	31			

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FUNCTION DESCRIPTION

The K7B2036/3225B and K7B201825B are synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSC, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$, and $\overline{WEd}$ are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(independent of $\overline{BW}$ and $\overline{WEx}$.), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In K7B203625B, a 64Kx36 organization, $\overline{WEa}$ controls DQa0 ~ DQa7 and DQPa, $\overline{WEb}$ controls DQb0 ~ DQb7 and DQPb, $\overline{WEc}$ controls DQc0 ~ DQc7 and DQPc and $\overline{WEd}$ controls DQd0 ~ DQd7 and DQPd.

$\overline{CS}_1$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE
(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

Note : 1. $\overline{LBO}$ pin must be tied to high or low, and floating state must not be allowed.

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to high or low, and floating state must not be allowed.

ASYNCHRONOUS TRUTH TABLE
(See Notes 1 and 2):

OPERATION	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes
1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffersmust be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

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TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS$_2$	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care".   2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.

   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36/32)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Voltage on V$_{DD}$ Supply Relative to V$_{SS}$		V$_{DD}$	-0.3 to 4.6	V
Voltage on V$_{DDQ}$ Supply Relative to V$_{SS}$		V$_{DDQ}$	V$_{DD}$	V
Voltage on Input Pin Relative to V$_{SS}$		V$_{IN}$	-0.3 to V$_{DD}$+0.3	V
Voltage on I/O Pin Relative to V$_{SS}$		V$_{IO}$	-0.3 to V$_{DDQ}$+0.3	V
Power Dissipation		P$_D$	1.4	W
Storage Temperature		T$_{STG}$	-65 to 150	°C
Operating Temperature	Commercial	T$_{OPR}$	0 to 70	°C
	Industrial	T$_{OPR}$	-40 to 85	°C
Storage Temperature Range Under Bias		T$_{BIAS}$	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C≤ T$_A$≤70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V$_{DD}$	3.135	3.3	3.6	V
	V$_{DDQ}$	3.135	3.3	3.6	V
Ground	V$_{SS}$	0	0	0	V

* The above parameters are also guaranteed at industrial temperature range.

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ T$_A$ ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V$_{DD}$	3.135	3.3	3.6	V
	V$_{DDQ}$	2.375	2.5	2.9	V
Ground	V$_{SS}$	0	0	0	V

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T$_A$=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C$_{IN}$	V$_{IN}$=0V	-	4	pF
Output Capacitance	C$_{OUT}$	V$_{OUT}$=0V	-	6	pF

*Note : Sampled not 100% tested.

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DC ELECTRICAL CHARACTERISTICS(T_A=0 to 70°C, V_{DD}=3.3V+0.3V/-0.165V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNI
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max , V_{IN}=V_{SS} to V_{DD}		-2	+2	µA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT}=V_{SS} to V_{DDQ}		-2	+2	µA
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, $ZZ \leq V_{IL}$, All Inputs=V_{IL} or V_{IH} Cycle Time ≥ t_{CYC} min	-65	-	250	mA
			-75	-	230	
			-80	-	210	
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, $ZZ \leq V_{IL}$, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-65	-	130	mA
			-75	-	120	
			-80	-	110	
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	80	mA
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	50	mA
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL} = 1.0mA		-	0.4	V
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH} = -1.0mA		2.0	-	V
Input Low Voltage(3.3V I/O)	V_{IL}			-0.5*	0.8	V
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+03**	V
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.3**	V

 The above parameters are also guaranteed at industrial temperature range.
* V_{IL}(Min)=-2.0(Pulse Width ≤ t_{CYC}/2)
** V_{IH}(Max)=4.6(Pulse Width ≤ t_{CYC}/2)
** In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

TEST CONDITIONS
(V_{DD}=3.3V+0.3V/-0.165V,V_{DDQ}=3.3V+0.3/-0.165V or V_{DD}=3.3V+0.3V/-0.165V,V_{DDQ}=2.5V+0.4V/-0.125V, T_A=0 to 70°C)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	1ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	1ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1
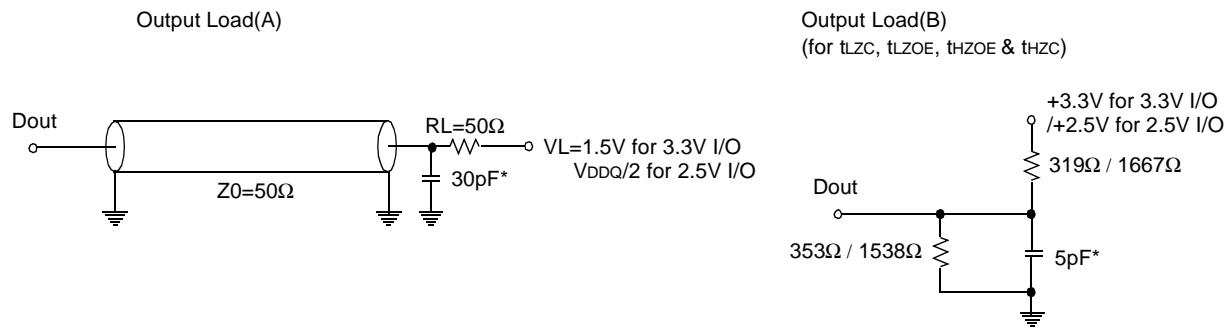
* The above parameters are also guaranteed at industrial temperature range.

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Output Load(A)

Output Load(B)
(for t_{LZC}, t_{LZOE}, t_{HZOE} & t_{HZC})

Dout
RL=50Ω
Z0=50Ω
30pF*
VL=1.5V for 3.3V I/O
V_{DDQ}/2 for 2.5V I/O

+3.3V for 3.3V I/O
/+2.5V for 2.5V I/O
319Ω / 1667Ω
Dout
353Ω / 1538Ω
5pF*

* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS(T_A=0 to 70°C, V_{DD}=3.3V+0.3V/-0.165V)

PARAMETER	Symbol	-65 Min	-65 Max	-75 Min	-75 Max	-80 Min	-80 Max	UNIT
Cycle Time	t_{CYC}	7.5	-	8.5	-	10	-	ns
Clock Access Time	t_{CD}	-	6.5	-	7.5	-	8.0	ns
Output Enable to Data Valid	t_{OE}	-	3.5	-	3.5	-	4.0	ns
Clock High to Output Low-Z	t_{LZC}	0	-	0	-	0	-	ns
Output Hold from Clock High	t_{OH}	2.5	-	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	3.5	-	3.5	-	4.0	ns
Clock High to Output High-Z	t_{HZC}	2	3.5	2	3.5	2	3.5	ns
Clock High Pulse Width	t_{CH}	2.5	-	3	-	4	-	ns
Clock Low Pulse Width	t_{CL}	2.5	-	3	-	4	-	ns
Address Setup to Clock High	t_{AS}	1.5	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	t_{SS}	1.5	-	2.0	-	2.0	-	ns
Data Setup to Clock High	t_{DS}	1.5	-	2.0	-	2.0	-	ns
Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	t_{WS}	1.5	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	t_{ADVS}	1.5	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	t_{CSS}	1.5	-	2.0	-	2.0	-	ns
Address Hold from Clock High	t_{AH}	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t_{SH}	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	t_{WH}	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	2	-	2	-	cycle
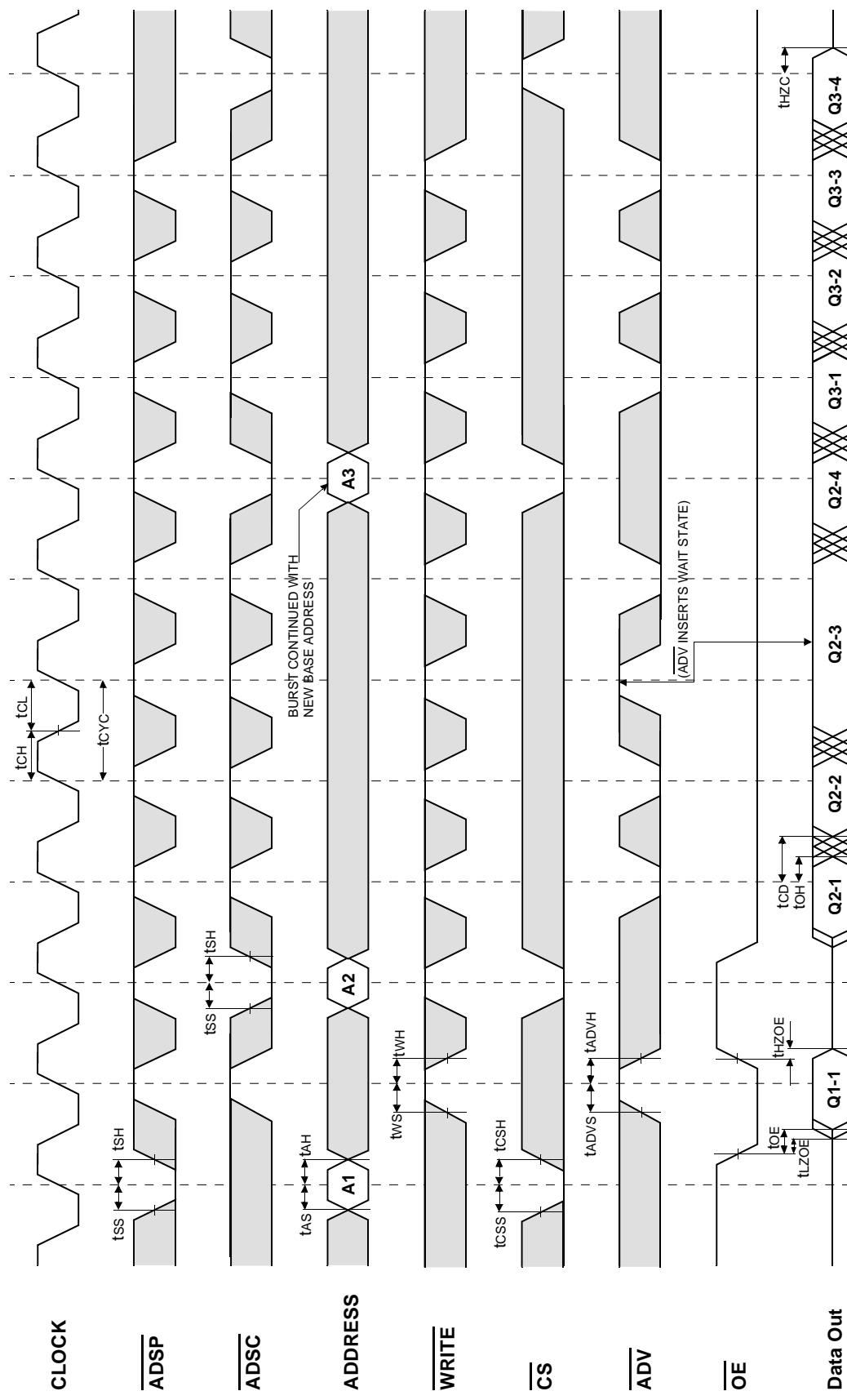
Notes : 1 The above parameters are also guaranteed at industrial temperature range.
2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
4. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.
5. At any given voltage and temperature, t_{HZC} is less than t_{LZC}.

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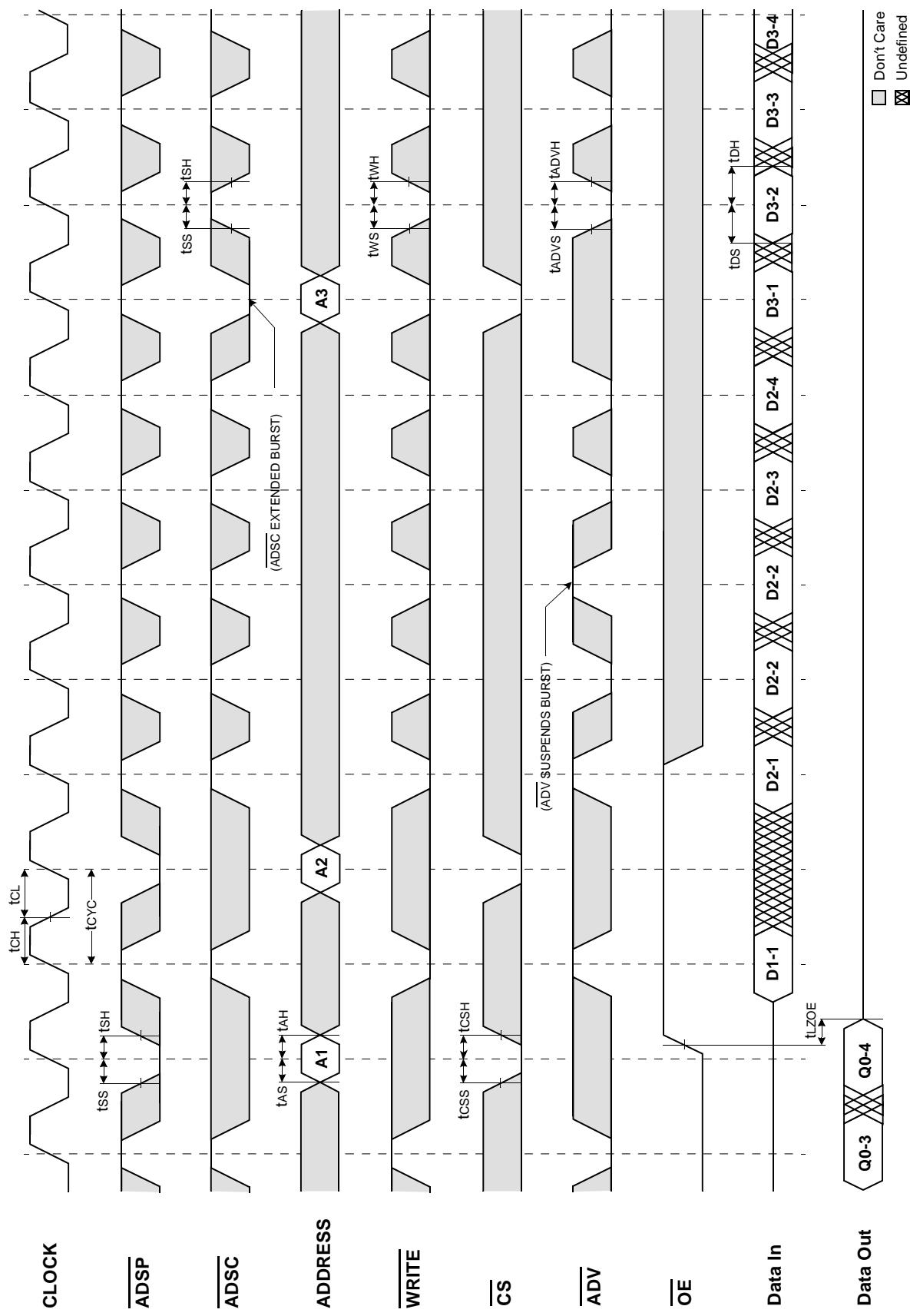
TIMING WAVEFORM OF READ CYCLE
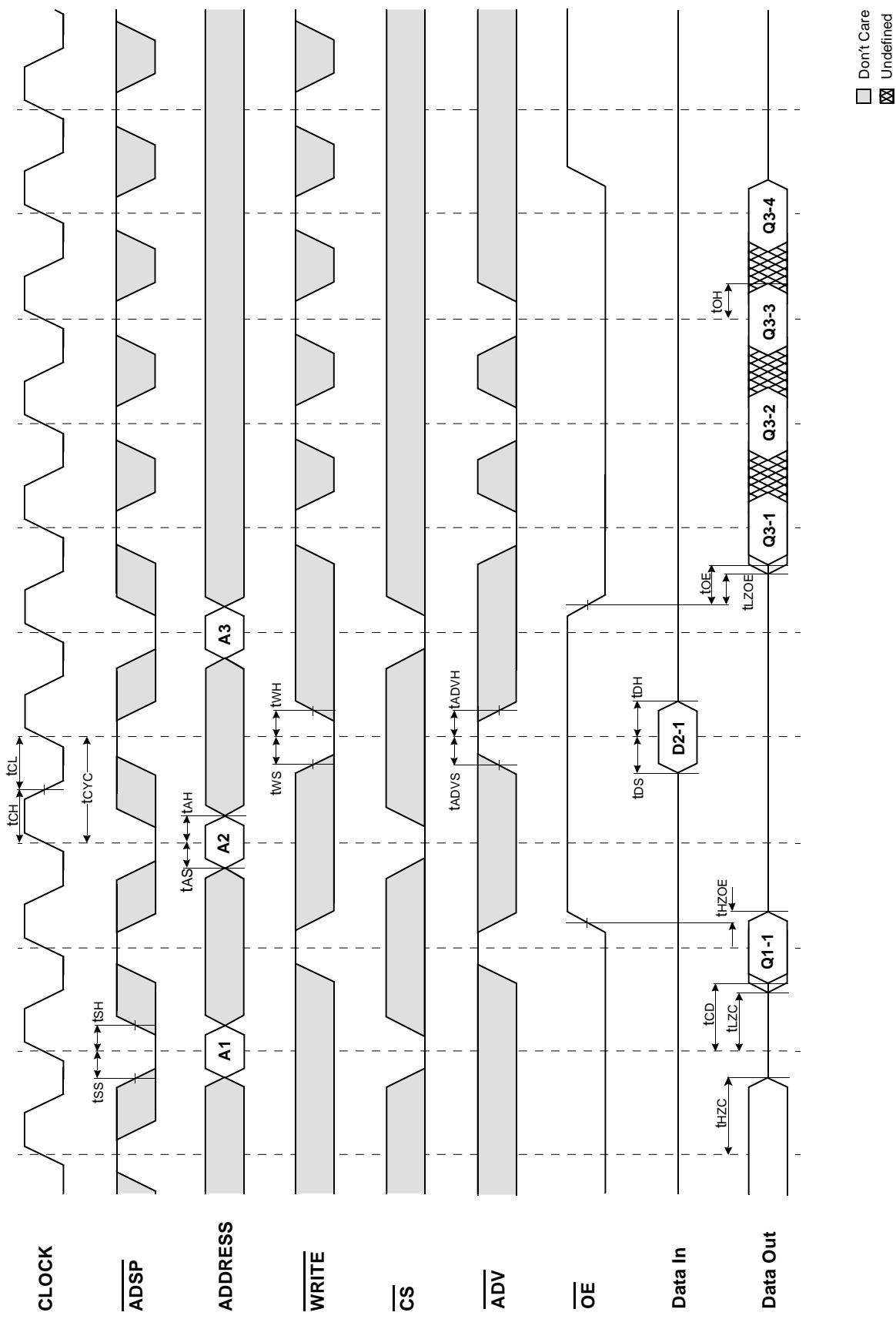
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WEx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

Signals: CLOCK, $\overline{ADSP}$, $\overline{ADSC}$, ADDRESS, $\overline{WRITE}$, $\overline{CS}$, $\overline{ADV}$, $\overline{OE}$, Data Out

□ Don't Care   ⊠ Undefined

TIMING WAVEFORM OF WRTE CYCLE

Signals (left to right along bottom): CLOCK, ADSP, ADSC, ADDRESS, WRITE, CS, ADV, OE, Data In, Data Out

Timing parameters: tCH, tCL, tCYC, tSS, tSH, tAS, tAH, tCSS, tCSH, tWS, tWH, tADVS, tADVH, tDS, tDH, tLZOE

Address: A1, A2, A3

(ADSC EXTENDED BURST)
(ADV SUSPENDS BURST)

Data In: D1-1, D2-1, D2-2, D2-2, D2-3, D2-4, D3-1, D3-2, D3-3, D3-4

Data Out: Q0-3, Q0-4

Legend: Don't Care, Undefined
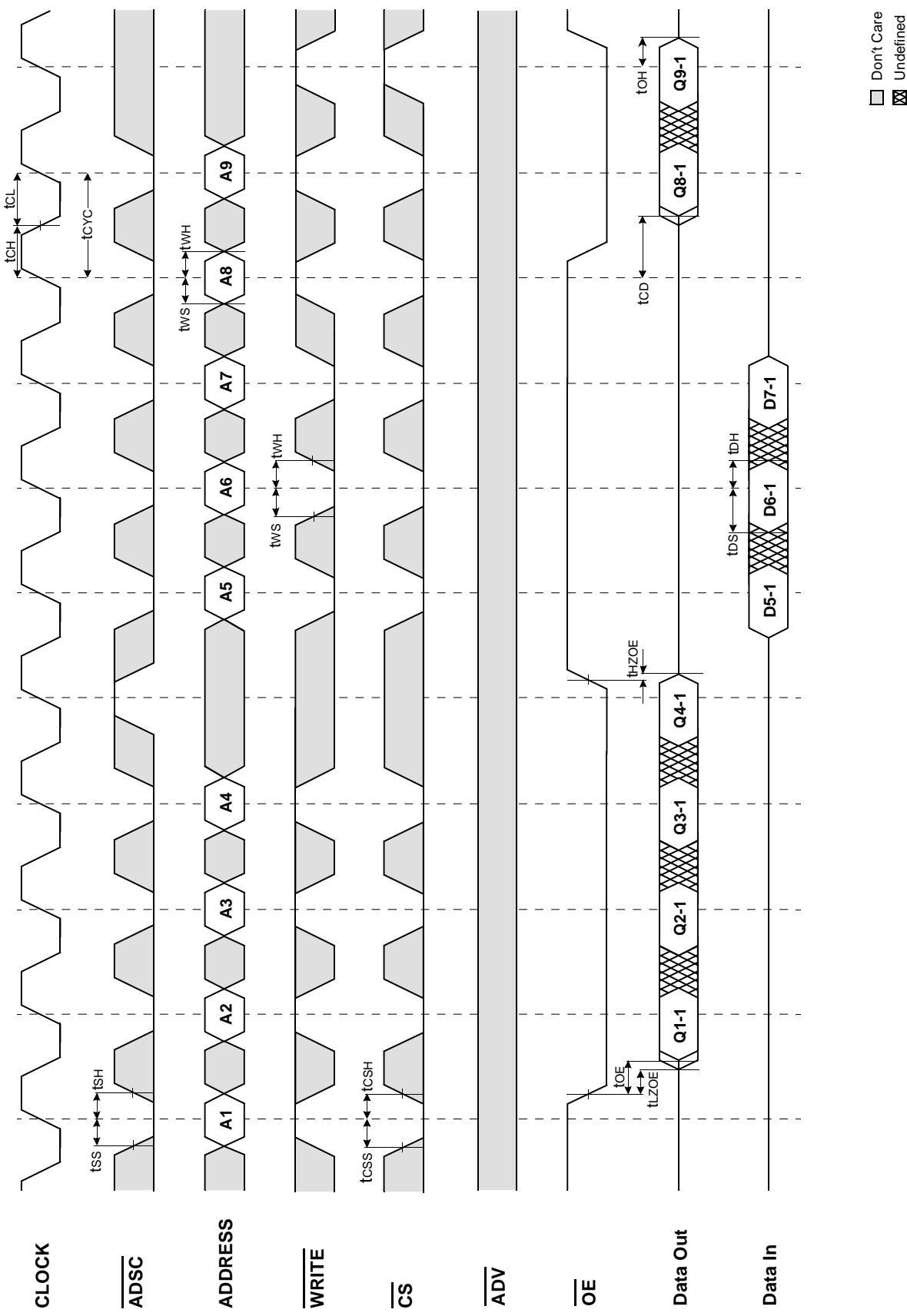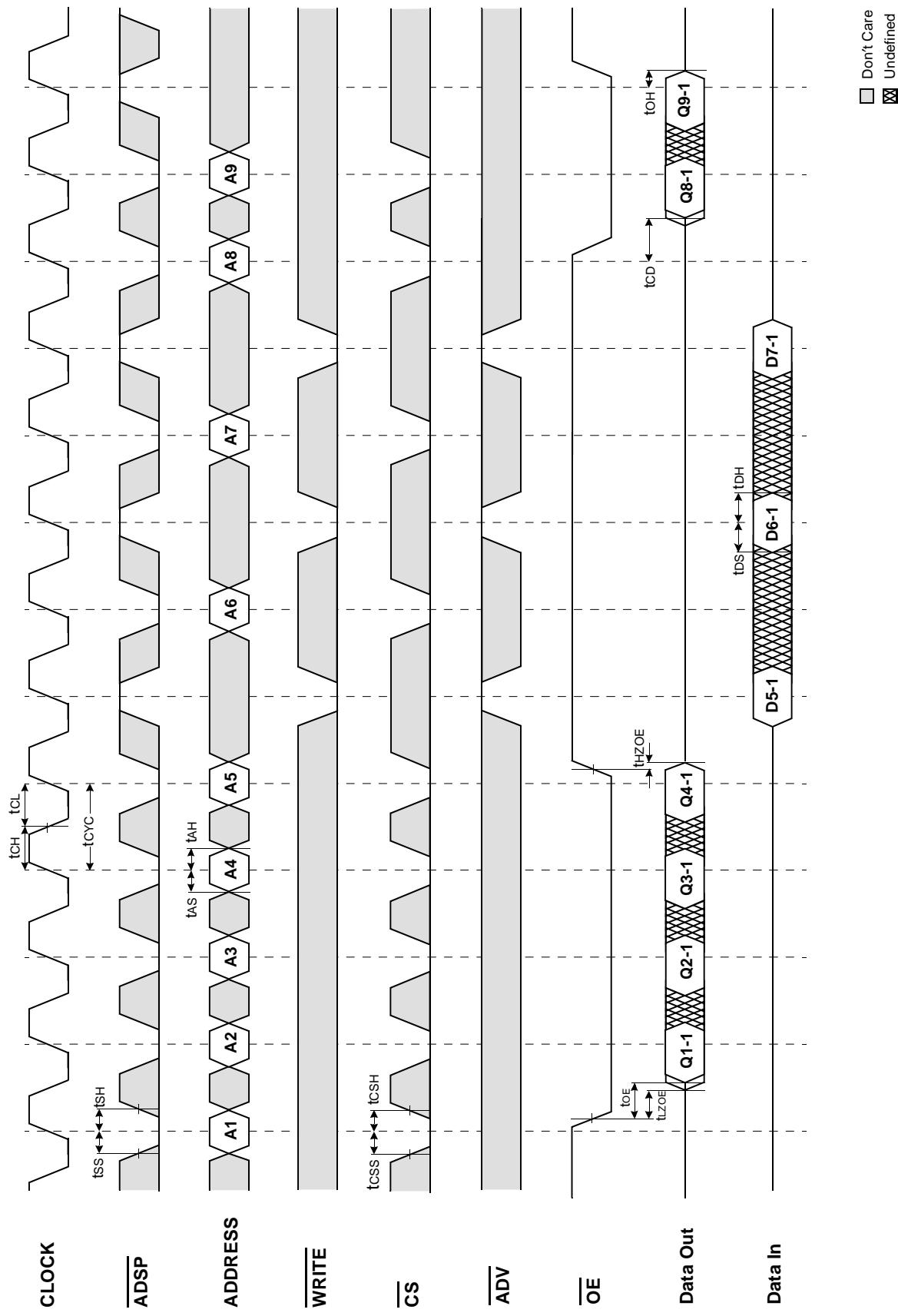
TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH)

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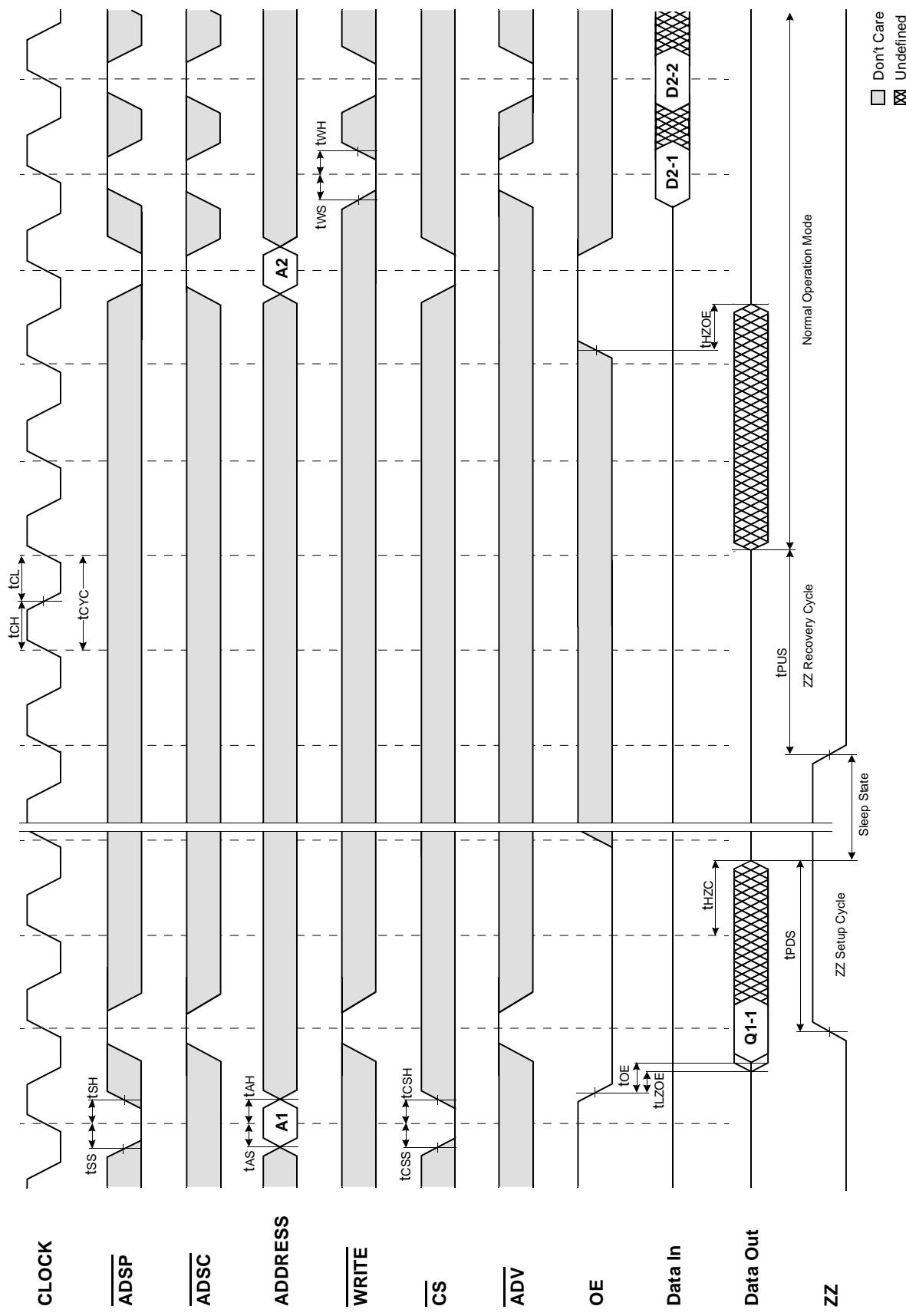
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, ADSP=HIGH)

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TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)

Don't Care
Undefined

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TIMING WAVEFORM OF POWER DOWN CYCLE

CLOCK
ADSP
ADSC
ADDRESS
WRITE
CS
ADV
OE
Data In
Data Out
ZZ

tSS, tSH, tAS, tAH, tCSS, tCSH, tOE, tLZOE, tCH, tCL, tCYC, tWS, tWH, tHZOE, tHZC, tPDS, tPUS

A1, A2, Q1-1, D2-1, D2-2

Normal Operation Mode, ZZ Recovery Cycle, Sleep State, ZZ Setup Cycle

Don't Care, Undefined

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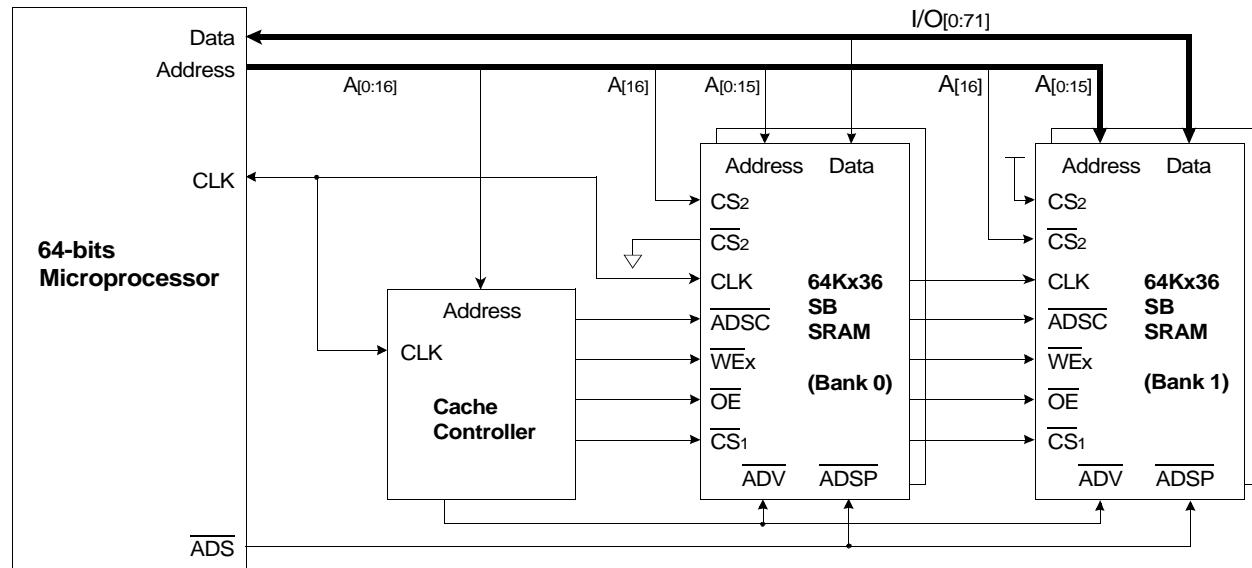
APPLICATION INFORMATION
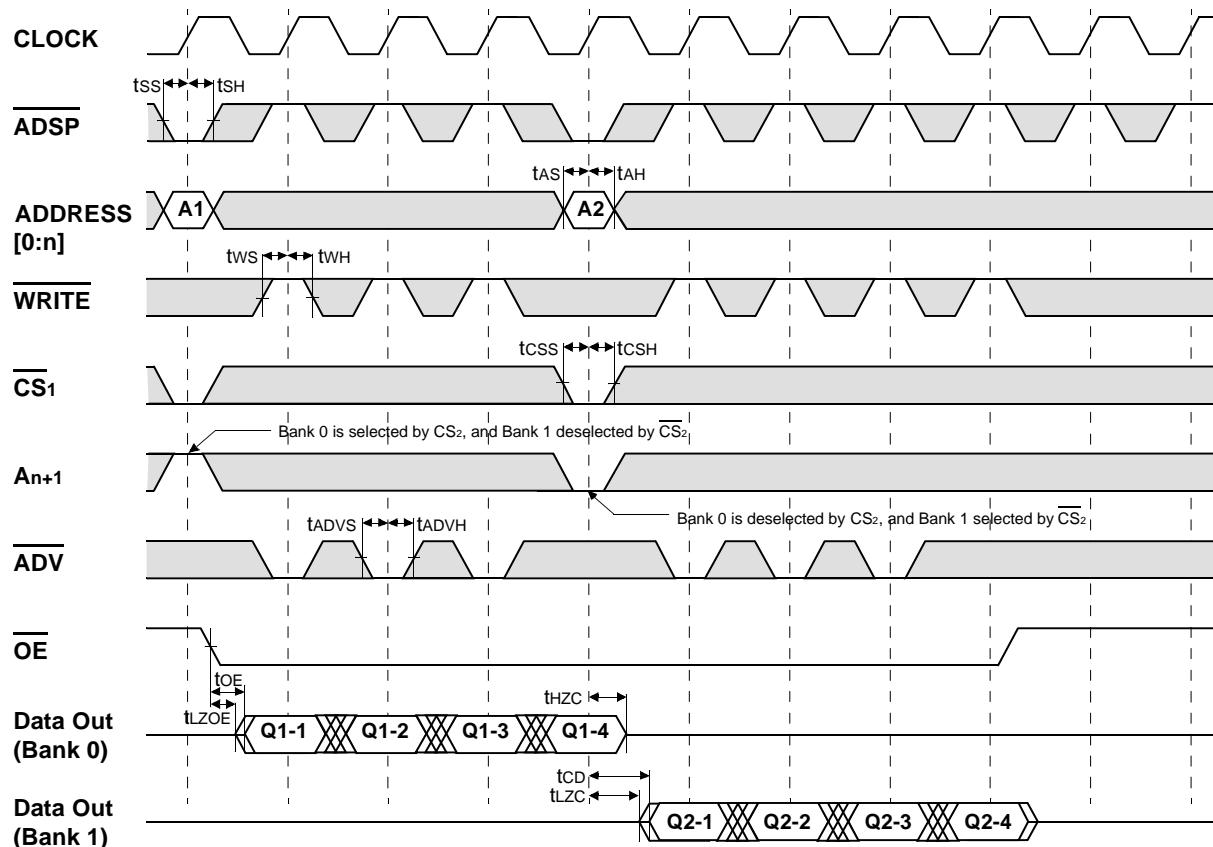
DEPTH EXPANSION

The Samsung 64Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.

INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

### ($\overline{ADSP}$ CONTROLLED , $\overline{ADSC}$=HiGH)

*NOTES n = 14   32K depth, 15   64K depth, 16   128K depth

☐ Don't Care   ☒ Undefined

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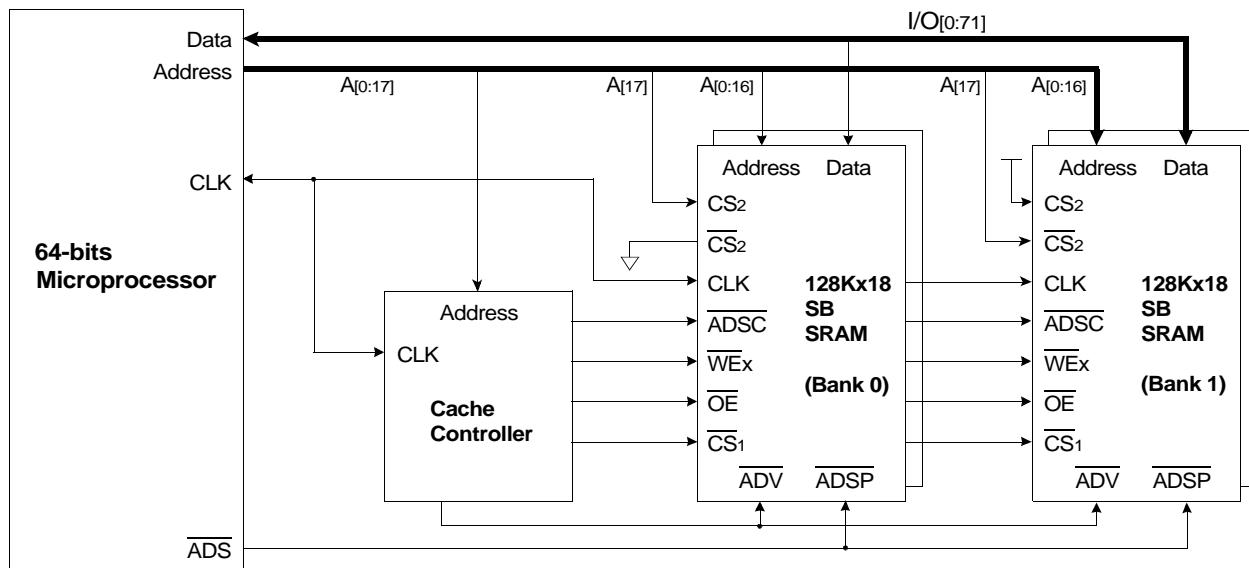
APPLICATION INFORMATION
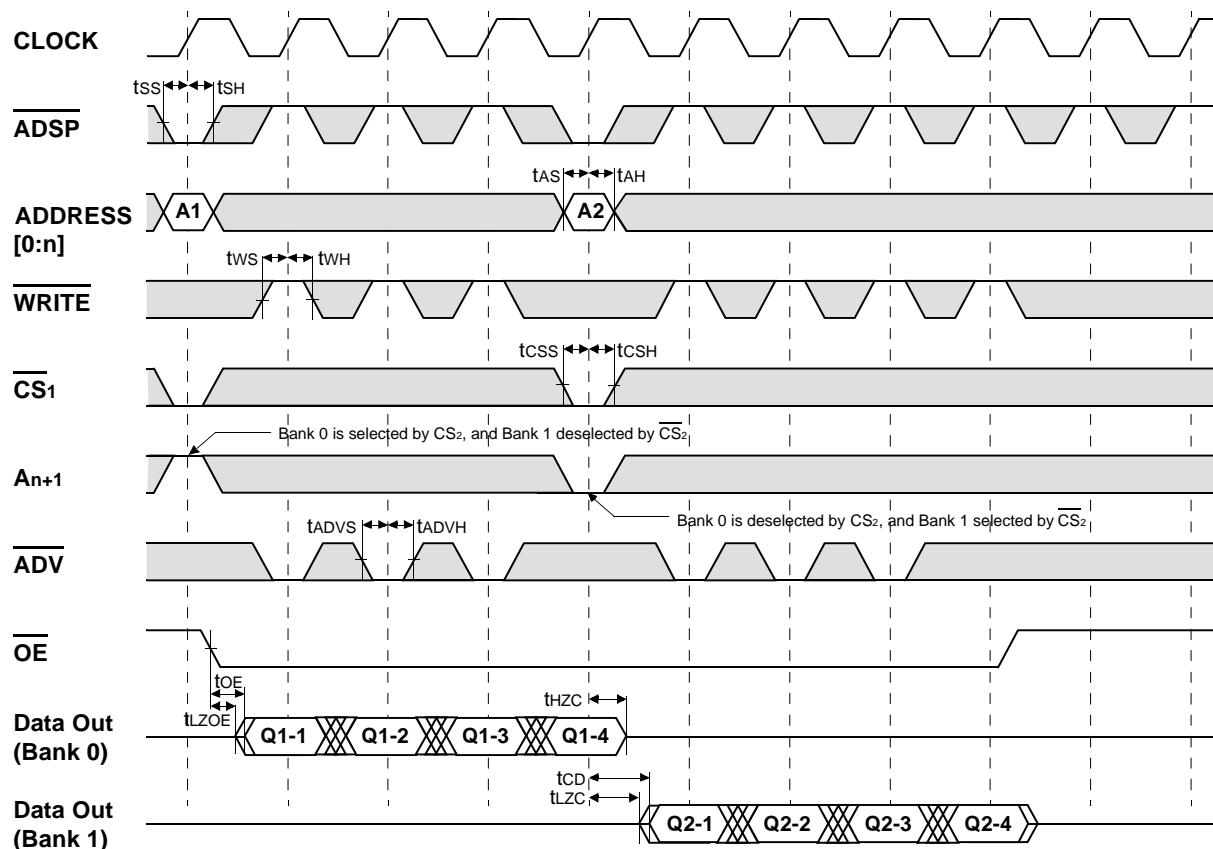
DEPTH EXPANSION

The Samsung 128Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.

INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

($\overline{\text{ADSP}}$ CONTROLLED , $\overline{\text{ADSC}}$=HiGH)

*NOTES n = 14   32K depth, 15   64K depth, 16   128K depth

Don't Care   Undefined

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64Kx36/x32 & 128Kx18 Synchronous SRAM

PACKAGE DIMENSIONS

100-TQFP-1420A   Units:millimeters/inches

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