TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74HC112AP,TC74HC112AF,TC74HC112AFN

#### Dual J-K Flip Flop with Preset and Clear

The TC74HC112A is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic levels applied to the J and K inputs, the outputs change state on the negative going transition of the clock pulse.

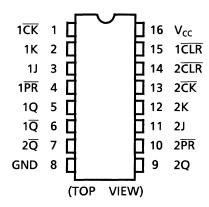
 $\overline{CLR}~$  and  $~\overline{PR}~$  are independent of the clock and are actived by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

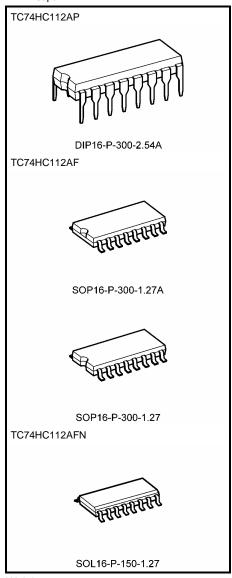
#### **Features**

- High speed:  $f_{max} = 67 \text{ MHz}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $ICC = 2 \mu A \text{ (max)}$  at  $Ta = 25^{\circ}C$
- High noise immunity: VNIH = VNIL = 28% VCC (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: |I<sub>OH</sub>| = I<sub>OL</sub> = 4 mA (min)
- Balanced propagation delays:  $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: VCC (opr) = 2 to 6 V
- Pin and function compatible with 74LS112

#### **Pin Assignment**



Note: xxxFN (JEDEC SOP) is not available in Japan.



Weight

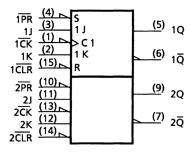
 DIP16-P-300-2.54A
 : 1.00 g (typ.)

 SOP16-P-300-1.27A
 : 0.18 g (typ.)

 SOP16-P-300-1.27
 : 0.18 g (typ.)

 SOL16-P-150-1.27
 : 0.13 g (typ.)

# **IEC Logic Symbol**

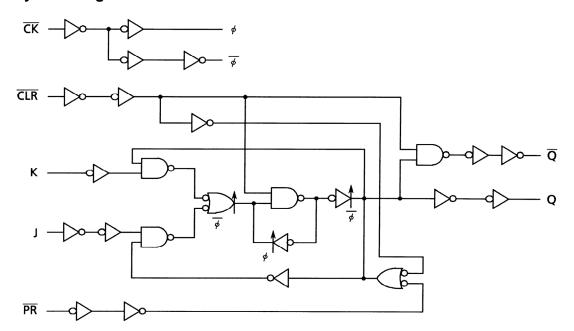


#### **Truth Table**

	Inputs						Function
CLR	PR	J	K	CK	Q	Q	Function
L	Н	Х	Х	Х	L	Н	Clear
Н	L	Х	Х	Х	Н	L	Preset
L	L	Х	Х	Х	Н	Н	
Н	Н	L	L	$\neg$	Qn	$\overline{Q}_n$	No Change
Н	Н	L	Н	$\neg$	L	Н	
Н	Н	Н	L	$\neg$	Н	L	
Н	Н	Н	Н		$\overline{Q}_n$	Qn	Toggle
Н	Н	Х	Х		Qn	$\overline{Q}_n$	No Change

X: Don't care

#### **System Diagram**





#### **Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	Vcc	–0.5 to 7	V
DC input voltage	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
DC output voltage	V <sub>OUT</sub>	−0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /ground current	Icc	±50	mA
Power dissipation	P <sub>D</sub>	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Note 2: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

#### **Recommended Operating Conditions (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	Vcc	2 to 6	V
Input voltage	V <sub>IN</sub>	0 to V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
		0 to 1000 (V <sub>CC</sub> = 2.0 V)	
Input rise and fall time	t <sub>r</sub> , t <sub>f</sub>	0 to 500 (V <sub>CC</sub> = 4.5 V)	ns
		0 to 400 ( $V_{CC} = 6.0 \text{ V}$ )	

Note: The recommended operating conditions are required to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.



#### **Electrical Characteristics**

#### **DC Characteristics**

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
Characteristics	Symbol			V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	Onit
				2.0	1.50	_	_	1.50	_	
High-level input voltage	V <sub>IH</sub>		_	4.5	3.15		_	3.15	_	V
				6.0	4.20	_	_	4.20	_	
				2.0	_	_	0.50	_	0.50	
Low-level input voltage	VIL	_		4.5	_	_	1.35	_	1.35	V
				6.0	_	_	1.80	_	1.80	
	V <sub>ОН</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		2.0	1.9	2.0	_	1.9	_	
			$I_{OH} = -20 \mu A$	4.5	4.4	4.5	_	4.4	_	
High-level output voltage				6.0	5.9	6.0		5.9	_	V
			$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	_	4.13		
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80		5.63	_	
	V <sub>OL</sub>			2.0		0.0	0.1	_	0.1	
			$I_{OL} = 20 \ \mu A$	4.5	_	0.0	0.1	_	0.1	
Low-level output voltage		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		6.0		0.0	0.1	_	0.1	V
			$I_{OL} = 4 \text{ mA}$	4.5	_	0.17	0.26	_	0.33	
			$I_{OL} = 5.2 \text{ mA}$	6.0	_	0.18	0.26	_	0.33	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0		_	±0.1	_	±1.0	μА
Quiescent supply current	Icc	$V_{IN} = V_{CC}$ or	GND	6.0	_	_	2.0	_	20.0	μА

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#### Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Test Condition			Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Тур.	Limit	Limit	
Minimum pulgo width	<b>4</b>		2.0	_	75	95	
Minimum pulse width ( CK )	t <sub>W</sub> (L)	_	4.5	_	15	19	ns
(CK)	t <sub>W (H)</sub>		6.0	_	13	16	
Minimum pulse width			2.0	_	75	95	
(CLR, PR)	t <sub>W (L)</sub>	_	4.5	_	15	19	ns
(OLK, FK)			6.0	_	13	16	
	t <sub>s</sub>		2.0	_	75	95	
Minimum set-up time		_	4.5	_	15	19	ns
			6.0	_	13	16	
			2.0	_	0	0	
Minimum hold time	th	_	4.5	_	0	0	ns
			6.0	_	0	0	
Minimum removal time			2.0	_	50	60	
(CLR, PR)	t <sub>rem</sub>	_	4.5	_	10	12	ns
(OLIX, FIX)			6.0	_	9	11	
			2.0	_	6	4	
Clock frequency	f	_	4.5	_	30	24	MHz
			6.0	_	34	28	

#### AC Characteristics (C<sub>L</sub> = 15 pF, $V_{CC}$ = 5 V, Ta = 25°C, input: $t_r$ = $t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Output transition time	t <sub>TLH</sub>	_	_	4	8	ns
Propagation delay time $(\overline{CK} \operatorname{-Q}, \overline{Q})$	t <sub>pLH</sub>	_	_	13	21	ns
Propagation delay time ( CLR , PR -Q, Q )	t <sub>pLH</sub>	_	_	15	22	ns
Maximum clock frequency	f <sub>max</sub>	_	32	67	_	MHz



AC Characteristics (C<sub>L</sub> = 50 pF, input:  $t_r = t_f = 6$  ns)

		Test Condition		Ta = 25°C			Ta = -40		
Characteristics	Symbol		V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	Unit
	tTLH		2.0	_	30	75	_	95	
Output transition time		_	4.5	_	8	15	_	19	ns
	t <sub>THL</sub>		6.0	_	7	13	_	16	
Propagation delay	<b>+</b>		2.0	_	52	125	_	155	
time	t <sub>pLH</sub> t <sub>pHL</sub>	_	4.5	_	16	25	_	31	ns
$(\overline{CK} - Q, \overline{Q})$			6.0	_	14	21	_	26	
Propagation delay	4		2.0	_	68	135	_	170	
time	t <sub>pLH</sub>	_	4.5	_	17	27	_	34	ns
$(\overline{CLR},\overline{PR}-Q,\overline{Q})$	t <sub>pHL</sub>		6.0	_	15	23	_	29	
			2.0	6	19	_	4	_	
Maximum clock frequency	f <sub>max</sub>	_	4.5	30	63	_	24	_	MHz
,,			6.0	34	71	_	28	_	
Input capacitance	C <sub>IN</sub>		•	_	5	10	_	10	pF
Power dissipation	C <sub>PD</sub>				35				pF
capacitance	(Note)				33				ρi

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

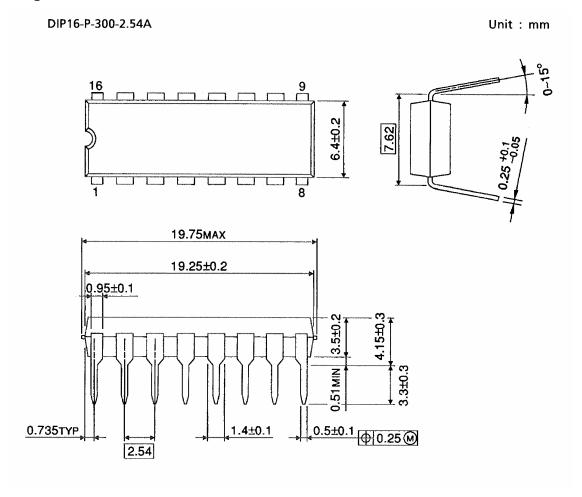
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Average operating current can be obtained by the equation:

 $I_{CC}$  (opr) =  $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$  (per F/F)



# **Package Dimensions**



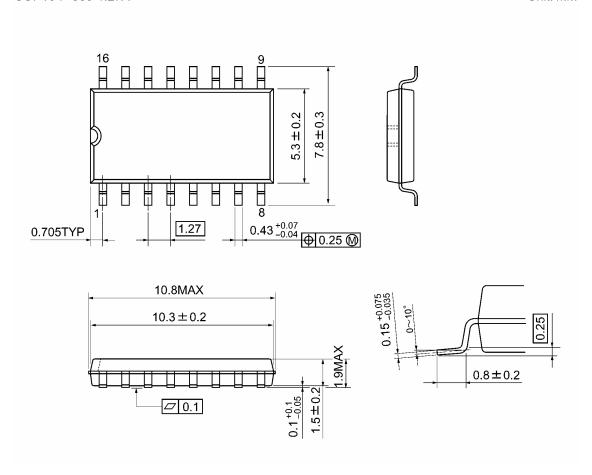
7

Weight: 1.00 g (typ.)



# **Package Dimensions**

SOP16-P-300-1.27A Unit: mm

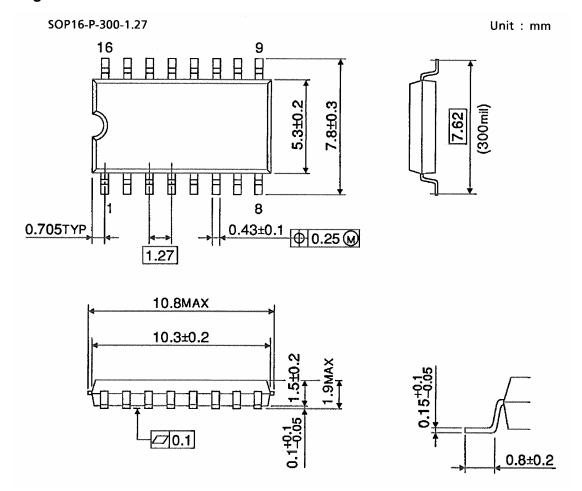


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Weight: 0.18 g (typ.)



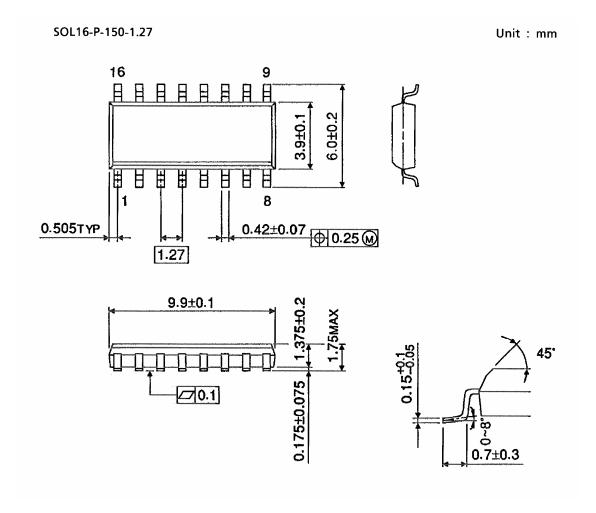
# **Package Dimensions**



Weight: 0.18 g (typ.)



# **Package Dimensions (Note)**



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

Note: Lead (Pb)-Free Packages

DIP16-P-300-2.54A SOP16-P-300-1.27A SOL16-P-150-1.27

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