# μPD4368
# 8,192 x 8-Bit
# Static CMOS RAM

## Description

The μPD4368 is a high-speed 8,192-word by 8-bit static RAM designed with CMOS peripheral circuits and N-channel memory cells with polysilicon resistors. Two chip enable pins are provided for battery backup application, and an output enable pin is provided for easy interface.

The μPD4368 is packaged in 28-pin plastic DIP and 28-pin plastic SOJ packaging.

## Features

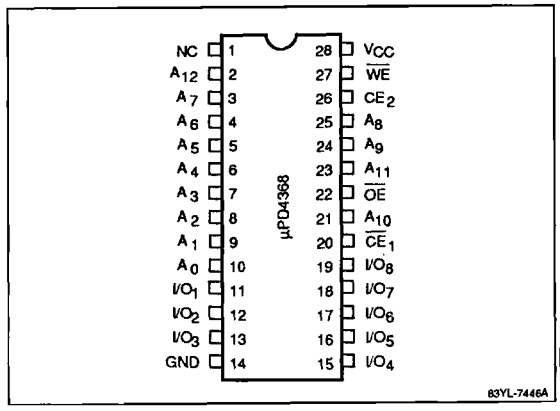
- 8,192 by 8-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{OE}$ and two $\overline{CE}$ pins for easy application
- Standard 28-pin plastic DIP, 28-pin plastic SOJ packaging

## Ordering Information

| Part Number | Access Time (max) | Package |
|---|---|---|
| μPD4368CR-15 | 15 ns | 28-pin plastic DIP |
| CR-20 | 20 ns | |
| μPD4368LA-15 | 15 ns | 28-pin plastic SOJ |
| LA-20 | 20 ns | |

## Pin Configuration

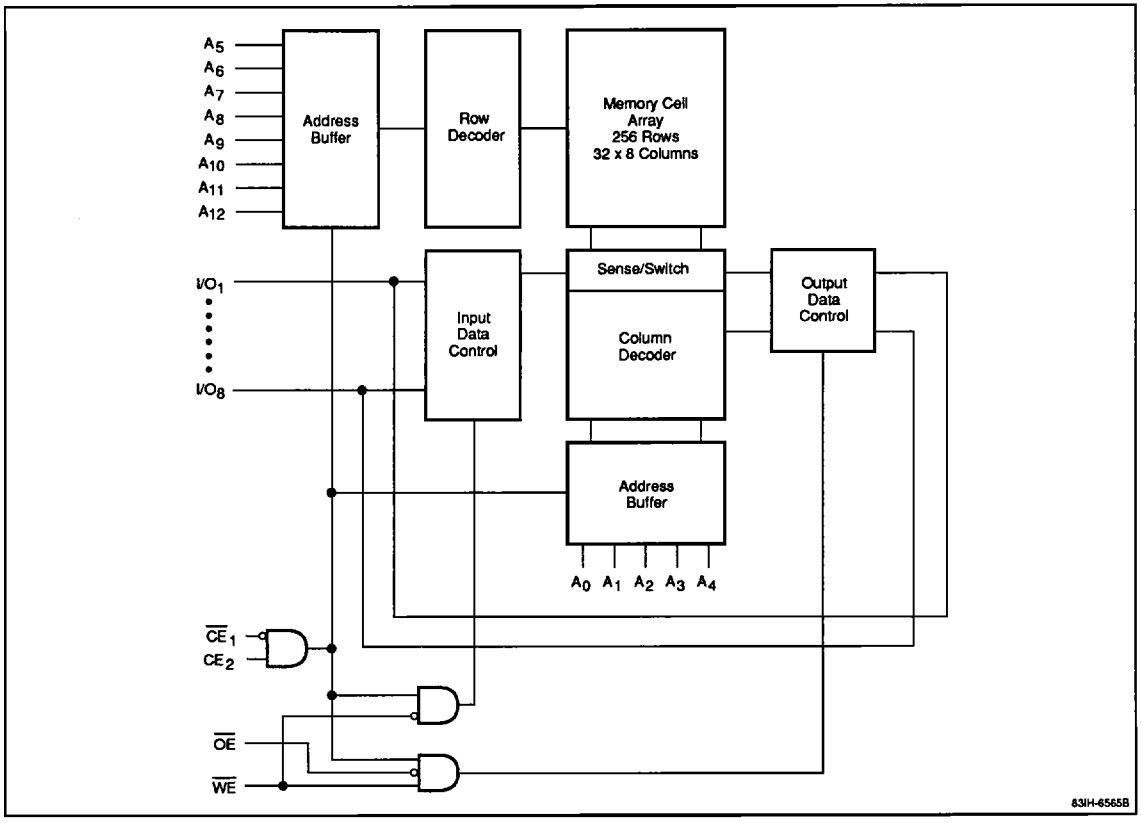
***28-Pin Plastic DIP or SOJ***




## Pin Identification

| Symbol | Function |
|---|---|
| $A_0$ - $A_{12}$ | Address inputs |
| $I/O_1$ - $I/O_8$ | Data inputs/outputs |
| $\overline{CE_1}$ | Chip enable (active low) |
| $CE_2$ | Chip enable (active high) |
| $\overline{OE}$ | Output enable |
| $\overline{WE}$ | Write enable |
| GND | Ground |
| $V_{CC}$ | +5-volt power supply |
| NC | No connection |

## Block Diagram



## Absolute Maximum Ratings

| | |
|---|---|
| Supply voltage, $V_{CC}$ (Note 1) | −0.5 to +7.0 V |
| Input voltage, $V_{IN}$ (Note 1) | −0.5 V to $V_{CC}$ + 0.3 V |
| Output voltage, $V_{OUT}$ (Note 1) | −0.5 V to $V_{CC}$ + 0.3 V |
| Operating temperature, $T_{OPR}$ | 0 to +70°C |
| Storage temperature, $T_{STG}$ | −55 to +125°C |
| Power dissipation, $P_D$ | 1.0 W |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

**Notes:**

(1) −3.0 V min for 10 ns maximum pulse.

## Capacitance

$T_A$ = 25°C; f = 1 MHz; $V_{IN}$ and $V_{OUT}$ = 0 V

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | | | 6 | pF |
| Input/output capacitance | $C_{I/O}$ | | | 8 | pF |

## Truth Table

| Function | $\overline{CE}_1$ | $CE_2$ | $\overline{OE}$ | $\overline{WE}$ | I/O | $I_{CC}$ |
|---|---|---|---|---|---|---|
| Not selected | H | X | X | X | High-Z | Standby |
| Not selected | X | L | X | X | High-Z | Standby |
| $D_{OUT}$ disabled | L | H | H | H | High-Z | Active |
| Read | L | H | L | H | $D_{OUT}$ | Active |
| Write | L | H | X | L | $D_{IN}$ | Active |

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input voltage, high | $V_{IH}$ | 2.2 | | $V_{CC}$ + 0.3 | V |
| Input voltage, low | $V_{IL}$ | −0.5 | | 0.8 | V |
| Operating temperature | $T_A$ | 0 | | 70 | °C |

**Notes:**

(1) $V_{IL}$ = −3.0 V min for 10 ns maximum pulse.

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## DC Characteristics

$T_A$ = 0 to +70°C; $V_{CC}$ = +5.0 V ±10%

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | −2 | | 2 | μA | $V_{IN}$ = 0 V to $V_{CC}$ |
| Output leakage current | $I_{LO}$ | −2 | | 2 | μA | $V_{I/O}$ = 0 V to $V_{CC}$; $\overline{CE}_1$ = $V_{IH}$ or $CE_2$ = $V_{IL}$ or $\overline{OE}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ |
| Operating supply current | $I_{CC}$ | | | 120 | mA | $\overline{CE}_1$ = $V_{IL}$; $CE_2$ = $V_{IH}$; $I_{I/O}$ = 0 mA (min cycle) |
| Standby supply current | $I_{SB}$ | | | 20 | mA | $\overline{CE}_1$ ≥ $V_{IH}$ or $CE_2$ = $V_{IL}$ |
| | $I_{SB1}$ | | | 2 | mA | $\overline{CE}_1$ ≥ $V_{CC}$ − 0.2 V; $CE_2$ ≥ $V_{CC}$ − 0.2 V |
| Output voltage, low | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |
| Output voltage, high | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = −4.0 mA |

## AC Characteristics

$T_A$ = 0 to +70°C; $V_{CC}$ = +5.0 V ±10%

| Parameter | Symbol | μPD4368-15 Min | μPD4368-15 Max | μPD4368-20 Min | μPD4368-20 Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| ***Read Operation*** | | | | | | | |
| Read cycle time | $t_{RC}$ | 15 | | 20 | | ns | |
| Address access time | $t_{AA}$ | | 15 | | 20 | ns | |
| $\overline{CE}_1$ access time | $t_{CO1}$ | | 15 | | 20 | ns | |
| $CE_2$ access time | $t_{CO2}$ | | 15 | | 20 | ns | |
| Output enable to output valid | $t_{OE}$ | | 9 | | 10 | ns | |
| Output hold from address change | $t_{OH}$ | 3 | | 3 | | ns | |
| $\overline{CE}_1$ to output in low-Z | $t_{LZ1}$ | 3 | | 3 | | ns | |
| $CE_2$ to output in low-Z | $t_{LZ2}$ | 3 | | 3 | | ns | |
| $\overline{OE}$ to output in low-Z | $t_{OLZ}$ | 0 | | 0 | | ns | |
| $\overline{CE}_1$ to output in high-Z | $t_{HZ1}$ | | 8 | | 9 | ns | |
| $CE_2$ to output in high-Z | $t_{HZ2}$ | | 8 | | 9 | ns | |
| $\overline{OE}$ to output in high-Z | $t_{OHZ}$ | | 7 | | 8 | ns | |
| ***Write Operation*** | | | | | | | |
| Write cycle time | $t_{WC}$ | 15 | | 20 | | ns | |
| Chip enable ($\overline{CE}_1$) to end of write | $t_{CW1}$ | 12 | | 13 | | ns | |
| Chip enable ($CE_2$) to end of write | $t_{CW2}$ | 12 | | 13 | | ns | |
| Address valid to end of write | $t_{AW}$ | 12 | | 13 | | ns | |
| Address setup time | $t_{AS}$ | 0 | | 0 | | ns | |
| Write pulse width | $t_{WP}$ | 11 | | 12 | | ns | |
| Write recovery time | $t_{WR}$ | 2 | | 2 | | ns | |
| Data valid to end of write | $t_{DW}$ | 9 | | 10 | | ns | |
| Data hold time | $t_{DH}$ | 0 | | 0 | | ns | |
| Write enable to output in high-Z | $t_{WHZ}$ | | 7 | | 8 | ns | |
| Output active from end of write | $t_{OW}$ | 0 | | 0 | | ns | |

**Notes:**

(1) Input pulse levels = 0.8 to 2.4 V; input pulse rise and fall times = 5 ns; timing reference level = 1.5 V; see figures 1 and 2 for output load.

***Figure 1. Output Load ($t_{RC}$, $t_{AA}$, $t_{CO1}$, $t_{CO2}$, $t_{OE}$, $t_{OH}$)***

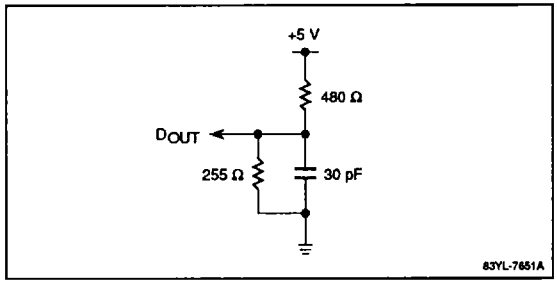
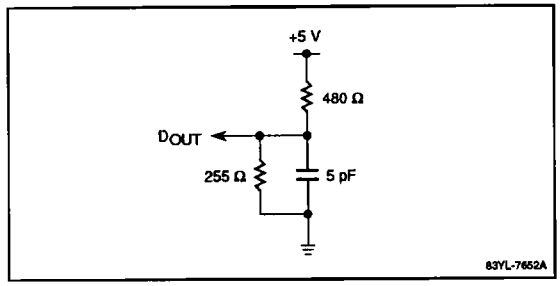
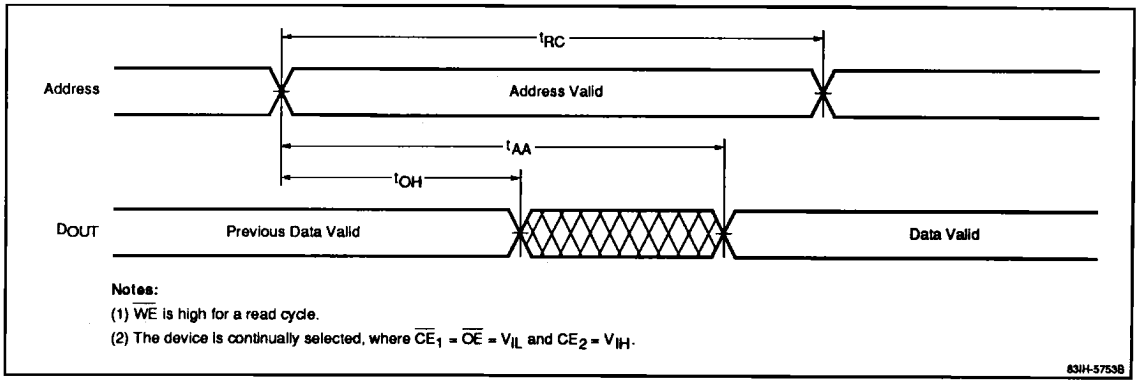



***Figure 2. Output Load ($t_{HZ1}$, $t_{HZ2}$, $t_{OHZ}$, $t_{WHZ}$, $t_{LZ1}$, $t_{LZ2}$, $t_{OLZ}$, $t_{OW}$)***



## Timing Waveforms

### *Address Access Cycle*




Notes:
(1) $\overline{WE}$ is high for a read cycle.
(2) The device is continually selected, where $\overline{CE_1} = \overline{OE} = V_{IL}$ and $CE_2 = V_{IH}$.

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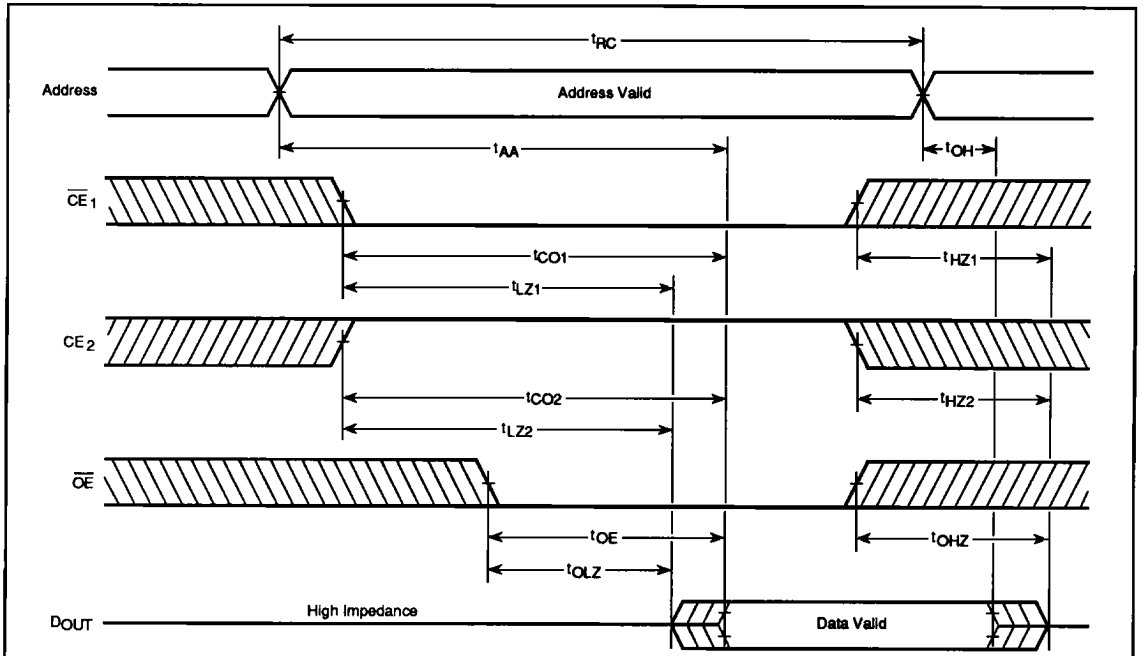
### *Chip Enable Access Cycle*






Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the latter of the low transition of $\overline{CE_1}$ or the high transition of $CE_2$.

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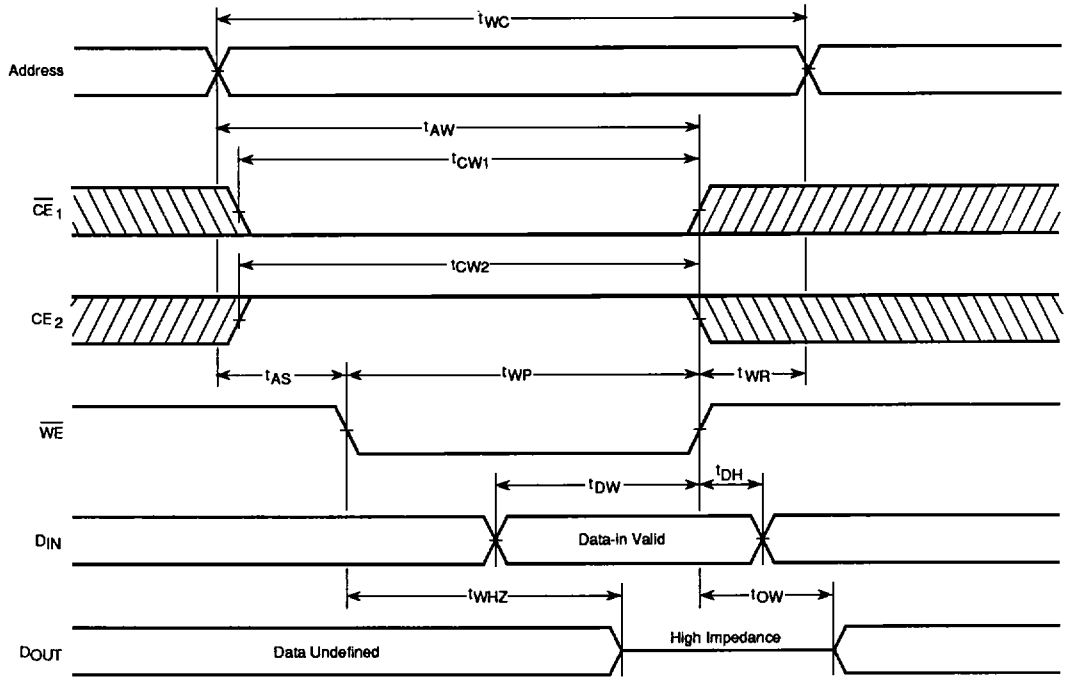
## Timing Waveforms (cont)

### *$\overline{WE}$-Controlled Write Cycle*




**Notes:**

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high $CE_2$.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or $CE_2$ must be low during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

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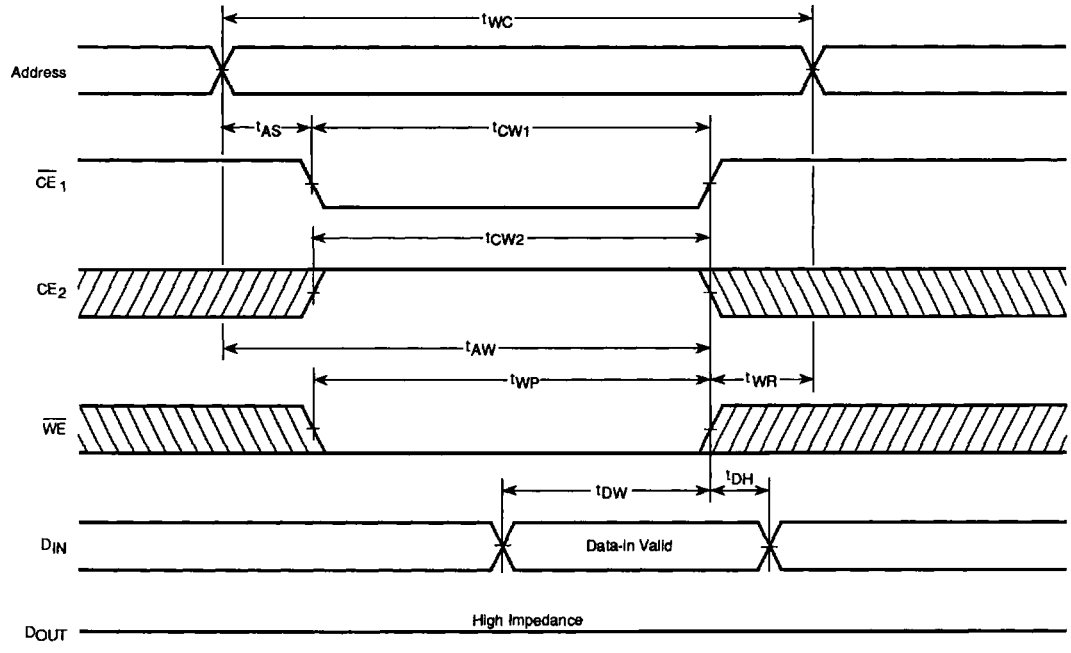
## Timing Waveforms (cont)

### $\overline{CE}_1$-Controlled Write Cycle




**Notes:**

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high $CE_2$.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or $CE_2$ must be low during address transition.

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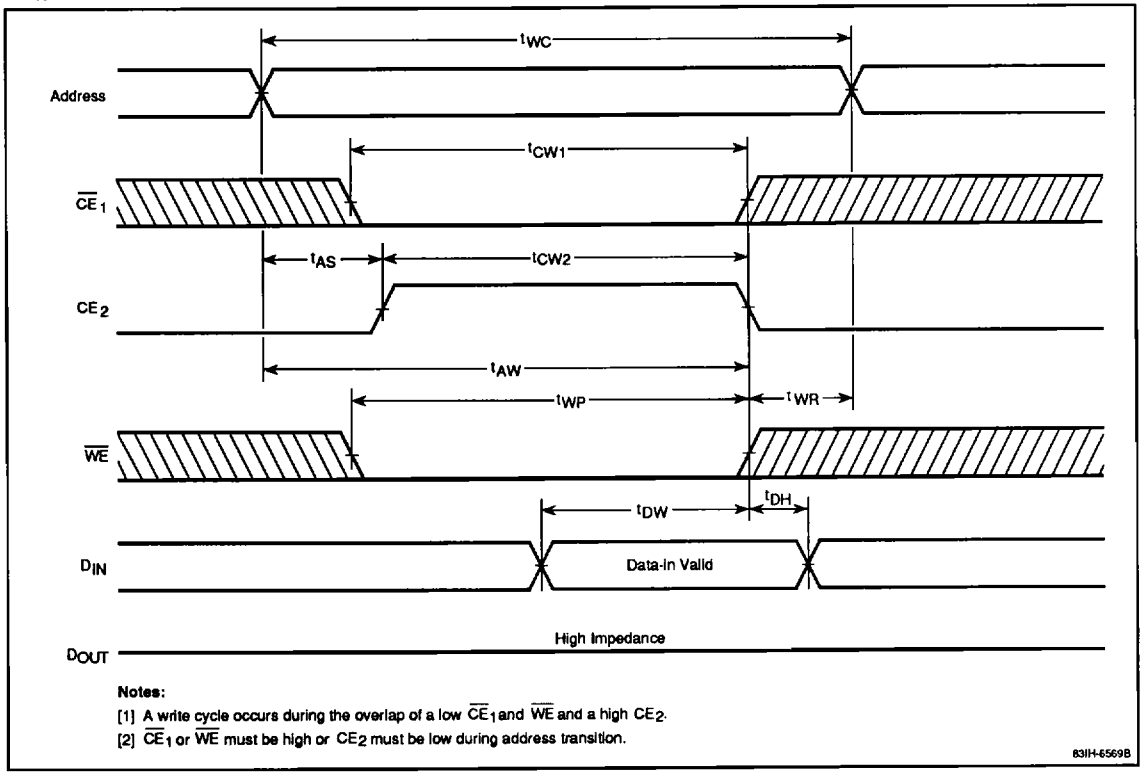
## Timing Waveforms (cont)

### *$CE_2$-Controlled Write Cycle*




**Notes:**

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high $CE_2$.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or $CE_2$ must be low during address transition.

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