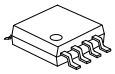
U74LVC2G126

CMOS IC

DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS



MSOP-8

TSSOP-8

Lead-free: U74LVC2G126L
Halogen-free: U74LVC2G126G

■ DESCRIPTION

The **U74LVC2G126** consists of two bus buffers with 3-state output controlled by enable input (nOE), when nOE is low, the output is disabling.

Inputs can be driven from either 3.3V or 5V devices, so the device can be used in a mix 3.3V/5V system.

This device is full specified for partial power-down protective circuit, preventing the backflow current through the device when it is powered down.

■ FEATURES

* Operation voltage range: 1.65~5.5V
* Support 5V V_{CC} operation
* Low power dissipation
* Input accept voltage to 5.5V

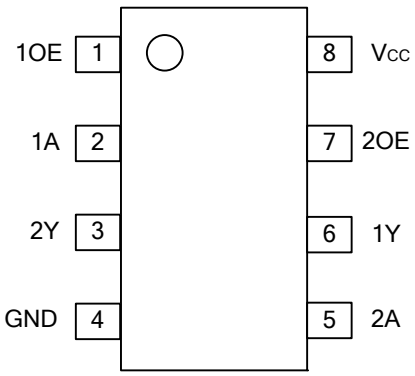
■ ORDERING INFORMATION

Ordering Number			Package	Packing
Normal	Lead Free Plating	Halogen Free		
U74LVC2G126-P08-R	U74LVC2G126L-P08-R	U74LVC2G126G-P08-R	TSSOP-8	Tape Reel
U74LVC2G126-SM1-R	U74LVC2G126L-SM1-R	U74LVC2G126G-SM1-R	MSOP-8	Tape Reel

U74LVC2G126L-P08-R
(1)Packing Type
(2)Package Type
(3)Lead Plating

(1) R: Tape Reel
(2) P08: TSSOP-8, SM1:MSOP-8
(3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn

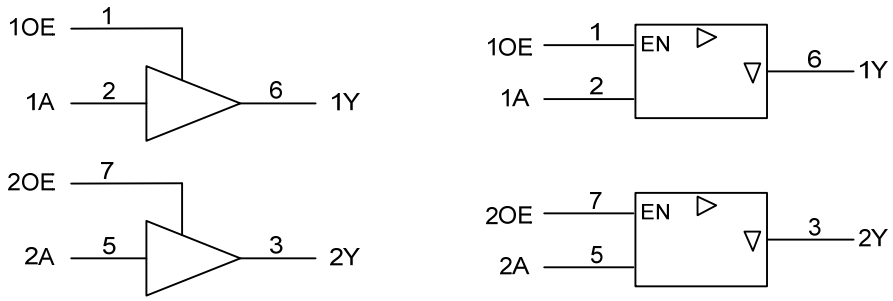
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(nOE)	INPUT(A)	OUTPUT(Y)
H	L	L
H	H	H
L	X	Z

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5~6.5	V
Input Voltage		V_{IN}	-0.5~6.5	V
Output Voltage	Enable	V_{OUT}	-0.5~V_{CC}+0.5	V
	Disable		-0.5~6.5	V
	Power-down		-0.5~6.5	V
V_{CC} or GND Current		I_{CC}	±100	mA
Input Clamp Current(V_{IN}<0)		I_{IK}	-50	mA
Output Clamp Current(V_{OUT}<0)		I_{OK}	±50	mA
Output Current		I_{OUT}	±50	mA
Power Dissipation		P_D	300	mW
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}		1.65		5.5	V
Input Voltage		V_{IN}		0		5.5	V
Output Voltage	Enable	V_{OUT}	V_{CC} =1.65~5.5V	0		V_{CC}	V
	Disable		V_{CC} =1.65~5.5V	0		5.5	V
	Power-down		V_{CC} =0V	0		5.5	V
Input Transition Rise or Fall Rate		t_R, t_F	V_{CC} =1.65~2.7V	0		20	ns/V
			V_{CC} =2.7~5.5V	0		10	ns/V
Operating Temperature		T_A		-40		125	°C

■ STATIC CHARACTERISTICS (T_a=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-Going Input Threshold Voltage	V_{T+}	V_{CC}=1.65V~1.95V	0.65×V_{CC}			V
		V_{CC}=2.3V~2.7V	1.7			V
		V_{CC}=2.7V~3.6V	2			V
		V_{CC}=4.5V~5.5V	0.7×V_{CC}			V
Negative-Going Input Threshold Voltage	V_{T-}	V_{CC}=1.65V~1.95V			0.35×V_{CC}	V
		V_{CC}=2.3V~2.7V			0.7	V
		V_{CC}=2.7V~3.6V			0.8	V
		V_{CC}=4.5V~5.5V			0.3×V_{CC}	V
High-Level Output Voltage	V_{OH}	V_{CC}=1.65V~5.5V, I_{OH}=-100μA	V_{CC}–0.1			V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2			V
		V_{CC}=2.3V, I_{OH}=-8mA	1.9			V
		V_{CC}=2.7V, I_{OH}=-12mA	2.2			V
		V_{CC}=3V, I_{OH}=-24mA	2.3			V
		V_{CC}=4.5V, I_{OH}=-32mA	3.8			V
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65V~5.5V, I_{OL}=100μA			0.1	V
		V_{CC}=1.65V, I_{OL}=4mA			0.45	V
		V_{CC}=2.3V, I_{OL}=8mA			0.3	V
		V_{CC}=2.7V, I_{OL}=12mA			0.4	V
		V_{CC}=3V, I_{OL}=24mA			0.55	V
		V_{CC}=4.5V, I_{OL}=32mA			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}=5.5V or GND		±0.1	±5	μA
Output OFF -State Current	I_{OZ}	V_{CC}=3.6V, V_{OUT}=V_{CC} or GND		±0.1	±10	μA
Power OFF Leakage Current	I_{OFF}	V_{CC}=0V, V_{IN} or V_{OUT} =5.5V		±0.1	±10	μA

■ STATIC CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Supply Current	I_Q	V_{CC}=5.5V, V_{IN}=V_{CC} or GND I_{OUT}=0		0.1	10	μA
Additional Quiescent Supply Current	ΔI_Q	V_{CC}=2.3V~5.5V, One input at V_{CC}- 0.6V, other inputs at V_{CC} or GND		5	500	μA
Input Capacitance	C_{IN}	V_{IN}=V_{CC} or GND		2		pF

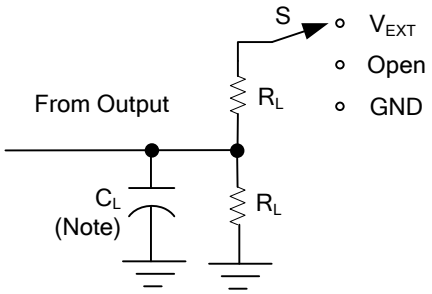
■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input(A) to Output(Y)	t_{PHL}/t_{PLH}	V_{CC}=1.8V±0.15V	1	3.9	9.8	ns
		V_{CC}=2.5V±0.2V	0.5	2.6	4.9	ns
		V_{CC}=2.7V	1	2.8	4.7	ns
		V_{CC}=3.3V±0.3V	0.5	2.4	4.3	ns
		V_{CC}=5.0V±0.5V	0.5	1.9	3.2	ns
Propagation Delay From Input(nOE) to Output(Y)	t_{PZH}/t_{PZL}	V_{CC}=1.8V±0.15V	1.0	4.1	10	ns
		V_{CC}=2.5V±0.2V	1.0	2.6	5	ns
		V_{CC}=2.7V	1.0	2.8	4.7	ns
		V_{CC}=3.3V±0.3V	1.0	2.4	4.1	ns
		V_{CC}=5.0V±0.5V	0.5	1.8	3.1	ns
Propagation Delay From Input(nOE) to Output(Y)	t_{PZL}/t_{PZH}	V_{CC}=1.8V±0.15V	1	3.3	12.6	ns
		V_{CC}=2.5V±0.2V	0.5	1.9	5.7	ns
		V_{CC}=2.7V	1	3.0	4.8	ns
		V_{CC}=3.3V±0.3V	1	2.5	4.4	ns
		V_{CC}=5.0V±0.5V	0.5	1.8	3.3	ns

■ OPERATING CHARACTERISTICS (T_a=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	Output Enable		17		pF
		Output Disable		5		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{EXT}

Note : C_L includes probe and jig capacitance.

V_{CC}	V_{IN}	t_R, t_F	V_M	V_{EXT}	C_L	R_L	$V_\triangle$
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2* V_{CC}	30pF	1KΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2* V_{CC}	30pF	500Ω	0.15V
2.7V	2.7V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
3.3V±0.3V	2.7 V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2* V_{CC}	50pF	500Ω	0.3V