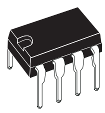
TL072 - TL072A - TL072B

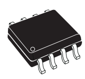
Low noise JFET dual operational amplifiers

Features

- Wide common-mode (up to V_{CC}^+) and differential voltage range
- Low input bias and offset current
- Low noise e_n = 15nV/√Hz (typ)
- Output short-circuit protection
- High input impedance JFET input stage
- Low harmonic distortion: 0.01% (typ)
- Internal frequency compensation
- Latch-up free operation
- High slew rate: 16 V/µs (typ)

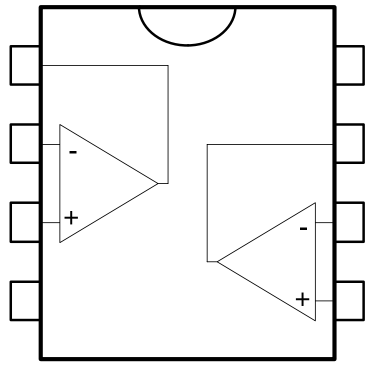


N
DIP8
(Plastic package)



D
SO-8
(Plastic micropackage)

Pin connections (top view)



1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 -Inverting input 2
7 - Output 2
8 - V_{CC}^+

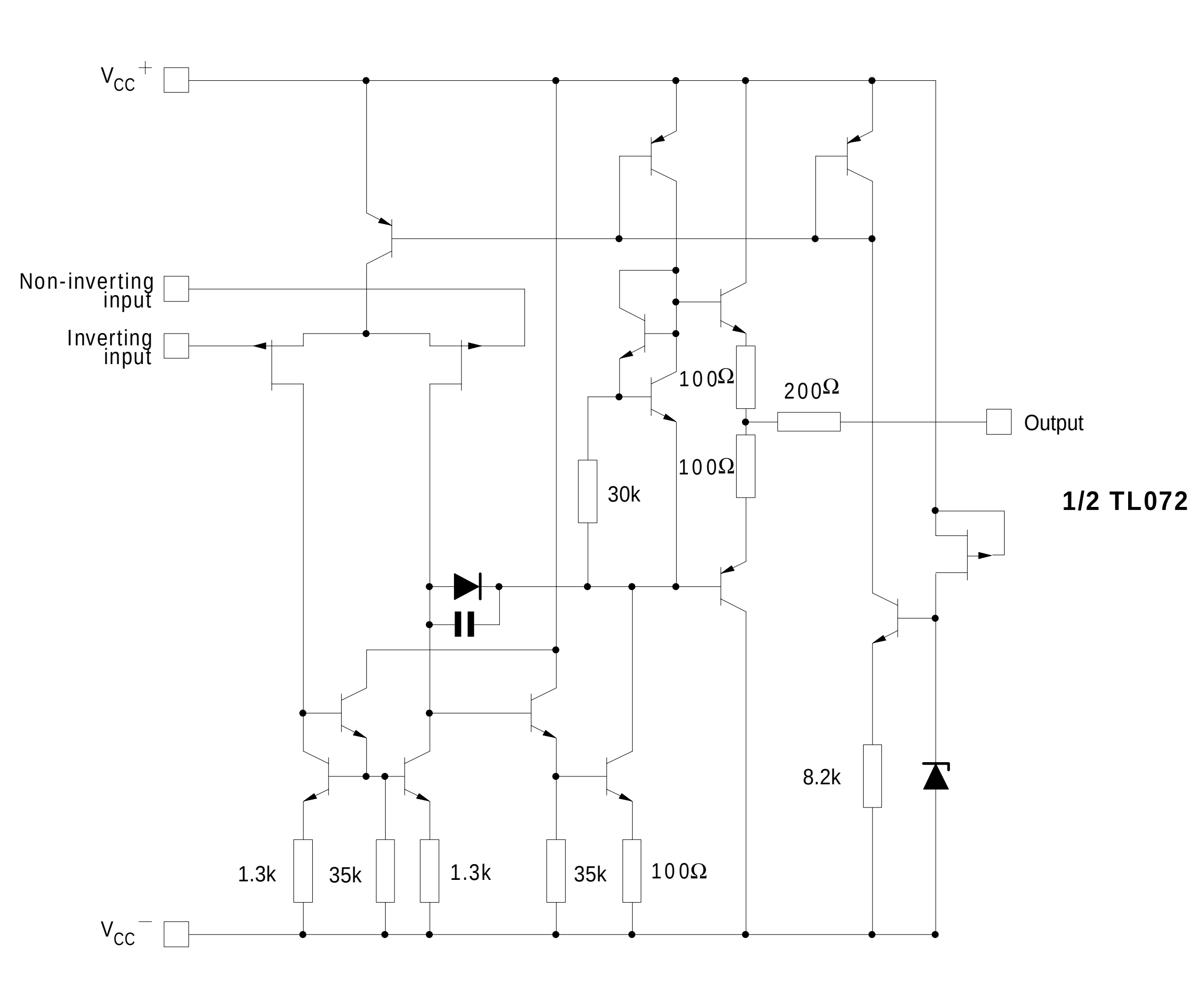
Description

The TL072, TL072A and TL072B are high speed JFET input dual operational amplifiers incorporating well matched, high voltage JFET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

1 Schematic diagram

Figure 1. Schematic diagram



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	TL072M, AM, BM	TL072I, AI, BI	TL072C, AC, BC	Unit
V_{CC}	Supply voltage (1)	±18			V
V_i	Input voltage (2)	±15			V
V_{id}	Differential input voltage (3)	±30			V
R_{thja}	Thermal resistance junction to ambient(4) SO-8 DIP8	 125 85			°C/W
R_{thjc}	Thermal resistance junction to case (4) SO-8 DIP8	 40 41			°C/W
	Output short-circuit duration (5)	Infinite			
T_{stg}	Storage temperature range	-65 to +150			°C
ESD	HBM: human body model(6)	1			kV
	MM: machine model(7)	200			V
	CDM: charged device model(8)	1.5			kV

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
5. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
6. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
7. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of pin combinations with other pins floating.
8. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	TL072M, AM, BM	TL072I, AI, BI	TL072C, AC, BC	Unit
V_{CC}	Supply voltage	6 to 36			V
T_{oper}	Operating free-air temperature range	-55 to +125	-40 to +105	0 to +70	°C

3 Electrical characteristics

Table 3. Electrical characteristics at V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	TL072I,M,AC,AI,AM BC,BI,BM			TL072C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input offset voltage (R_s = 50Ω) T_{amb} = +25°C TL072 TL072A TL072B $T_{min} \le T_{amb} \le T_{max}$ TL072 TL072A TL072B		3 3 1	10 6 3 13 7 5		3	10 13	mV
DV_{io}	Input offset voltage drift		10			10		µV/°C
I_{io}	Input offset current [(1)] T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	100 4		5	100 10	pA nA
I_{ib}	Input bias current [(1)] T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		20	200 20		20	200 20	pA nA
A_{vd}	Large signal voltage gain (R_L = 2kΩ, V_o = ±10V) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	50 25	200		25 15	200		V/mV
SVR	Supply voltage rejection ratio (R_S = 50Ω) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	80 80	86		70 70	86		dB
I_{CC}	Supply current, no load T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		1.4	2.5 2.5		1.4	2.5 2.5	mA
V_{icm}	Input common mode voltage range	±11	-12 to +15		±11	-12 to +15		V
CMR	Common mode rejection ratio (R_S = 50Ω) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	80 80	86		70 70	86		dB
I_{os}	Output short-circuit current T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	10 10	40	60 60	10 10	40	60 60	mA

Table 3. Electrical characteristics at V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified) (continued)

Symbol	Parameter	TL072I,M,AC,AI,AM BC,BI,BM			TL072C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$\pm V_{opp}$	Output voltage swing T_{amb} = +25°C R_L = 2kΩ R_L = 10kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 2kΩ R_L = 10kΩ	 10 12 10 12	 12 13.5		 10 12 10 12	 12 13.5		V
SR	Slew rate (T_{amb} = +25°C) V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, unity gain	8	16		8	16		V/µs
t_r	Rise time (T_{amb} = +25°C) V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain		0.1			0.1		µs
K_{ov}	Overshoot (T_{amb} = +25°C) V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain		10			10		%
GBP	Gain bandwidth product (T_{amb} = +25°C) V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF, f= 100kHz	2.5	4		2.5	4		MHz
R_i	Input resistance		10^{12}			10^{12}		Ω
THD	Total harmonic distortion (T_{amb} = +25°C) f= 1kHz, R_L = 2kΩ,C_L = 100pF, A_v = 20dB, V_o = $2V_{pp}$		0.01			0.01		%
e_n	Equivalent input noise voltage R_S = 100Ω, f = 1KHz		15			15		$\frac{nV}{\sqrt{Hz}}$
∅m	Phase margin		45			45		degrees
V_{o1}/V_{o2}	Channel separation A_v = 100		120			120		dB

1. The input bias currents are junction leakage currents which approximately double for every 10° C increase in the junction temperature.

Figure 2. Maximum peak-to-peak output voltage versus frequency

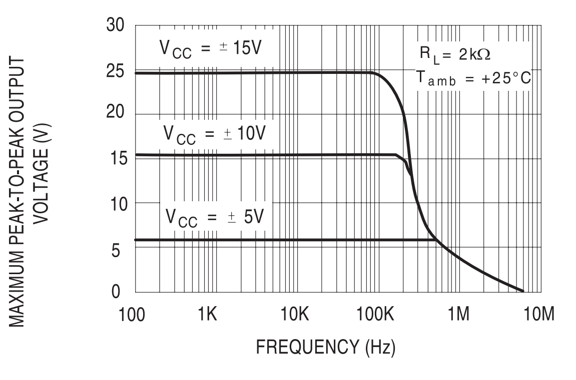


Figure 3. Maximum peak-to-peak output voltage versus frequency

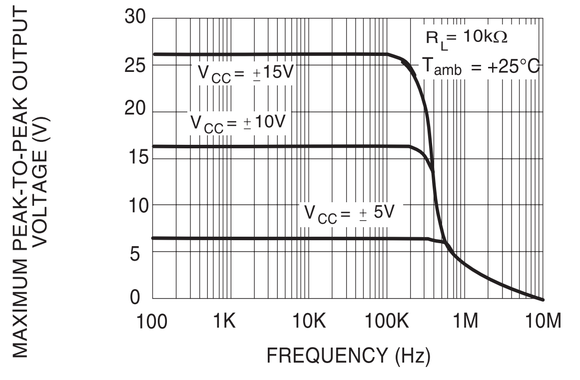


Figure 4. Maximum peak-to-peak output voltage versus frequency

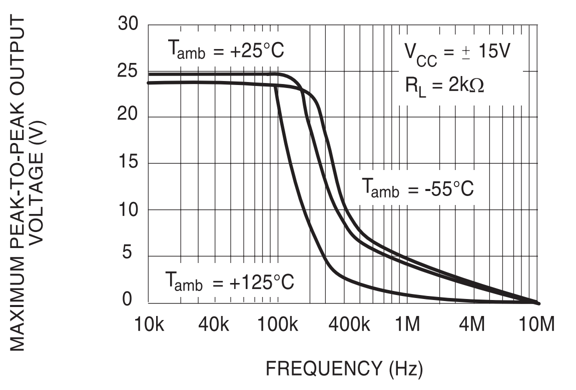


Figure 5. Maximum peak-to-peak output voltage versus free air temperature

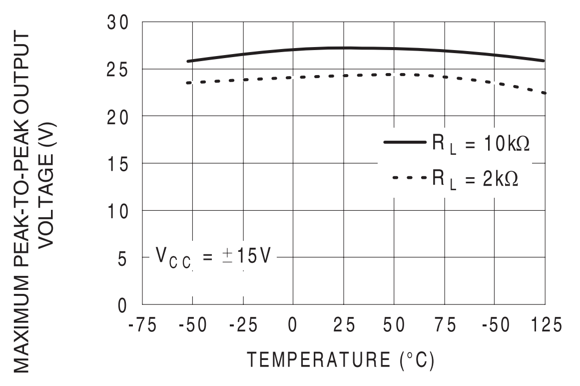


Figure 6. Maximum peak-to-peak output voltage versus load resistance

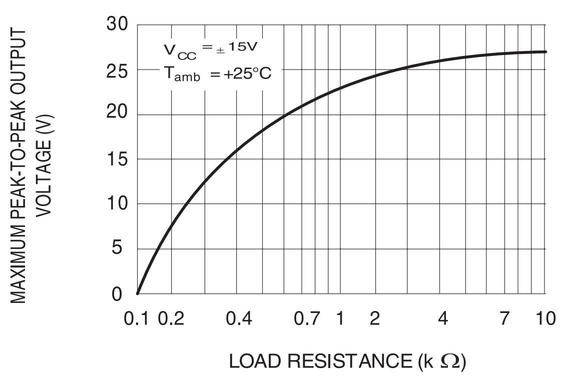


Figure 7. Maximum peak-to-peak output voltage versus supply voltage

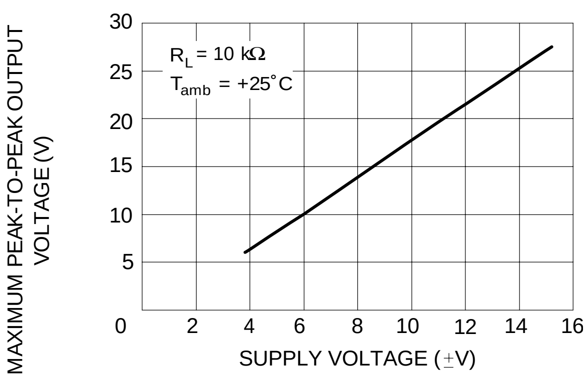


Figure 8. Input bias current versus free air temperature

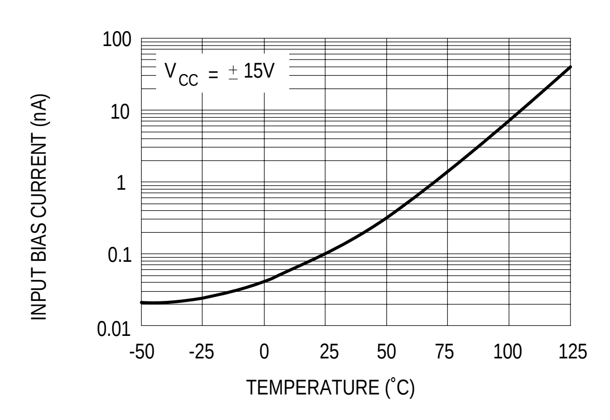


Figure 9. Large signal differential voltage amplification versus free air temp

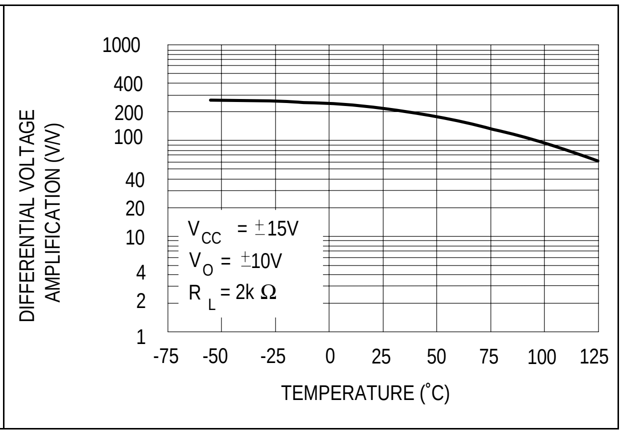


Figure 10. Large signal differential voltage amplification and phase shift versus frequency

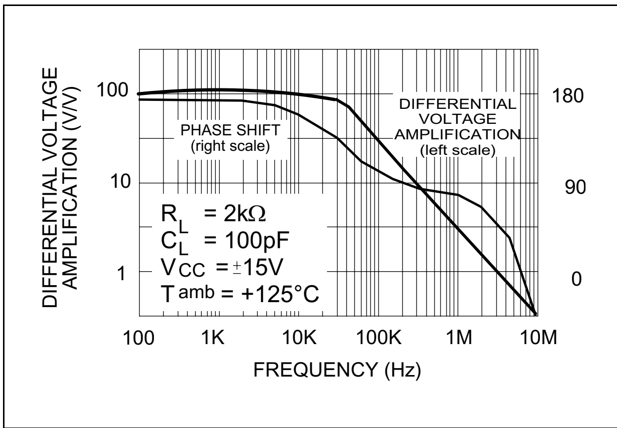


Figure 11. Total power dissipation versus free air temperature

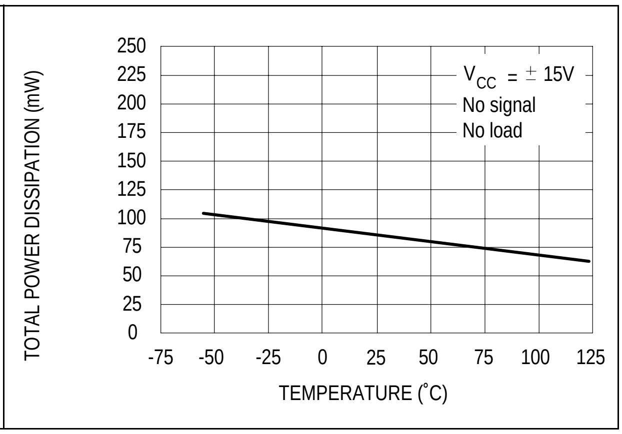


Figure 12. Supply current per amplifier versus free air temperature

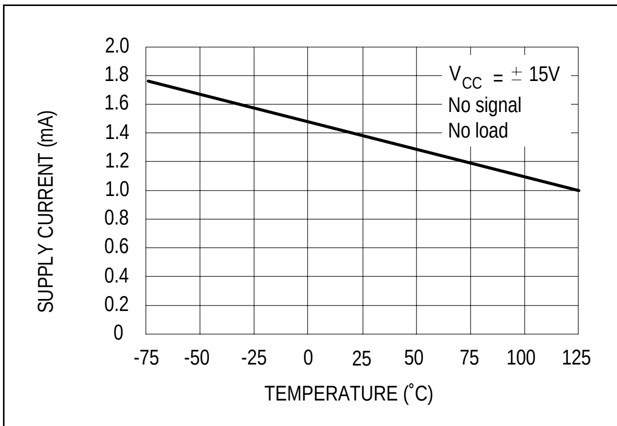


Figure 13. Common mode rejection ratio versus free air temperature

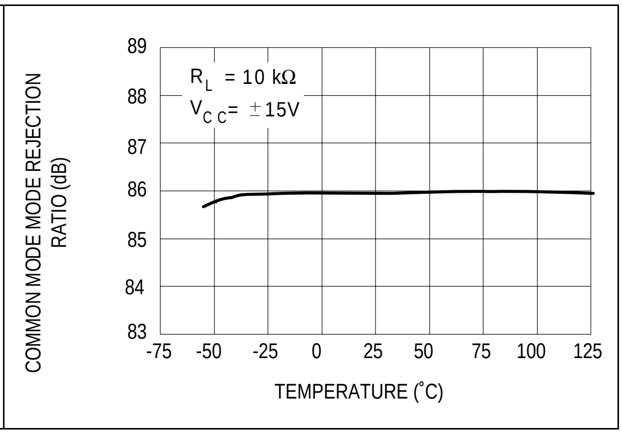


Figure 14. Voltage follower large signal pulse response

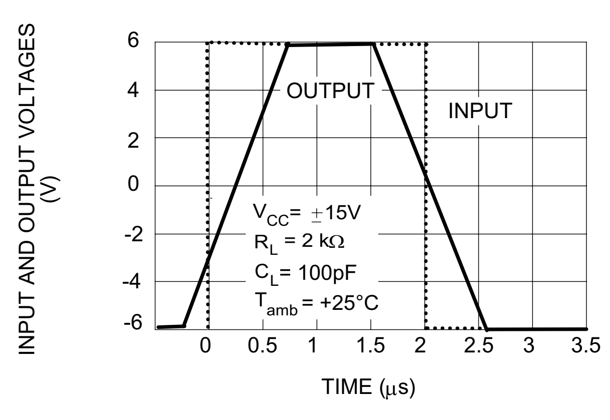


Figure 15. Output voltage versus elapsed time

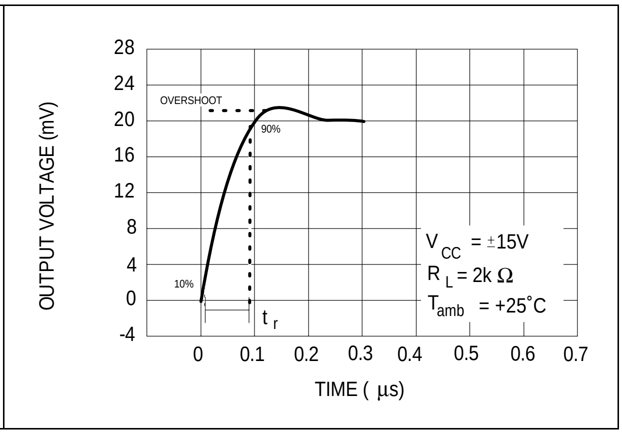


Figure 16. Equivalent input noise voltage versus frequency

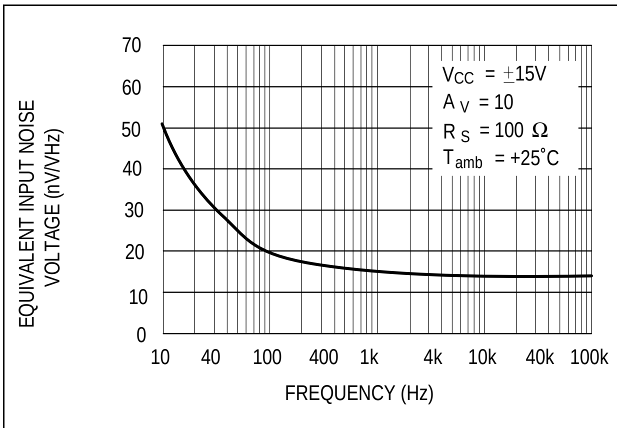
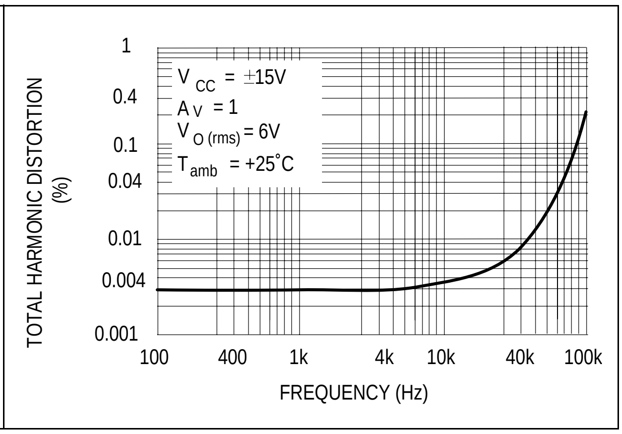


Figure 17. Total harmonic distortion versus frequency



4 Parameter measurement information

Figure 18. Voltage follower

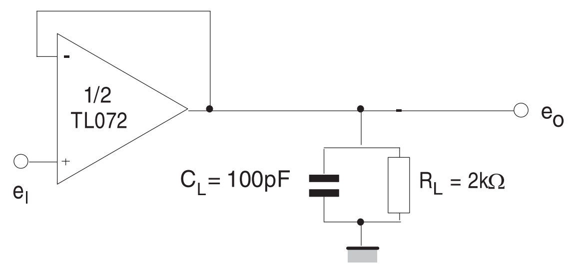
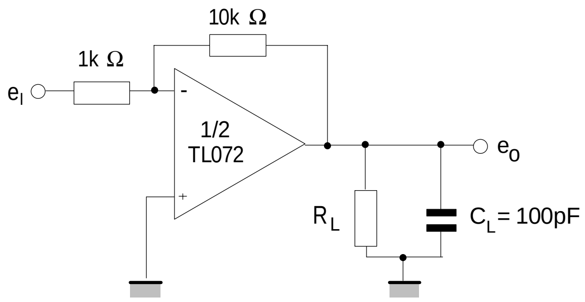
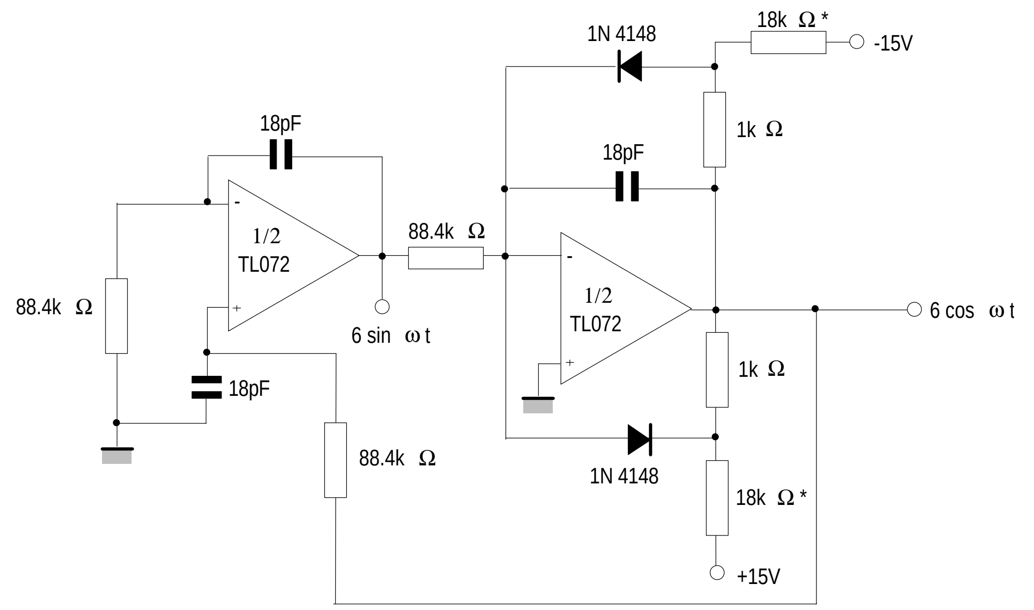


Figure 19. Gain-of-10 inverting amplifier



5 Typical application

Figure 20. 100kHz quadruple oscillator



* These resistor values may be adjusted for a symmetrical output

6 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

6.1 DIP8 package information

Figure 21. DIP8 package mechanical drawing

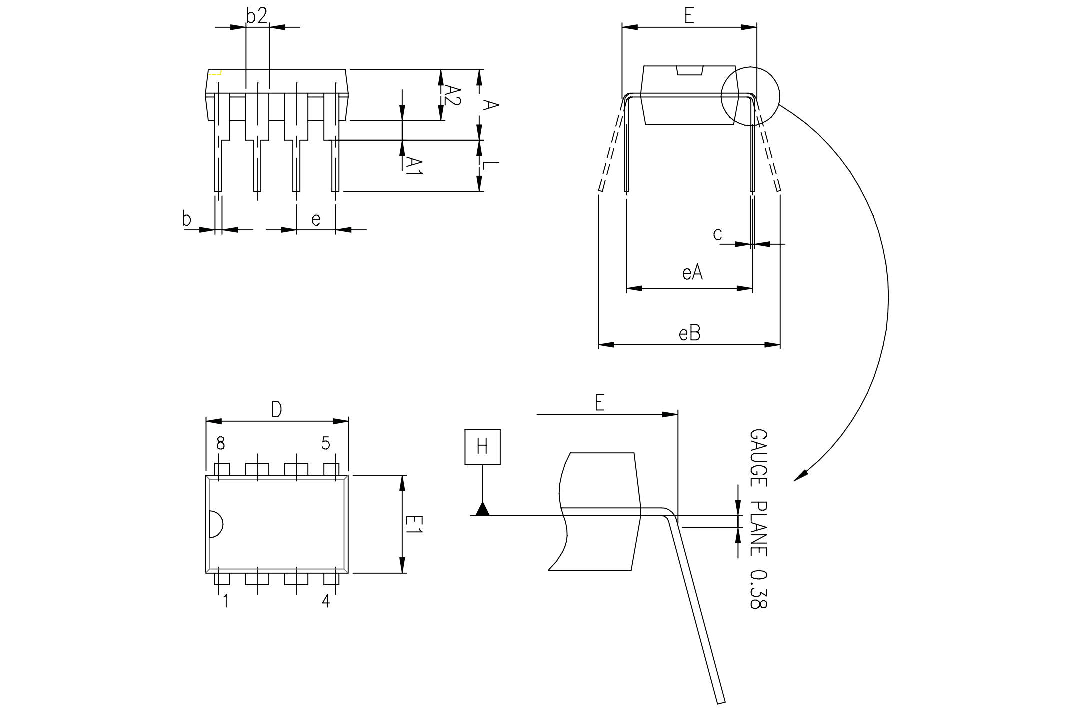


Table 4. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

6.2 SO-8 package information

Figure 22. SO-8 package mechanical drawing

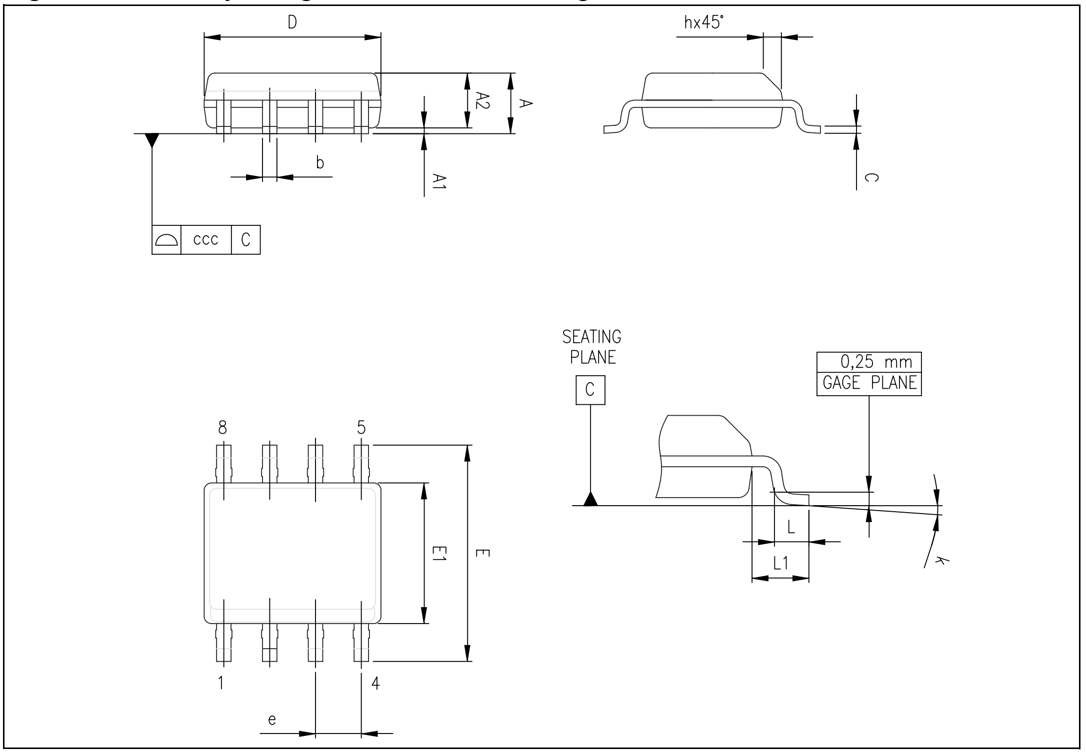


Table 5. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

7 Ordering information

Table 6. Order codes

Order code	Temperature range	Package	Packing	Marking
TL072MN	-55°C, + 125°C	DIP8	Tube	TL072MN
TL072AMN				TL072AMN
TL072BMN				TL072BMN
TL072MD/MDT		SO-8	Tube or tape & reel	072M
TL072AMD/AMDT				072AM
TL072BMD/BMDT				072BM
TL072IN	-40°C, +105°C	DIP8	Tube	TL072IN
TL072AIN				TL072AIN
TL072BIN				TL072BIN
TL072ID/IDT		SO-8	Tube or tape & reel	072I
TL072AID/AIDT				072AI
TL072BID/BIDT				072BI
TL072CN	0°C, +70°C	DIP8	Tube	TL072CN
TL072ACN				TL072ACN
TL072BCN				TL072BCN
TL072CD/CDT		SO-8	Tube or tape & reel	072C
TL072ACD/ACDT				072AC
TL072BCD/BCDT				072BC
TL072IYDT(1)	-40°C, +105°C	SO-8 (Automotive grade)	Tube or tape & reel	072IY

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
28-Mar-2001	1	Initial release.
02-Apr-2004	2	Correction to pin connection diagram on cover page. Unpublished.
04-Dec-2006	3	Modified graphics in package mechanical data.
06-Mar-2007	4	Expanded order codes table and added automotive grade order codes. See *Table 6 on page 14*. Added thermal resistance and ESD tolerance in *Table 1 on page 3*. Added *Table 2: Operating conditions on page 3*. Updated package mechanical data to make it compliant with the latest JEDEC standards.
13-Mar-2008	5	ESD HBM value modified in AMR table. Re-ordered order codes table. Removed TLO72BIY and TSO72AIY order codes from order code table. Corrected footnote for automotive grade order codes in order codes table.

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