IMISC492 SYSTEM CLOCK CHIP

March 15, 1995
Preliminary

CMOS LSI
PLL FREQUENCY SYNTHESIZER

PRODUCT FEATURES

- Supports Pentium™ asynchronous PCI system board designs
- Integrates system clocks and distribution buffers
- Operates from 5V or 3.3V supply
- Separate B1 buffer VDD supports mixed 5V/3.3V outputs
- Doze and 100µA power down low power operating modes
- 60 mA buffer switching current
- 28 Pin SSOP package for minimum board space

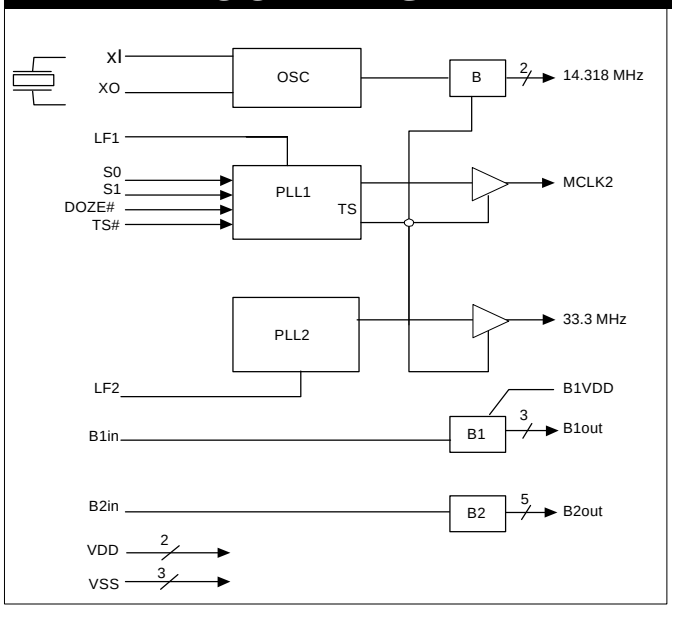
PRODUCT DESCRIPTION

The IMISC492 provides the clocks and the low skew distribution buffers required to drive the Pentium™ CPU and PCI busses. The doze control supports green PC applications by smoothly transitioning the CPU clock to it's minimum operating frequency. Power down and output tristate are rovided by the TS# input. Large buffer drive is provided to handle multiple loads.

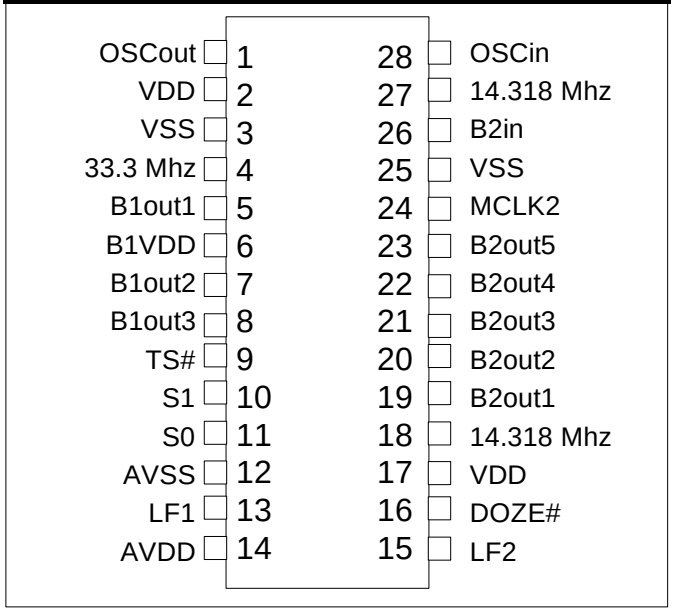
FREQUENCY TABLE

S1	S0	MCLK2	
		DOZE# = 1	DOZE# = 0
0	0	66.6	33.3
0	1	50	33.3
1	0	60	33.3
1	1	40	33.3

BLOCK DIAGRAM



CONNECTION DIAGRAM



INTERNATIONAL MICROCIRCUITS, INC. 525 LOS COCHES ST.
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PIN DESCRIPTION

OSCin, OSCout - These pins form an on-chip reference oscillator when conected to terminals of an external parallel resonant crystal (nominally 14.318 Mhz). OSCin may also serve as input for an externally generated reference signal.

S0 and S1 - Standard frequency select inputs. These inputs control the high speed MCLK frequency selection. All these inputs have internal pull-ups. MCLK switches smoothly to changes in these inputs.

The output frequency selection is shown on page 1.

MCLK2 - aster clock output. Programmable output frequencies can be selected using S0-S1 inputs.

DOZE# - DOZE control pin. When DOZE# is high, the clock chip oeprates in the standard mode. When this pin goes low output frequencies are switched to the preprogrammed DOZE frequencies. Switching to DOZE frequencies occurs smoothly to allow tracking by CPU internal PLL. This pin has an internall pull-up.

B2in - ON-chip buffer input. This is a CMOS input that switches at VDD/2. This pin has an internall pull-up.

B1out - Buffered outputs of B1 buffer. Switching current and output high level voltage controlled by B1VDD.

B2out - Buffered outputs of B2 buffer. Switching current and output high level controlled by VDD.

33 Mhz - PCI Clock Output

TS# - Logic low on this input tristates all clock and B1 buffer outputs if S1 = S0 = logic high. PLL's and OSC are stopped to reduce power and all circuitry is reset. Other states of S1 and S0 put circuit in a test mode. This pin has an internall pull-up.

14.318 Mhz - 14.318 Mhz output. Buffered output of on-chip reference oscillator or externally provided reference.

LF1 and LF2 - These are the phase detector outputs for the clock generators. They are single-ended, tristate output for use as loop error signal. A 0.1µF capcaitor to ground should be connected from this pin to form the loop filter. Grounding LF puts PLL in low power mode.

VSS - Circuit ground.

VDD - Positive power supply.

AVSS - Analog circuit ground.

AVDD - Analog positive power suppy.

B1VDD - 3.3v/5V logic level control for B1 buffer.

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 6V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65˚C to +150˚
Ambient Temperature:	-55˚C to +125˚C
Recommended Operating Range:	3V-6V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric filed; hodwever, precautions should be taken to avoid application of any vltage higher than the maximum rated voltages to this circuit. For proper operation, Vin anv Vout should be constrained to the range:

VSS < (Vin or Vout) < VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	V_{IL}	-	-	0.8	Vdc	-
Input High Voltage	V_{IH}	2.0	-	-	Vdc	TS#, DOZE#, and S0-S1 Inputs
Input High Voltage	V_{IH}	0.7VDD	-	-	Vdc	B1in and B2in Inputs
Input Low Current With Pull-up or Pull-down	I_{IL}	-	-	5 ±50	µA	TS#, B1in and B2in, DOZE#, and S0-S2 Inputs
Input High current With Pull-up or Pull-down	I_{IH}	-	-	5 ±50	µA	TS#, B1in and B2in, DOZE#, and S0-S2 Inputs
Output Low Voltage IOH=6mA	V_{OL}	-	-	0.4	Vdc	All Outputs
Output High Voltage IOH=6mA	V_{OH}	2.4	-	-	Vdc	All Outputs
Tri-State leakage Current	I_{OZ}	-	-	10	µA	LF1 and LF2
Dynamic Supply Current	I_{CC}	-	-	35*	mA	MCLK2 = 50 Mhz
Static Supply Current	I_{CC}(PD)	-	70	-	µA	TS# = Low, S1 = S0 = High
Short Circuit Current	I_{SC}	25	-	-	mA	-
						VDD = +3.1V to +5.5V, TA = 0 ˚C to + 70 ˚C

*For VDD = 5V ± 10% operation only.

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SWITCHING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Rise (0.8V - 2.0V) and Fall (2.0V-0.8V) time All Outputs	t_{TLH}, t_{THL}	-	-	1.5*	ns	15 pf Load
Output Duty cycle		-	45*	-	%	Measured at 1.5V
MCLK2 to B1out Propagation Delay	t_{PHLH1}, t_{PHL1}	-	3.0*	-	ns	15pf Load Measured at 1.5V
B2Buffer Propagation Delay Bin to Bout	t_{PLH2}, t_{PHL2}	-	4.7*	-	ns	15 pf load Measured at 1.5V
Buffer out Skew All B1 and B2 Buffer Outputs	t_{SKEW}	-	-	250	ps	15 pf Load Measured at 1.5V B1in = B2in
ΔPeriod Adjacent cycles MCLK2	ΔP	-	± 200	-	ps	-
Jitter Absolute MCLK2	T_{jab}	-	± 200	-	ps	-
Input Rise/Fall Time S0-S1		-	-	2	µs	-
Switching Current Low	I_{OL}(AC)*	-	60*	-	mA	VOL = 1.5V
Switching Current High	I_{OH}(AC)*	-	50*	-	mA	VOL = 1.5V

VDD = +3.1V to +5.5V, TA = 0 ˚C to + 70 ˚C

OSCILLATOR CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Transconductance	g_m	20	330	-	millimhos	@ 14.3 Mhz
Output Impedance	Z_o	-	200	800	ohms	@ 14.3 Mhz
Input Capacitance	Ci	8	13	18	pf	-
Output Capacitance	Co	3	6	9	pf	-
DC Bias Voltage	V_B	-	VDD/2	-	Volt	-
Start-up Time	ts	-	-	10	ms	@ 14.3 Mhz
Input Rise Time OSCin	ICLKr	-	-	2	µs	-
Input Fall Time OSCout	ICLKf	-	-	2	µs	-

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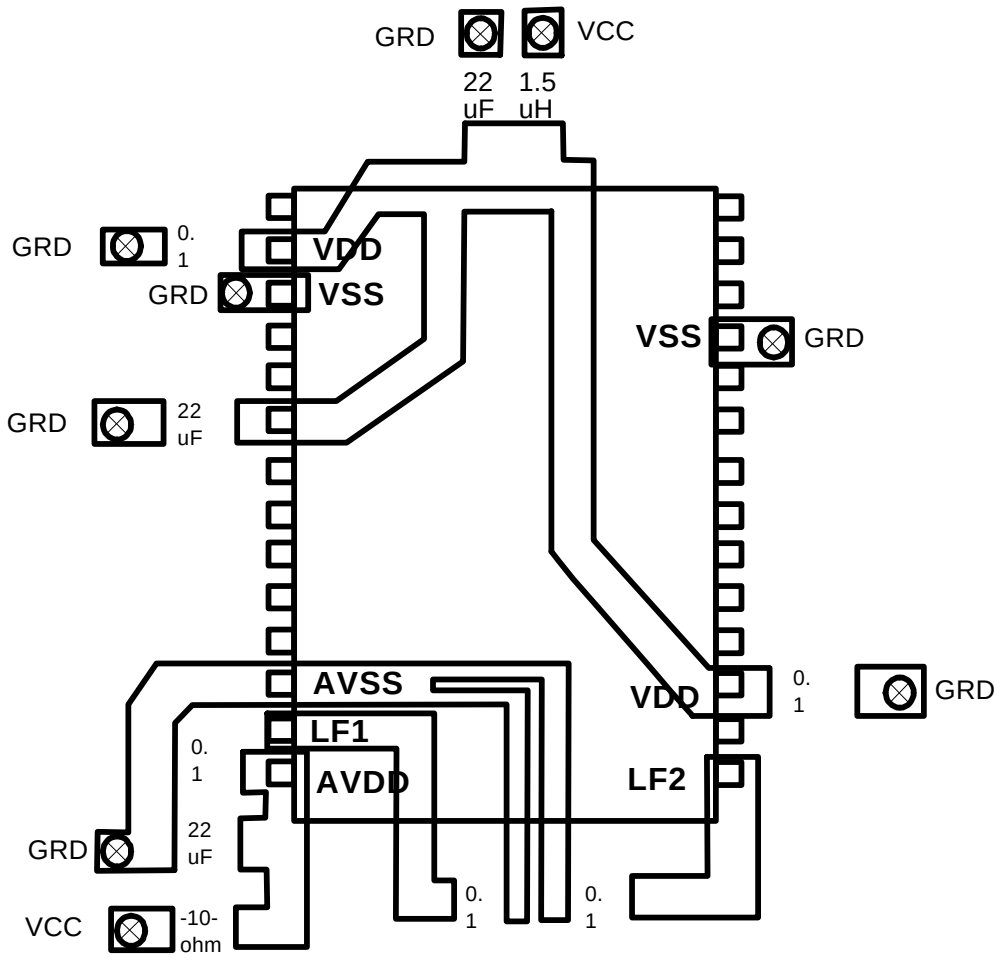
APPLICATION SUGGESTION



NOTES

1) LF cap must be connected to AVSS pin, not ground plane. Its connection should not be in the path of current flow from AVSS to GRD.
2) Power supply bypass cap (0.1uF) must be positioned close to VDD pins to be effective.
3) Topy layer traces and filtering to AVDD/AGRD separated from traces to VDD/VSS produce the best performance for IMI clock generators.
4) LF caps must be low leakage, such as multilayer ceramic Z5U or X7R material.
5) Pin 6 connection changes when mixed 5V/3.3V operation is required.

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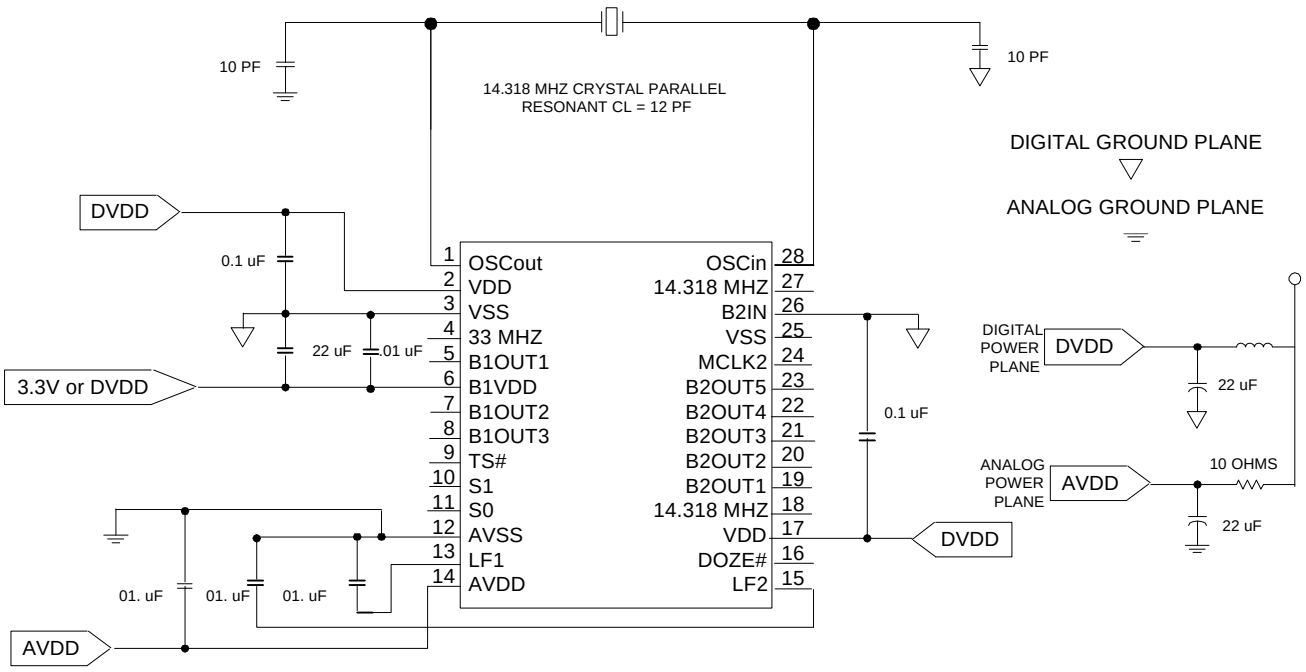
NOTE 1: Connect Analog Ground to digital Ground through one pont only on PC board.
NOTE 2: Caps connected to pins 6, 14, and 17 should be close to their pins.
NOTE 3: Caps on pins 13 and 15 should be connected to AVSS independent of the trace between AVSS and system ground.
NOTE 4: If VDD at clock generator ramps up more than 100MV DC within a 5 US time period (from turning disk drive off, etc.), the values of the DVDD and AVDD filter components should be increased.



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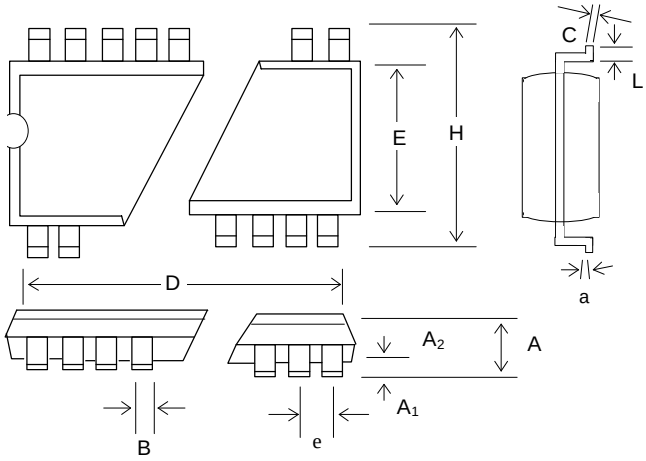
PACKAGE DRAWING AND DIMENSIONS



28 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.068	0.073	0.078	1.73	1.86	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.01	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.397	0.402	0.407	10.07	10.20	10.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

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ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMISC492xXB	28 PIN SSOP	Commerical, 0°C to + 70°C

NOTE: The “x” following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: IMI
SC492xYB
Date Code
Lot #

IMISC492xYB

Flow

B = Commercial, 0°C to + 70°C

Package

Y = SSOP

Revision

IMI Device Number