Am27F010

131,072 x 8—Bit CMOS Windowless EPROM

Advanced
Micro
Devices

DISTINCTIVE CHARACTERISTICS

- **Flasherase™ Electrical Bulk Chip-Erase**
  — One Second Typical Chip-Erase

- **Compatible with JEDEC Standard Byte Wide EPROM Pinouts**
  — 32-pin DIP
  — 32-pin PLCC

- **Flashrite™ Programming**
  — 10µS Typical Byte-Program
  — Less than 2 Second Typical Chip Program

- **Advanced CMOS Technology**
  — EPROM Compatible Process
  — Extensive Manufacturing Experience

- **100 Program/Erase Cycles**

- **Low Power Consumption**
  — 30mA Maximum Active Current
  — 100µA Maximum Standby Current

- **Command Register Architecture for Microprocessor/Micro-controller Compatible Write Interface**

- **Program and Erase Voltage**
  12.75V ± 0.25V V_{PP}

- **High Performance**
  — 120nS Maximum Access Time

- **Allows for Auto-Insertion**

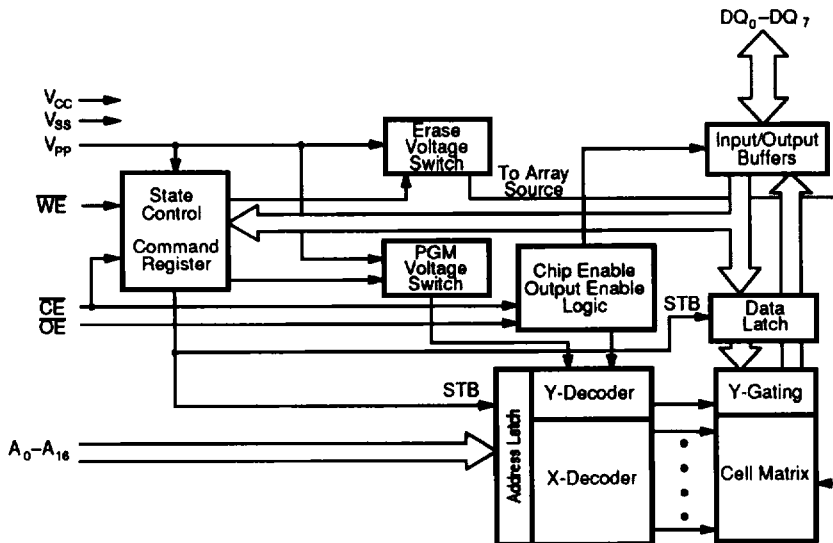- **5V ±10% Single Power Supply**

GENERAL DESCRIPTION

The Am27F010 CMOS windowless EPROM provides the industry's highest performance and most cost-effective alternative for reprogrammable non-volatile memory. It is organized as 128K bytes of 8 bits each. The Am27F010 is pin compatible with the 32 pin byte-wide JEDEC 1MEG EPROM. The 27F010 is targeted for alterable code- or data-storage applications were ultraviolet erasure is impractical or time consuming. The windowless EPROM adds electrical Flash chip-erasure

and reprogramming to AMD's EPROM technology. The device may be packaged in plastic and is ideal for use in auto-insertion manufacturing systems. The entire memory content may be erased and reprogrammed using AMD's Flasherase™ and Flashrite™ programming algorithm respectively in a standard PROM programmer. Electrical erasure increases the memory's flexibility, while providing time savings over traditional UV erasing.
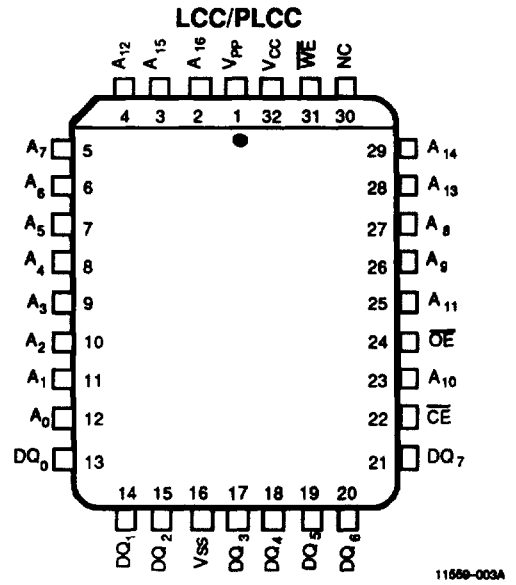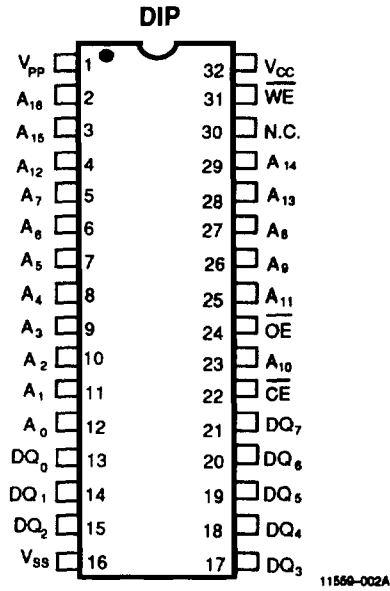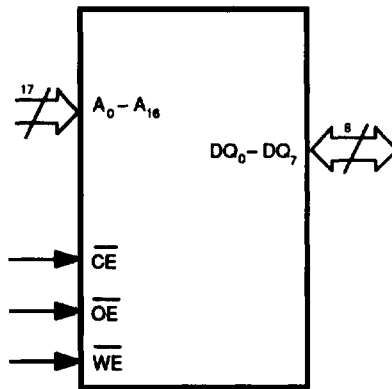
BLOCK DIAGRAM

11559-001A

CONNECTION DIAGRAMS

DIP

V_{PP}	1		32	V_{CC}
A_{16}	2		31	$\overline{WE}$
A_{15}	3		30	N.C.
A_{12}	4		29	A_{14}
A_7	5		28	A_{13}
A_6	6		27	A_8
A_5	7		26	A_9
A_4	8		25	A_{11}
A_3	9		24	$\overline{OE}$
A_2	10		23	A_{10}
A_1	11		22	$\overline{CE}$
A_0	12		21	DQ_7
DQ_0	13		20	DQ_6
DQ_1	14		19	DQ_5
DQ_2	15		18	DQ_4
V_{SS}	16		17	DQ_3

11559-002A

LCC/PLCC

11559-003A

LOGIC SYMBOL

11559-004A

FUNCTIONAL DESCRIPTION

In-circuit electrical erase and reprogramming increases flash memory's flexibility over EPROM. Standard PROM programmers may be used for erasing and programming. A command register in the windowless EPROM manages the electrical erasure and reprogramming. The command register architecture allows for fixed power supplies during erasure and programming, does not require high voltage on control pins, and provides maximum EPROM compatibility.

Read Mode

The windowless EPROM device functions as a read only memory when high voltage is not applied to the V_{pp} pin. In this mode the external memory control pins produce the standard EPROM read, standby, output disable, and Auto-select modes.

Programming/Read Mode

High voltage on the V_{pp} pin enables erasure and programming of the device. The same EPROM read, standby, and output disable functions are available when high voltage is applied to the V_{pp} pin. All functions associated with altering memory contents (erase, erase-verify, program, and program-verify) are accessed via the command register.

Standard microprocessor write timing is used to write commands into the register. Register contents serve as input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for programming or erase operations. Standard microprocessor read timings are used to access array data, access data for erase and program verification, or access the Auto-select modes.

The command register is alterable only when high voltage is applied to V_{pp}. When high voltage is removed, the contents of the register default to the read command. The device then functions as a read only memory.

Performance

AMD's windowless EPROMs offer access times of 120ns which allows operation of high-speed microprocessors and microcontrollers without wait-states. The windowless EPROM architecture supports separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls in order to eliminate bus contention.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_c)   0°C to +70°C
Industrial (I) Devices
Case Temperature (T_c)   −40°C to +85°C
Extended Commercial (E) Devices
Case Temperature (T_c)   −55°C to +125°C
Military (M) Devices
Case Temperature (T_c)   −55°C to +125°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

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