ANALOG DEVICES

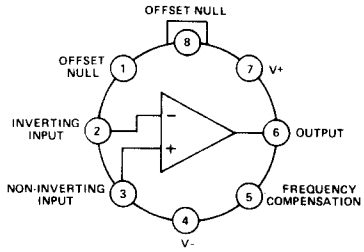
High Accuracy IC Operational Amplifier

AD504

4

FEATURES
Low V_{OS}: 500μV max (AD504M)
High Gain: 10^6 min (AD504L, M, S)
Low Drift: 0.5μV/°C max (AD504M)
Free of Popcorn Noise

AD504 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The Analog Devices AD504J, K, L, M and S IC operational amplifiers provide ultra-low drift and extremely high gain, comparable to that of modular amplifiers, for precision applications. A new double integrator circuit concept combined with a precise thermally balanced layout achieves gain greater than 10^6, offset voltage drift of less than 1μV/°C, small signal unity gain bandwidth of 300kHz, and slew rate of 0.12V/μs. Because of monolithic construction, the cost of the AD504 is significantly below that of modules, and becomes even lower with larger quantity requirements. The amplifier is externally compensated for unity gain with a single 470pF capacitor; no compensation is required for gains above 500. The inputs are fully protected, which permits differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits to ground and/or either supply voltage, and is capable of driving 1000pF of load capacitance. The AD504J, K, L and M are supplied in the hermetically sealed TO-99 package, and are specified for operation over the 0 to +70°C temperature range. The AD504S is specified over the -55°C to +125°C temperature range and is also supplied in the TO-99 package.

PRODUCT HIGHLIGHTS

1. Fully guaranteed and 100% tested 1μV/°C maximum voltage drift combined with voltage offset of 500μV (AD504L).
2. Fully protected input ($\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, and is of critical importance in this type of device whose overall performance is strongly dependent upon front-end stability.
3. Single capacitor compensation eliminates elaborate stabilizing networks while providing flexibility not possible with an internally compensated op amp. This feature allows bandwidth to be optimized by the user for his particular application.
4. High gain is maintained independent of offset nulling, power supply voltage and load resistance.
5. Bootstrapping of the critical input transistor quad produces CMRR and PSRR compatible with the tight 1μV/°C drift. CMRR and PSRR are both in the vicinity of 120dB.
6. Noise performance is closely monitored at Outgoing QC to ensure compatibility with the low error budgets afforded by the performance of all other parameters.
7. Every AD504 receives a stabilization bake for 24 hours at 150°C to ensure reliability and long term stability.
8. The 100 piece price of the AD504 is 1/3 to 1/2 less than that of modular low drift operational amplifiers, and is competitive with the price of less accurate IC op amps.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

PARAMETER	AD504J	AD504K	AD504L
OPEN LOOP GAIN			
V_{OS} = ±10V, $R_L \geq 2k\Omega$	250,000 min (4 x 10^6 typ)	500,000 min (4 x 10^6 typ)	10^6 min (8 x 10^6 typ)
$T_{min} \leq T_A \leq T_{max}$	125,000 min (10^6 typ)	250,000 min (10^6 typ)	500,000 min (10^6 typ)
OUTPUT CHARACTERISTICS			
Voltage at $R_L \geq 2k\Omega$, $T_{min} \leq T_A \leq T_{max}$	±10V min (±13V typ)	*	*
Load Capacitance	1000pF	*	*
Output Current	10mA min	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal, C_c = 390pF	300kHz	*	*
Full Power Response, C_c = 390pF	1.5kHz	*	*
Slew Rate, Unity Gain, C_c = 390pF	0.12V/μs	*	*
INPUT OFFSET VOLTAGE			
Initial Offset, $R_S \leq 10k$	2.5mV max (0.5mV typ)	1.5mV max (0.5mV typ)	0.5mV max (0.2mV typ)
vs Temp, $T_{min} \leq T_A \leq T_{max}$, V_{OS} nulled	5.0μV/°C max (0.5μV/°C typ)	3.0μV/°C max (0.5μV/°C typ)	1.0μV/°C max (0.3μV/°C typ)
$T_{min} \leq T_A \leq T_{max}$, V_{OS} unnulled†	10μV/°C max (1.5μV/°C typ)	5.0μV/°C max (1.5μV/°C typ)	2.0μV/°C max (1.0μV/°C typ)
vs Supply	25μV/V max	15μV/V max	10μV/V max
@ $T_{min} \leq T_A \leq T_{max}$	40μV/V	25μV/V max	15μV/V max
vs Time	20μV/mo	15μV/mo	10μV/mo
INPUT OFFSET CURRENT			
@ T_A = 25°C	40nA max	15nA max	10nA max
INPUT BIAS CURRENT			
Initial	200nA max	100nA max	80nA max
T_{min} to T_{max}	300nA max	150nA max	100nA max
vs Temp, T_{min} to T_{max}	300pA/°C	250pA/°C	200pA/°C
INPUT IMPEDANCE			
Differential	0.5MΩ	1.0MΩ	1.3MΩ
Common Mode	100MΩ‖4pF	*	*
INPUT NOISE			
Voltage, 0.1 to 10Hz	1.0μV (p-p)	*	*
100Hz	10nV/$\sqrt{Hz}$(rms)	*	*
1kHz	8nV/$\sqrt{Hz}$(rms)	*	*
Current, 0.1 to 10Hz	50pA(p-p)	*	*
100Hz	0.6pA/$\sqrt{Hz}$(rms)	*	*
1kHz	0.5pA/$\sqrt{Hz}$(rms)	*	*
INPUT VOLTAGE RANGE			
Differential or Common Mode, Max Safe	$\pm V_S$	*	*
Common Mode Rejection, V_{IN} = ±10V	94dB min (120dB typ)	100dB min (120dB typ)	110dB min (120dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Current, Quiescent	±4.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)
TEMPERATURE RANGE			
Operating, Rated Performance (T_{min} to T_{max})	0 to +70°C	*	*
Storage	-65°C to +150°C	*	*
PACKAGE OPTION:[1] TO-99 Style (H08B)	AD504JH	AD504KH	AD504LH

NOTES
*Specifications same as for AD504J.
[1] See Section 19 for package outline information.

Specifications subject to change without notice.

NOTE
Analog Devices 100% tests and guarantees all specified maximum and minimum limits. Certain parameters, because of the relative difficulty and cost of 100% testing, have been specified as "typical" numbers. At ADI, "typical" numbers are subjected to rigid statistical sampling and outgoing quality control procedures, resulting in "typicals" that are indicative of the performance that can be expected by the user.

AD504M	AD504S(AD504S/883)
10^6 min (8 x 10^6 typ) 500,000 min (10^6 typ)	10^6 min (8 x 10^6 typ) 250,000 min
• • • •	• • • •
• • •	• • •
0.5mV max (0.2mV typ) 0.5μV/°C max (0.2μV/°C typ) 1.0μV/°C max (0.5μV/°C typ) 10μV/V max 15μV/V max 10μV/mo	0.5mV max 1.0μV/°C max (0.3μV/°C typ) 2.0μV/°C max (1.0μV/°C typ) 10μV/V max 20μV/V max 10μV/mo
10nA max	10nA max
80nA max 100nA max 200pA/°C	80nA max 200nA max 200pA/°C
1.3MΩ •	1.3MΩ •
0.6μV (p-p) max 10nV/$\sqrt{Hz}$ max 9nV/$\sqrt{Hz}$ max 50pA p-p max 0.6pA/$\sqrt{Hz}$ max 0.3pA/$\sqrt{Hz}$ max	• • • • • •
• 110dB min (120dB typ)	• 110dB min (120dB typ)
• • ±3.0mA max (±1.5mA typ)	• • ±3mA max (±1.5mA typ)
• •	-55°C to +125°C -65°C to +150°C
AD504MH	AD504SH

OFFSET VOLTAGE DRIFT AND NULLING

Most differential operational amplifiers have provisions for adjusting the initial offset voltage to zero with an external trim potentiometer. It is often not realized that there is a resulting increase in voltage drift which accompanies this initial offset adjustment. The increased voltage drift can often be safely ignored in conventional amplifiers, since it may be a small percentage of the specified voltage drift. However, the voltage drift of the AD504 is so small that this effect cannot be ignored.

To achieve low drift over temperature, it is necessary to maintain equal current densities in the input pair. Unless the initial offset nulling circuit is carefully arranged, the nulling circuits will themselves drift with temperature. The resulting change in the input transistor current *ratio* will produce an additional input offset voltage drift. This drift component can actually be larger than the unnulled drift.

Typically, IC op amps are nulled by using an external potentiometer to adjust the ratio of two resistances. These resistances are part of a network from which the input stage emitter currents are derived. Most commercially available op amps use diffused resistors in their internal nulling circuitry, which typically display large positive temperature coefficients of the order of 2000ppm/°C. As a result of the failure of the external potentiometer resistance to track the diffused resistors over temperature, the two resistance branches will drift relative to one another. This will cause a change in the emitter current ratio and induce an offset drift with temperature.

In the AD504, this problem is reduced an order of magnitude by the use of thin film resistors deposited on the monolithic amplifier chip. These resistors, which make up the critical bias network from which the input stage emitter current balance is determined, display typical temperature coefficients of less than 200ppm/°C, an order of magnitude improvement over diffused types. Thus, when the initial offset of the AD504 is trimmed using a low TC pot in combination with the thin film network, the drift induced by nulling even relatively large offsets is extremely small. This means that AD504 units of all three grades (J, K, L) will typically yield significantly better temperature performance in nulled applications than an all-diffused amplifier with comparable initial offset.

Since the intrinsic offset drift of the amplifier is improved by nulling, the direct measurement of any additional drift induced by differing temperature coefficients of resistors would be extremely difficult. However, the *induced* offset drift can be established by calculating the change in the emitter current ratio brought about by the differing TC's of resistances. From the change in this ratio, the offset voltage contribution at any temperature can be easily calculated.

A simple computer program was written to calculate induced offset drift as a function of initial offset voltage nulled. This calculation was made assuming zero TC of the amplifier resistors, and TC's of 200ppm/°C and 2000ppm/°C for the null pot. These results are very nearly equivalent to the case where the pot has zero temperature coefficient and the amplifier resistors drift. The results of these calculations are summarized graphically in Figure 1.

Figure 1 shows the variation of induced voltage drift with nulled offset voltage for:

a. AD504 op amp.
b. 725 typ op amp.

Note that as a result of nulling 1.4mV of offset, *the AD504 induces 30X less offset drift (only 0.05μV/°C) than the 725 type op amp* with its actual diffused resistor values and the recommended 100k pot to trim the offset. Actual induced drifts from this source for the AD504 may be even lower in the practical case when metal film resistors or pots are used for nulling, since their TC's tend to closely *match* the negative TC's of the thin film resistors on the AD504 chip.

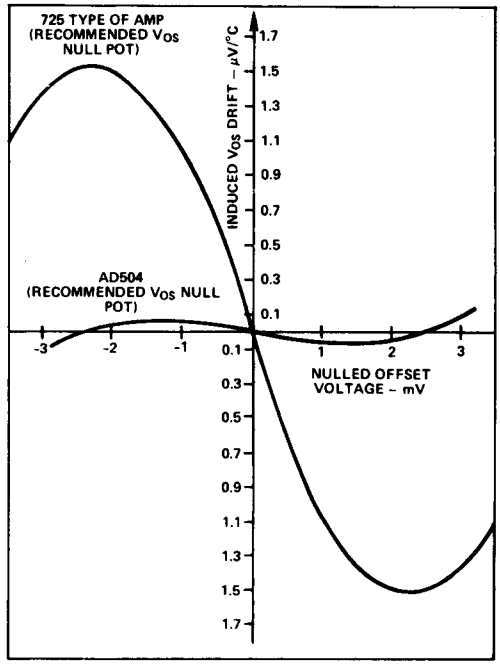


Figure 1. Induced Offset Drift vs. Nulled Offset Using Manufacturer's Recommended Adjustment Potentiometer

NULLING THE AD504

Since calculations show that superior drift performance can be realized with the AD504, special care should be taken to null it in the most advantageous manner. Using the actual values of resistors in the AD504, it is possible to calculate, under worst case conditions, that the total adjustment range of the AD504 is approximately 8mV. Since the amplifier may often be trimmed to within 1μV, this represents an adjustment of 1 part in 8000. This type of accuracy would require a pot with 0.0125% resolution and stability. Because of the problems of obtaining a pot of this stability, a slightly more sophisticated nulling operation is recommended for applications where offset drift is critical (see Figure 2a).

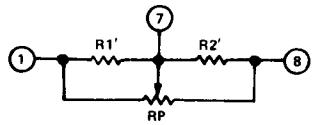


Figure 2a. High Resolution, High Stability Nulling Circuit

NULLING PROCEDURE

1. Null the offset to zero using a commercially available pot (suggest R_P = 10kΩ).
2. Measure pot halves R1 and R2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1},\ R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Insert R1′ and R2′ (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (R_P) to fine tune the trim.

For applications in which stringent nulling is not required, the user may choose a simplified nulling scheme as shown in Figure 2b. For best results the wiper of the potentiometer should be connected directly to pin 7 of the op amp. This is true for both nulling schemes.

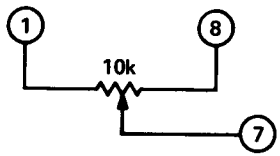


Figure 2b. Simplified Nulling Circuit

INPUT BIAS CURRENT

The input bias current vs. temperature characteristic is displayed in Figure 3.

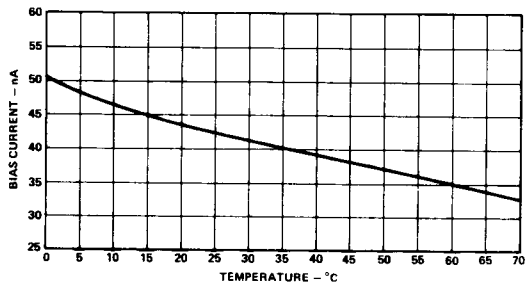


Figure 3. Input Bias Current vs. Temperature

GAIN PERFORMANCE

Most commercially available monolithic op amps have gain characteristics that vary considerably with:

1. Offset Nulling.
2. Load Resistance.
3. Supply Voltage.

Careful design allows the AD504 to maintain gain well in excess of 10^6, independent of nulling, load or supply voltage.

Nulling – The gain of a 741 op amp varies considerably with nulling (see Figure 4).

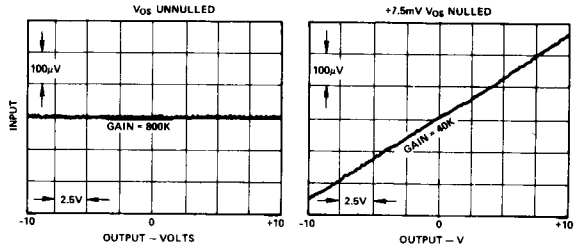


Figure 4. Gain Error Voltage Before and After Nulling a Typical 741 Op Amp

The gain of the AD504 is independent of nulling.

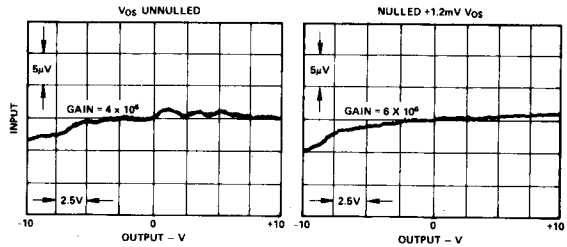


Figure 5. Gain Error Voltage Before and After Nulling the AD504

Load Resistance – The gain of the AD504 is flat with load resistance to 1kΩ loads and below.

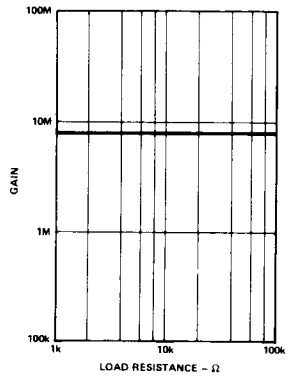


Figure 6. Gain vs. Load Resistance

Supply Voltage – The gain of the AD504 stays well above 1M down to V_S = ±5V.

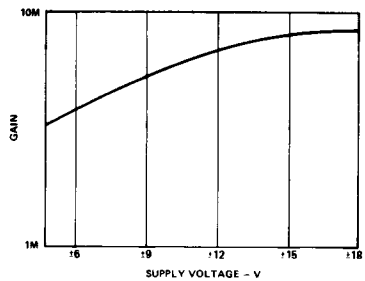


Figure 7. Gain vs. Supply Voltage

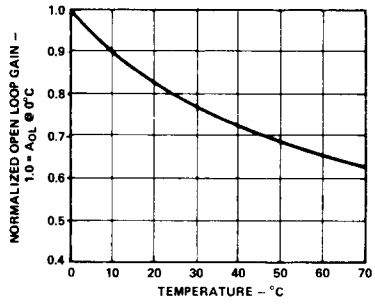


Figure 8. Normalized Open Loop Gain vs. Temperature

NOISE CHARACTERISTICS

An op amp with the precision of the AD504 must have correspondingly low noise levels if the user is to take advantage of its exceptional dc characteristics. Of primary importance in this type of amplifier is the absence of popcorn noise and minimum I/f or "flicker" noise in the 0.01Hz to 10Hz frequency band. Sample noise testing is done on every lot to guarantee that better than 90% of all devices will meet the noise specifications.

Separate voltage and current noise levels referred to the input are specified to enable the designer to calculate or optimize signal-to-noise ratio based on any desired source resistance. The spot noise figures are useful in determining total wideband noise over any desired bandwidth (see Figure 9).

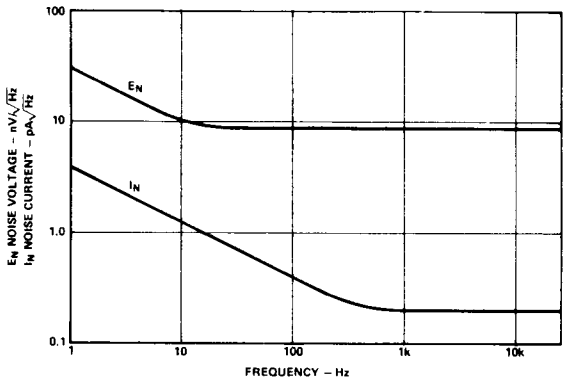


Figure 9. Spot Noise vs. Frequency

The key to success in using the AD504 in precision low noise applications is "attention to detail".

Here are a few reminders to help the user achieve optimum noise performance from the AD504.

1. Use metal film resistors in the source and feedback networks.
2. Use fixed resistors instead of potentiometers for nulling or gain setting.
3. Take advantage of the excellent common-mode noise rejection qualities of the AD504 by connecting the input differentially.
4. Limit the bandwidth of the system to the minimum possible consistent with the desired response time.
5. Use input guarding to reduce capacitive and leakage noise pickup.
6. Avoid ground loops and proximity to strong magnetic or electrostatic fields, etc.

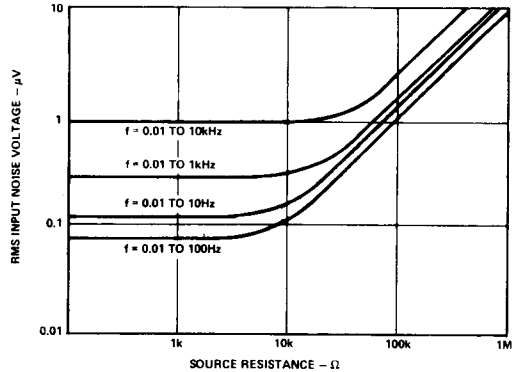


Figure 10. RMS Noise vs. Source Resistance

DYNAMIC PERFORMANCE

The dynamic performance of the AD504, although comparable to most general purpose op amps, is superior to most low drift op amps. Figure 11 shows the small signal frequency response for both open and closed loop gains for a variety of compensating values. Note that the circuit is completely stable for C_C = 390pF with a -3dB bandwidth of 300kHz; with C_C = 0, the -3dB bandwidth is 50kHz at a gain of 2000.

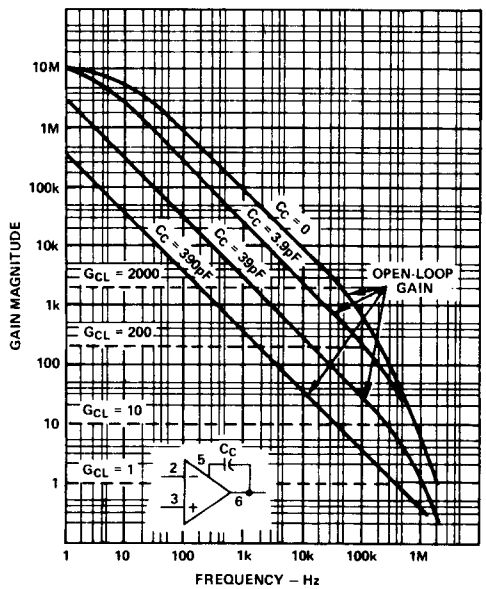


Figure 11. Small Signal Gain vs. Frequency

More important, at unity gain (390pF), full power bandwidth is (Figure 12) 2kHz which corresponds to a 0.12V/μs slew rate. At a gain of 10 (39pF), it increases to 20kHz, corresponding to 1.2V/μs, a considerable improvement over "725 type" amplifiers.

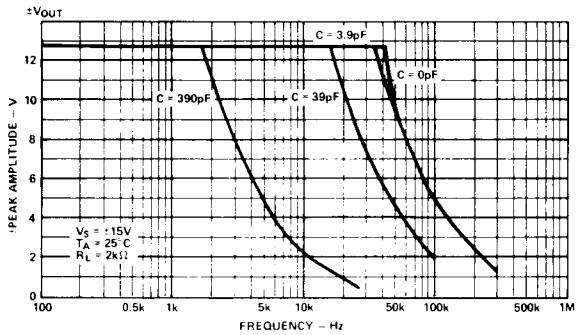


Figure 12. Output Voltage Swing vs. Frequency

Figure 13 shows the voltage follower step response for $V_S = \pm 15V$, $R_L = 2k\Omega$, $C_L = 200pF$ and $C_C = 390pF$.

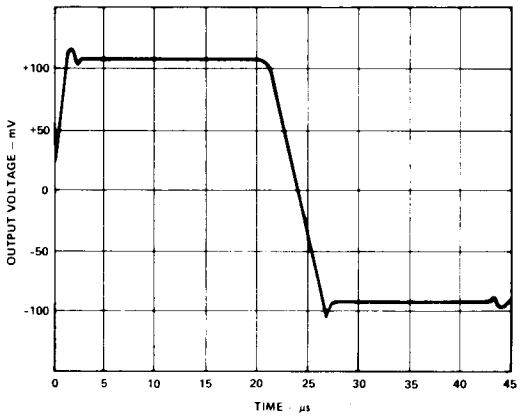


Figure 13. Voltage Follower Step Response

The common mode rejection of the AD504 is typically 120dB, and is shown as a function of frequency in Figure 14.

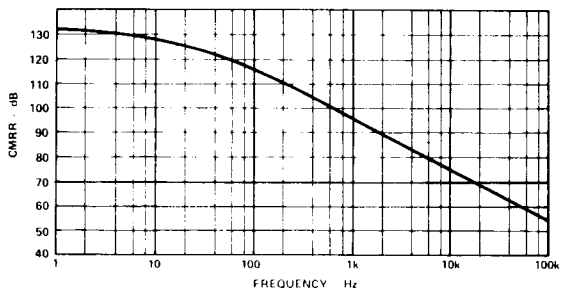


Figure 14. CMRR vs. Frequency

The power supply rejection ratio of the AD504 is shown in Figure 15.

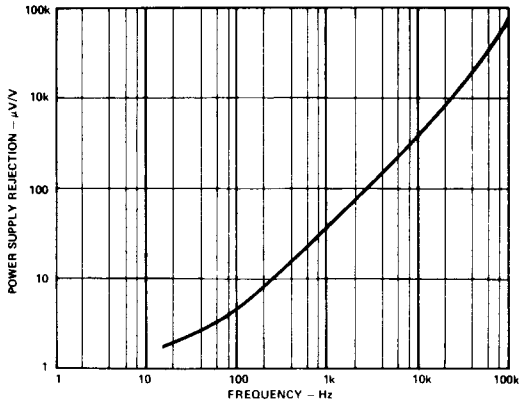


Figure 15. PSRR vs. Frequency

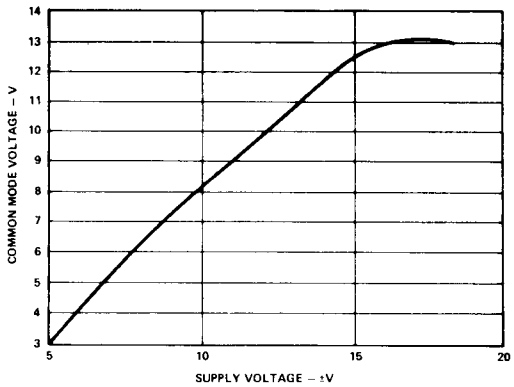


Figure 16. CMV Range vs. Supply Voltage

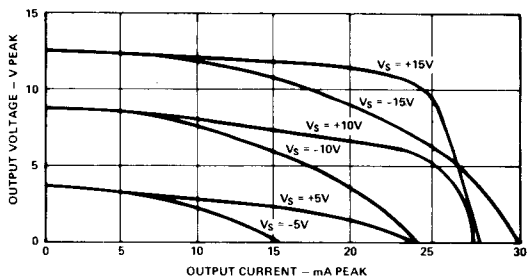


Figure 17. Output Characteristics

THERMAL PERFORMANCE

Temperature Gradients

Most modular and hybrid operational amplifiers are extremely sensitive to thermal gradients. The transient offset voltage response to thermal shock for a high performance modular op amp is shown in Figure 18.

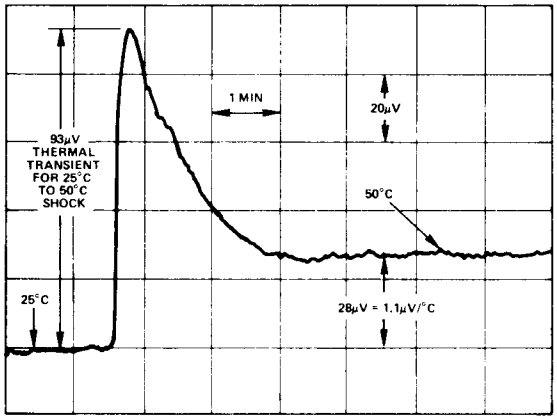


Figure 18. Response to Thermal Shock for High Performance Modular Op Amp

The graph shows the transient offset voltage resulting from a thermal shock when the amplifier's temperature is abruptly changed from 25°C to 50°C by dipping it into a hot silicon oil bath. Note the large overshoot (approximately 60μV) and long settling time (2.5 minutes). Also note the hysteresis of about 30μV.

Monolithic technology affords the AD504 significant improvements in this area. Thermal transients in the AD504 are small and over with quickly (see Figure 19).

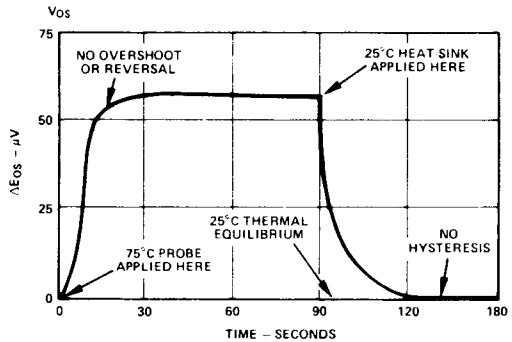


Figure 19. Response to Thermal Shock for AD504

In Figure 19, a 50°C step change in ambient temperature, applied to the can via a room temperature heat sink, then a 75°C thermal probe and back to the heat sink, results in settling to the final value within 30 seconds, for both increases and decreases in temperature. Note that the offset goes directly to its final value, with no spikes or hysteresis.

Warmup Drift

Modular and hybrid op amps have historically been plagued by excessive thermal time constants. Figure 20 shows the typical warmup drift of a high performance modular op amp.

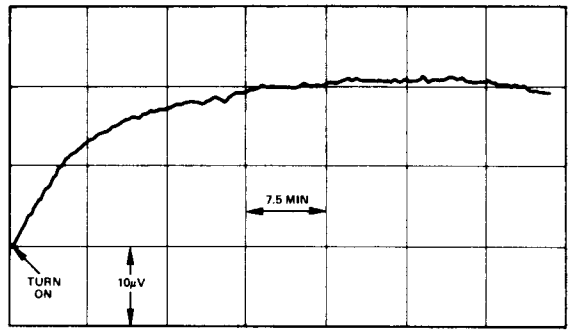


Figure 20. Warmup Voltage Drift for High Performance Modular Op Amp

Note that although warmup drift is low (20μV), it requires a long time to settle (>20 minutes).

Monolithic technology results in significant reduction of thermal time constants (see Figure 21).

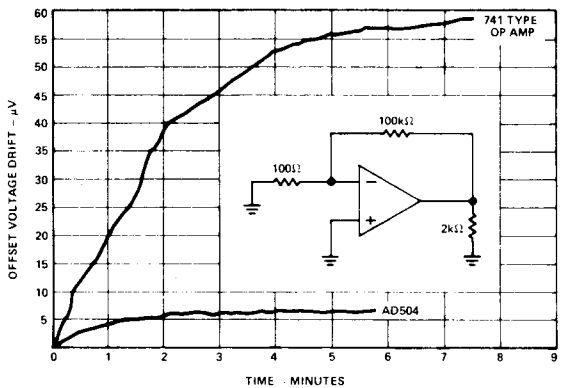


Figure 21. Warmup Voltage Drift for AD504 and 741 Type Op Amp

Note that warmup drift remains low (10μV), but that the thermal time constant decreases significantly to about 2 minutes. If a heat sink were used, total settling time would be completed within 30 seconds. Note that the 741 type op amp has a significantly longer warmup drift and thermal time constant.