



CD4027BM/CD4027BC Dual J-K Master/Slave Flip-Flop with Set and Reset

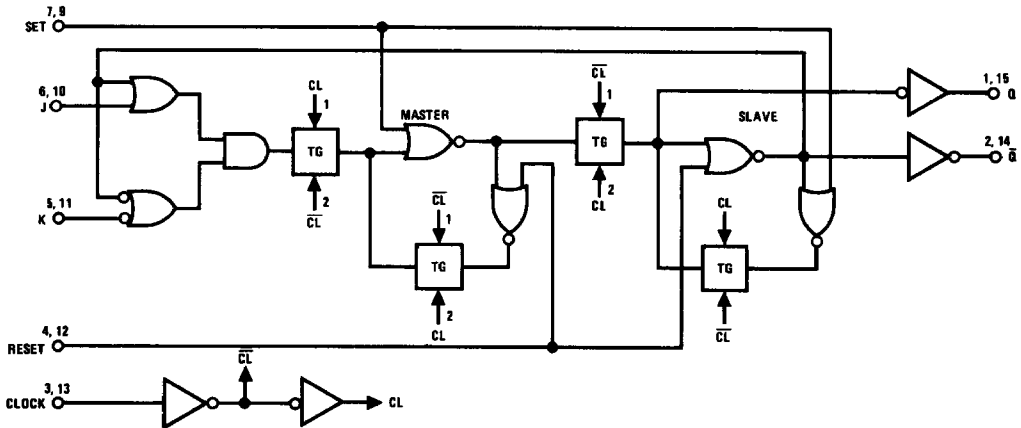
General Description

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset, and clock inputs and buffered Q and \bar{Q} outputs. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input. All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS} .

Features

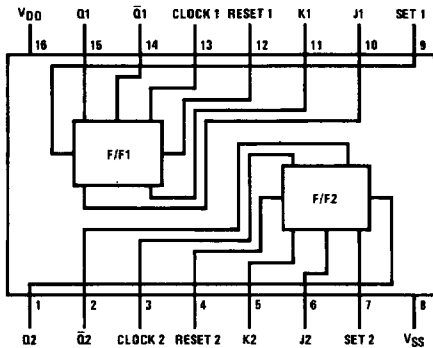
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility Fan out of 2 driving 74L or 1 driving 74LS
- Low power 50 nW (typ.)
- Medium speed operation 12 MHz (typ.) with 10V supply

Schematic and Connection Diagrams



TL/F/5958-1

Dual-In-Line Package



Top View

TL/F/5958-2

Order Number CD4027B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 V_{DC} to +18 V_{DC}
Input Voltage (V_{IN})	-0.5V to V_{DD} + 0.5 V_{DC}
Storage Temperature Range (T_S)	-65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4027BM	-55°C to +125°C
CD4027BC	-40°C to +85°C

DC Electrical Characteristics CD4027BM (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		1			1		30	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		2		2		60	μA	
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		4		4		120	μA	
V_{OL}	Low Level Output Voltage	$ I_O < 1 \mu A$ $V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$ I_O < 1 \mu A$ $V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or $9V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		-10^{-5}	-0.1		-1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4027BC (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I _{DD}	Quiescent Device Current	V _{DD} = 5V, V _{IN} = V _{DD} or V _{SS}		4			4		30	μA
		V _{DD} = 10V, V _{IN} = V _{DD} or V _{SS}		8			8		60	μA
		V _{DD} = 15V, V _{IN} = V _{DD} or V _{SS}		16			16		120	μA
V _{OL}	Low Level Output Voltage	I _O < 1 μA								
		V _{DD} = 5V		0.05		0	0.05		0.05	V
		V _{DD} = 10V		0.05		0	0.05		0.05	V
		V _{DD} = 15V		0.05		0	0.05		0.05	V
V _{OH}	High Level Output Voltage	I _O < 1 μA								
		V _{DD} = 5V	4.95		4.95	5		4.95		V
		V _{DD} = 10V	9.95		9.95	10		9.95		V
		V _{DD} = 15V	14.95		14.95	15		14.95		V
V _{IL}	Low Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V _{DD} = 10V, V _O = 1V or 9V		3.0			3.0		3.0	V
		V _{DD} = 15V, V _O = 1.5V or 13.5V		4.0			4.0		4.0	V
V _{IH}	High Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V _{DD} = 10V, V _O = 1V or 9V	7.0		7.0			7.0		V
		V _{DD} = 15V, V _O = 1.5V or 13.5V	11.0		11.0			11.0		V
I _{OL}	Low Level Output Current (Note 3)	V _{DD} = 5V, V _O = 0.4V	0.52		0.44	0.88		0.36		mA
		V _{DD} = 10V, V _O = 0.5V	1.3		1.1	2.25		0.9		mA
		V _{DD} = 15V, V _O = 1.5V	3.6		3.0	8.8		2.4		mA
I _{OH}	High Level Output Current (Note 3)	V _{DD} = 5V, V _O = 4.6V	-0.52		-0.44	-0.88		-0.36		mA
		V _{DD} = 10V, V _O = 9.5V	-1.3		-1.1	-2.25		-0.9		mA
		V _{DD} = 15V, V _O = 13.5V	-3.6		-3.0	-8.8		-2.4		mA
I _{IN}	Input Current	V _{DD} = 15V, V _{IN} = 0V		-0.3		-10 ⁻⁵	-0.3		-1.0	μA
		V _{DD} = 15V, V _{IN} = 15V		0.3		10 ⁻⁵	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics* $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $t_{rCL} = t_{fCL} = 20\text{ ns}$, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Clock to Q or \bar{Q}	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		200 80 65	400 160 130	ns ns ns
t_{PHL} or t_{PLH}	Propagation Delay Time from Set to \bar{Q} or Reset to Q	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		170 70 55	340 140 110	ns ns ns
t_{PHL} or t_{PLH}	Propagation Delay Time from Set to Q or Reset to \bar{Q}	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		110 50 40	220 100 80	ns ns ns
t_S	Minimum Data Setup Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		135 55 45	270 110 90	ns ns ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 50 40	200 100 80	ns ns ns
f_{CL}	Maximum Clock Frequency (Toggle Mode)	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	2.5 6.2 7.6	5 12.5 15.5		MHz MHz MHz
t_{rCL} or t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	15 10 5			μs μs μs
t_W	Minimum Clock Pulse Width ($t_{WH} = t_{WL}$)	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		100 40 32	200 80 65	ns ns ns
t_{WH}	Minimum Set and Reset Pulse Width	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		80 30 25	160 60 50	ns ns ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Per Flip-Flop (Note 4)		35		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

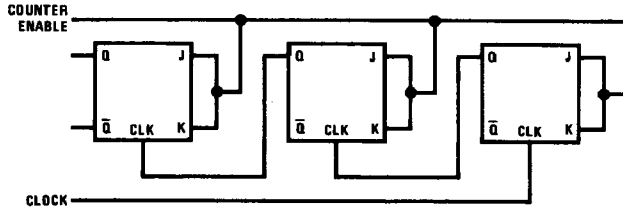
Note 2: $V_{SS} = 0\text{V}$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

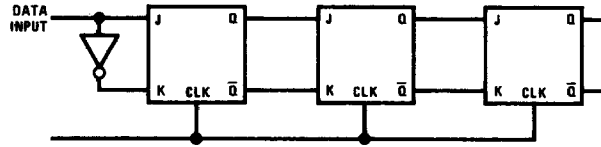
Typical Applications

Ripple Binary Counters



TL/F/5958-3

Shift Registers



TL/F/5958-4

Truth Table

${}^{*}t_{n-1}$ Inputs						${}^{*}t_n$ Outputs	
CL Δ	J	K	S	R	Q	Q	\bar{Q}
↗	1	X	0	0	0	1	0
↘	X	0	0	0	1	1	0
↗	0	X	0	0	0	0	1
↘	X	1	0	0	1	0	1
↗	X	X	0	0	X	(No Change)	
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

Where: 1 = High Level
 0 = Low Level
 Δ = Level Change
 X = Don't Care
 ${}^{*}t_{n-1}$ refers to the time interval prior to the positive clock pulse transition
 ${}^{*}t_n$ refers to the time intervals after the positive clock pulse transition