

**SN54ABT16648, SN74ABT16648**  
**16-BIT TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

SEPTEMBER 1992 - REVISED OCTOBER 1992

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-IIIB™ BICMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (-32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )**
- **Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings**

#### description

The 'ABT16648 is a 16-bit bus transceiver that consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16648.

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus will receive data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16648 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16648 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16648 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

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PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

**SN54ABT16648 . . . WD PACKAGE**  
**SN74ABT16648 . . . DL PACKAGE**  
**(TOP VIEW)**

1DIR	1	56	1 $\overline{OE}$
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
$V_{CC}$	7	50	$V_{CC}$
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
$V_{CC}$	22	35	$V_{CC}$
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2DIR	28	29	2 $\overline{OE}$



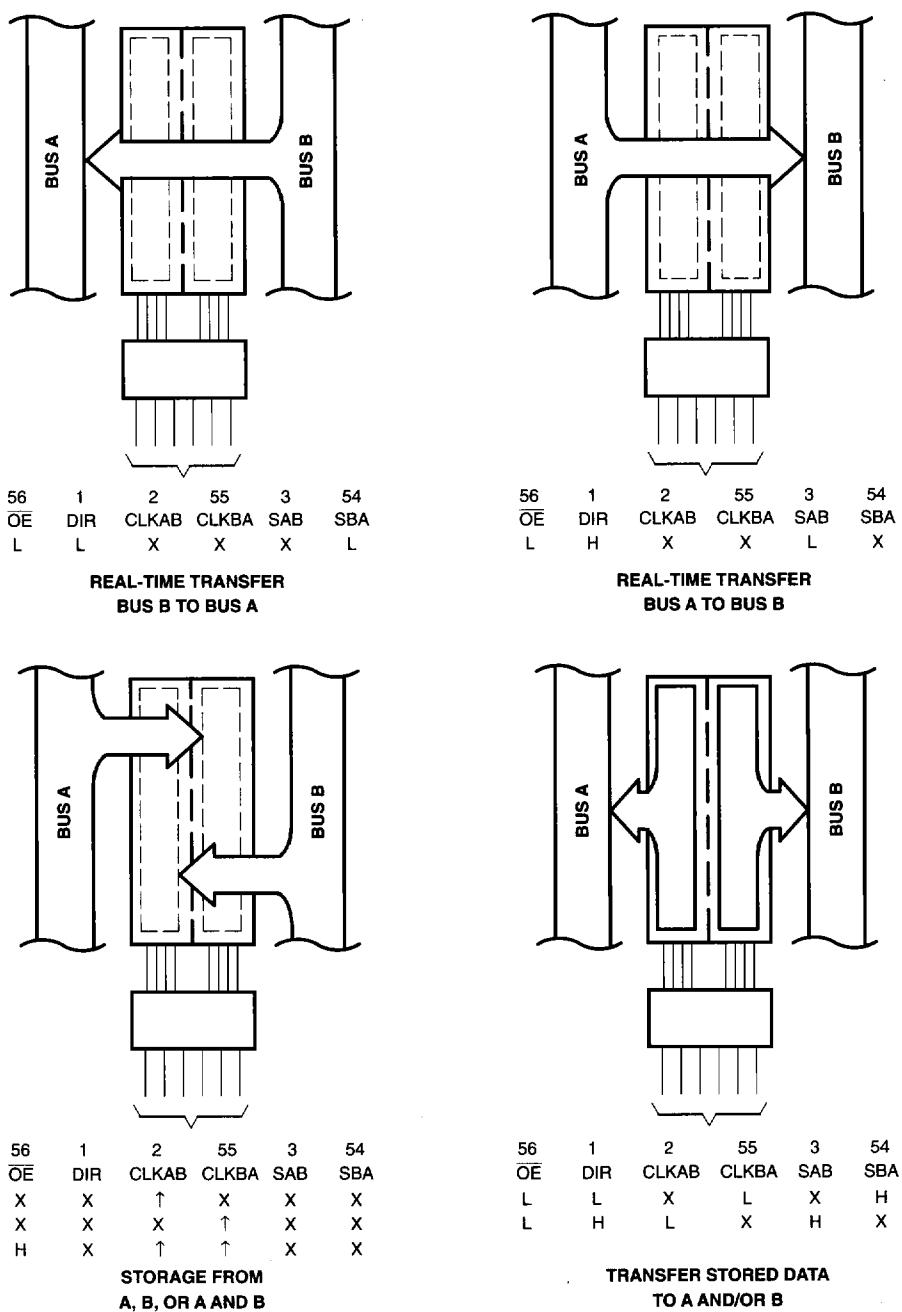
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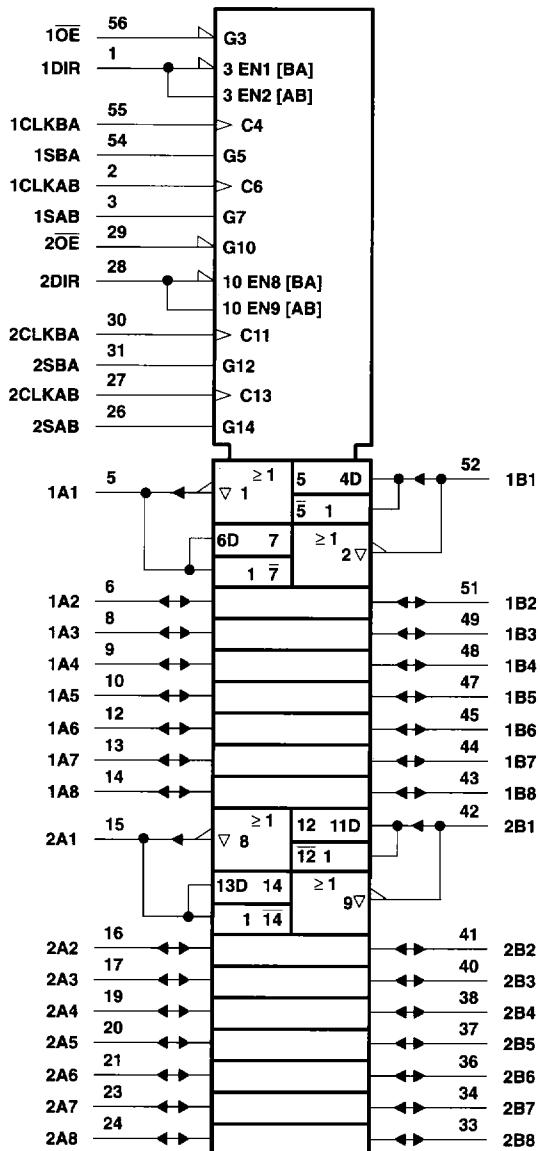


**Figure 1. Bus-Management Functions**



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logic symbol†

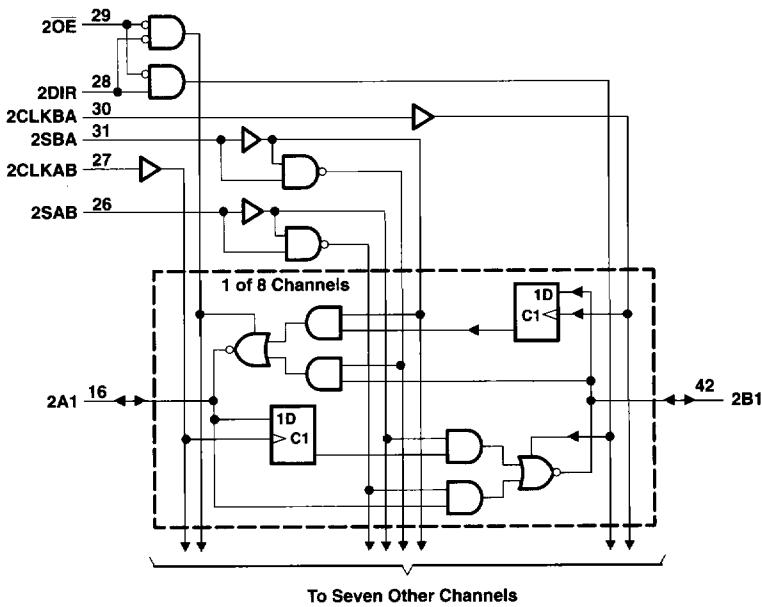
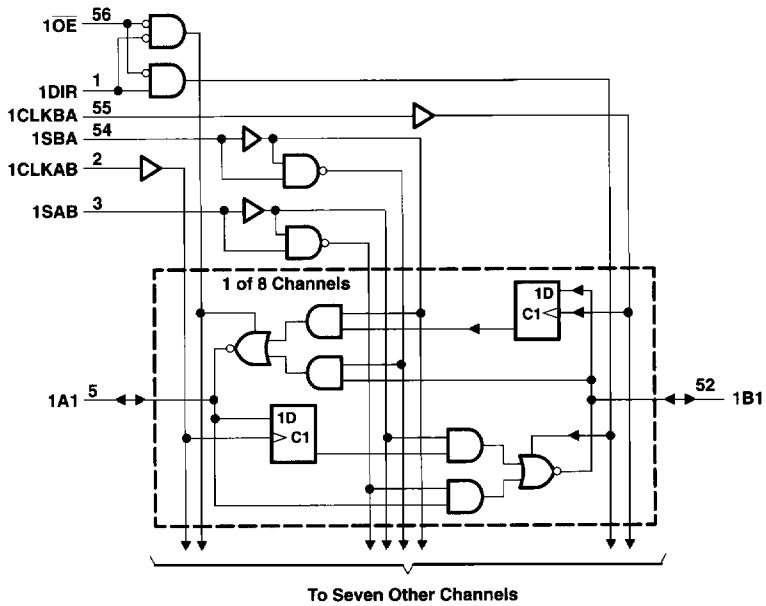


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**logic diagram (positive logic)**



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**FUNCTION TABLE**  
 (each 8-bit section)

OE	DIR	INPUTS			DATA I/O		OPERATION OR FUNCTION	
		CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, V <sub>CC</sub> .....	-0.5 V to 7 V
Input voltage range, V <sub>I</sub> (except I/O ports) (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V <sub>O</sub> .....	-0.5 V to 5.5 V
Current into any output in the low state, I <sub>O</sub> : SN54ABT16648 .....	96 mA
	SN74ABT16648 .....
Input clamp current, I <sub> K</sub> (V <sub>I</sub> < 0) .....	-18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0) .....	-50 mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) .....	1 W
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**recommended operating conditions (see Note 2)**

		SN54ABT16648		SN74ABT16648		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24		-32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TA = 25°C		SN54ABT16648		SN74ABT16648		UNIT
		MIN	TYPE†	MAX	MIN	MAX	MIN	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5		2.5	V
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3		3	
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA	2			2			
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -32 mA	2‡					2	
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA			0.55	0.55			V
	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 64 mA			0.55‡			0.55	
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND	Control inputs		±1	±1	±1		µA
		A or B ports		±100	±100	±100		
I <sub>OZH</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50	50	50		µA
I <sub>OZL</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-50	-50	-50		µA
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100			±100	µA
I <sub>CEx</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high		50	50	50		µA
I <sub>O¶</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50 -100 -180			-50 -180		-50 -180	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	A or B ports	Outputs high	2	2	2		mA
			Outputs low	72	72	30		
			Outputs disabled	2	2	2		
ΔI <sub>CC</sub> #	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Data inputs	Outputs enabled	1	1.5	1		mA
			Outputs disabled	0.05	0.05	0.05		
		Control inputs		1.5	1.5	1.5		
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V	Control inputs						pF
C <sub>io</sub>	V <sub>O</sub> = 2.5 V or 0.5 V	A or B ports						pF

† All typical values are at V<sub>CC</sub> = 5 V.

‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

§ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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