mosaic
semiconductor, inc.

128K x 32 SRAM MODULE

PUMA 68S4000-020/025/35/45

Issue 4.2 : August 1997

Description

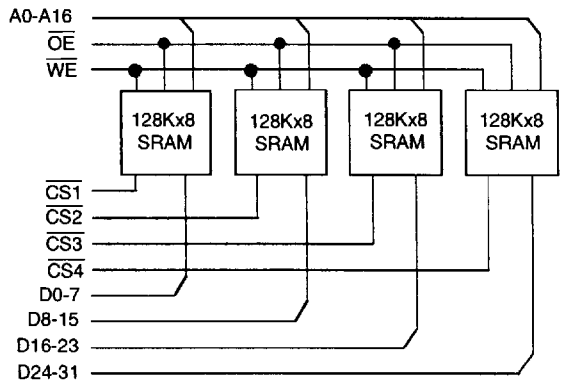
The PUMA68S4000 is a 4Mbit CMOS High Speed Static RAM organised as 128K x 32 in a JEDEC 68 pin surface mount PLCC, available with access times of 20, 25, 35, and 45ns. The output width is user configerable as 8 , 16 or 32 bits using four Chip Selects ($\overline{CS1-4}$). The plastic device is screened to ensure high reliability.

The device features low power standby, multiple ground pins for maximum noise immunity and TTL compatible inputs and outputs. The PUMA 68S4000 offers a dramatic space saving advantage over four standard 128Kx8 devices. A low power standby option with 2V data retention mode is available.

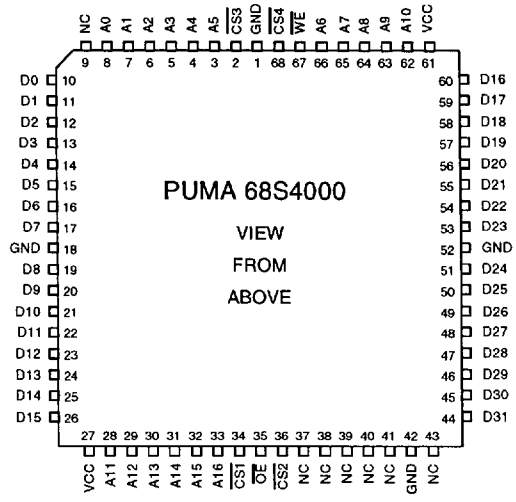
Features

- Very Fast Access Times of 020,025,35,45 ns.
- JEDEC 68 'J' leaded plastic Surface Mount Substrate.
- Industrial, Military or Military(High Rel) Grade.
- User Configurable as 8 / 16 / 32 bit wide output.
- Operating Power : 2.86 W (max)
- Standby Power : -L Part 44 mW (max)
- TTL Compatible Inputs and Outputs.
- Fully Static operation.
- Multiple ground pins for maximum noise immunity.
- Single 5V±10% Power supply.

Block Diagram



Pin Definition



Pin Functions

Address Inputs	**A0 - A16**
Data Input/Output	**D0 - D31**
Chip Select	**$\overline{CS1-4}$**
Write Enable	**$\overline{WE}$**
Output Enable	**$\overline{OE}$**
No Connect	**NC**
Power (+5V)	**V_{CC}**
Ground	**GND**

Package Details

Plastic 68 J-Leaded JEDEC PLCC

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Parameter	Symbol	Min	Typ	Max	Unit
Voltage on any pin relative to V_{SS}	V_T (2)	-0.5	-	7.0	V
Power Dissipation	P_T	-	-	5.0	W
Storage Temperature	T_{STG}	-65	-	150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.0V pulse of less than 10ns.

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
Input High Voltage		V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage		V_{IL}	-0.3	-	0.8	V
Operating Temperature	(Commercial)	T_A	0	-	70	°C
	(Industrial)	T_{AI}	-40	-	85	°C (Suffix I)
	(Military)	T_{AM}	-55	-	125	°C (Suffix M,MB)

DC Electrical Characteristics (V_{CC}=5V±10%, TA = -55°C to +125°C)

Parameter		Symbol	Test Condition	Min	Typ	max	Unit
I/P Leakage Current	Address,$\overline{OE}$,$\overline{WE}$	I_{LI}	$0V \le V_{IN} \le V_{CC}$	-20	-	20	µA
Output Leakage Current		I_{LO}	$\overline{CS} = V_{IH}$, $V_{I/O}$ = GND to V_{CC}	-20	-	20	µA
Operating Supply Current	32-bit mode	I_{CC32}	Min. Cycle, $\overline{CS} = V_{IL}$, f=f_{MAX}, I_{OUT} = 0mA	-	-	520	mA
(015 ns)	32-bit mode	I_{CC32}	Min. Cycle, $\overline{CS} = V_{IL}$, f=f_{MAX}, I_{OUT} = 0mA	-	-	600	mA
	16-bit mode	I_{CC16}	As Above.	-	-	320	mA
	8-bit mode	I_{CC8}	As Above.	-	-	250	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS} = V_{IH}$, f=f_{MAX}	-	-	160	mA
	CMOS levels	I_{SB2}	$\overline{CS} \ge V_{CC}$-0.2V, $0.2 \le V_{IN} \le V_{CC}$-0.2V, f=0	-	-	40	mA
	-L Version (CMOS)	I_{SB3}	$\overline{CS} \ge V_{CC}$-0.2V, $0.2 \le V_{IN} \le V_{CC}$-0.2V, f=0	-	-	8	mA
Output Voltage		V_{OL}	I_{OL} = 8.0mA	-	-	0.4	V
		V_{OH}	I_{OH} = -4.0mA	2.4	-	-	V

Notes :

1/ Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

2/ $\overline{CS}$ above refers to $\overline{CS1}$~$\overline{4}$.

3/ At f=f_{MAX} address and data inputs are cycling at maximum frequency.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

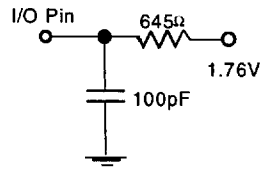
Note: Capacitance calculated, not measured.

Parameter	*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance (Address,$\overline{OE}$,$\overline{WE}$)	C_{IN1}	V_{IN} = 0V	30	pF
I/P Capacitance (other)	C_{IN2}	V_{IN} = 0V	7	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	38	pF

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%

Output Load



Operation Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*DATA PINS*	*SUPPLY CURRENT*	*MODE*
H	X	X	High Impedance	I_{SB1}, I_{SB2}, I_{SB3}	Standby
L	L	H	Data Out	I_{CC32}, I_{CC16}, I_{CC8}	Read
L	H	L	Data In	I_{CC32}, I_{CC16}, I_{CC8}	Write
L	L	L	Data In	I_{CC32}, I_{CC16}, I_{CC8}	Write
L	H	H	High-Impedance	I_{SB1}, I_{SB2}, I_{SB3}	High-Z

Notes : H = V_{IH} : L = V_{IL} : X = V_{IH} or V_{IL}

$\overline{CS}$ above refers to $\overline{CS1}$~4.

Low V_{cc} Data Retention Characteristics - L Version Only

Parameter	*Symbol*	*Test Condition*	*min*	*typ(1)*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR1} (1,2)	V_{CC}=3.0V, $\overline{CS} \geq V_{CC}$-0.2	-		4	mA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}	-	-	ms

Notes (1) Typical figures are measured at 25°C.
(2) This parameter is guaranteed not tested.

AC OPERATING CONDITIONS

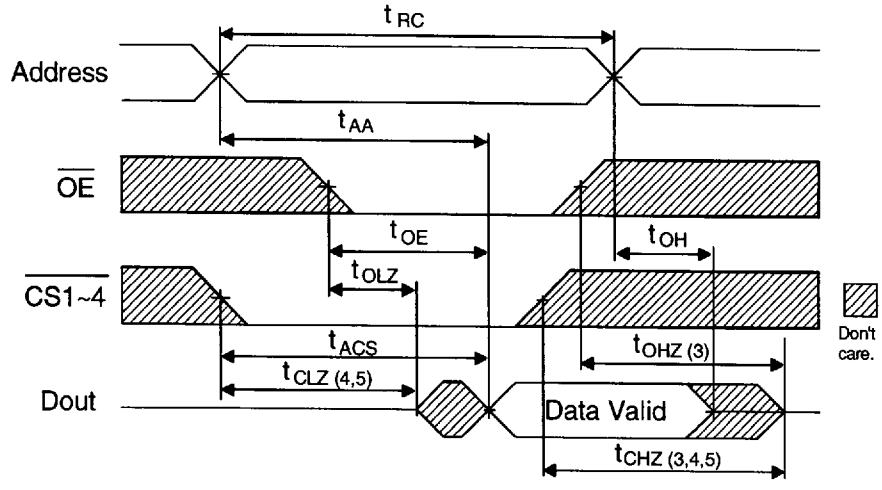
Read Cycle

		-020		-025		-35		-45		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	20	-	25	-	35	-	45	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	-	45	ns
Chip Select Access Time	t_{ACS}	-	20	-	25	-	35	-	45	ns
Output Enable to Output Valid	t_{OE}	-	9	-	9	-	12	-	15	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Deselection to O/P in High Z	t_{CHZ}	0	9	0	10	0	12	0	15	ns
Output Disable to Output in High Z	t_{OHZ}	0	7	0	10	0	12	0	15	ns

Write Cycle

		-020		-025		-35		-45		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Write Cycle Time	t_{WC}	20	-	25	-	35	-	45	-	ns
Chip Selection to End of Write	t_{CW}	15	-	20	-	25	-	35	-	ns
Address Valid to End of Write	t_{AW}	15	-	20	-	25	-	35	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	12	-	15	-	17	-	20	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	10	0	12	0	15	0	15	ns
Data to Write Time Overlap	t_{DW}	10	-	12	-	15	-	15	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output active from end of write	t_{OW}	2	-	2	-	2	-	2	-	ns

Read Cycle Timing Waveform (1,2)



AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

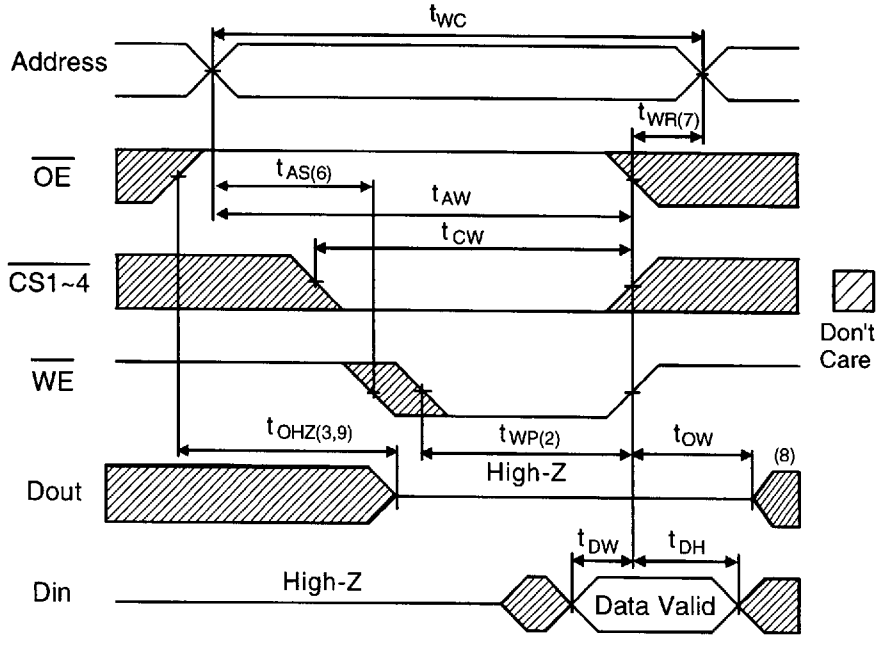
(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

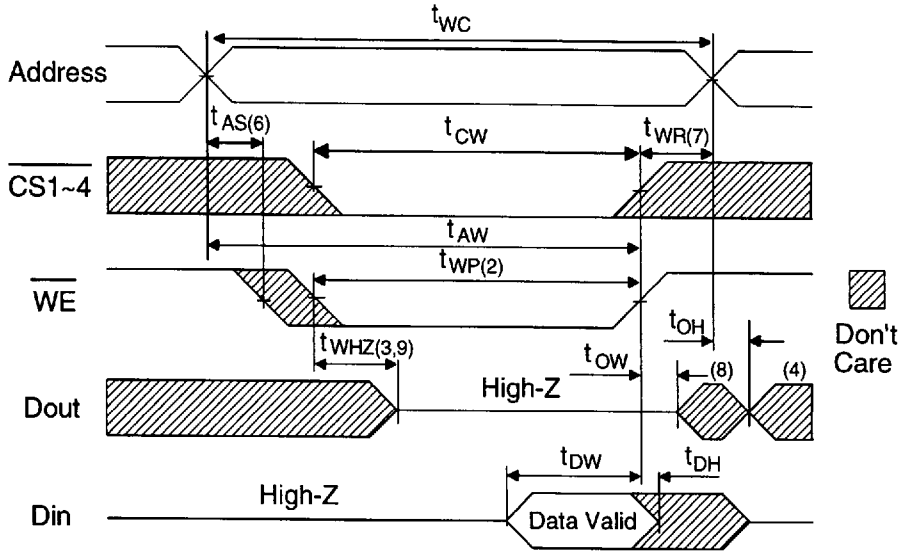
(4) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform (1,4)



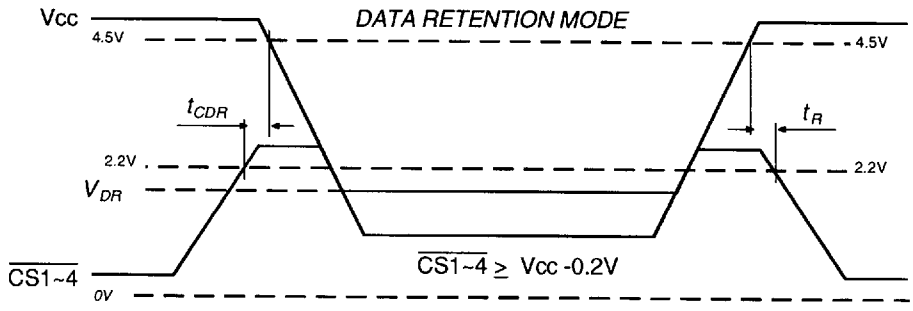
Write Cycle No.2 Timing Waveform (1,5)



AC Write Characteristics Notes

(1) All write cycle timing is referenced from the last valid address to the first transition address.
(2) All writes occur during the overlap of $\overline{CS1\sim4}$ and $\overline{WE}$ low.
(3) If $\overline{OE}$, $\overline{CS1\sim4}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.
(4) Dout is the Read data of the new address.
(5) $\overline{OE}$ is continuously low.
(6) Address is valid prior to or coincident with $\overline{CS1\sim4}$ and $\overline{WE}$ low, too avoid inadvertant writes.
(7) $\overline{CS1\sim4}$ or $\overline{WE}$ must be high during address transitions.
(8) When $\overline{CS1\sim4}$ are low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.
(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Data Retention Waveform



SCREENING

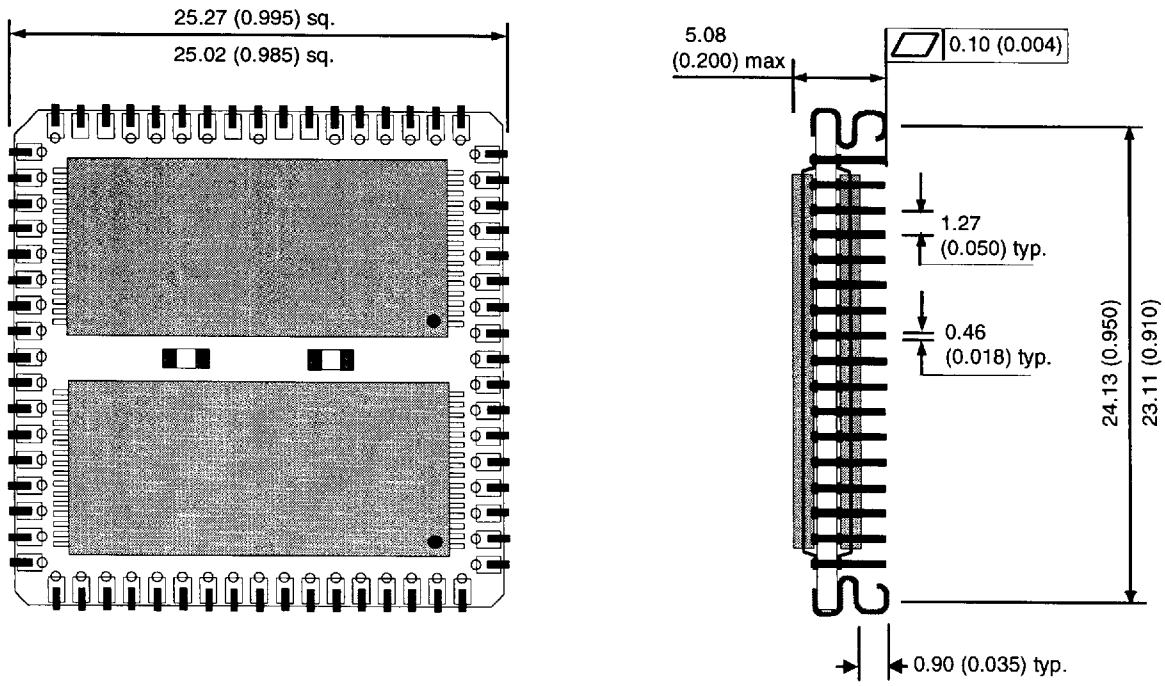
Military Screening Procedure

Screening Flow for high reliability product is in accordance with Mil-883 method 5004 .

MB MODULE SCREENING FLOW		
SCREEN	**TEST METHOD**	**LEVEL**
Visual and Mechanical		
Temperature cycle	1010 Condition B (10 Cycles,-55°C to +125°C)	100%
Burn-In		
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	T_A=+125°C,160hrs minimum.	100%
Final Electrical Tests	Per applicable Device Specification	
Static (DC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (AC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
External Visual	2009 Per vendor or customer specification	100%

Package Information Dimensions in mm(inches)

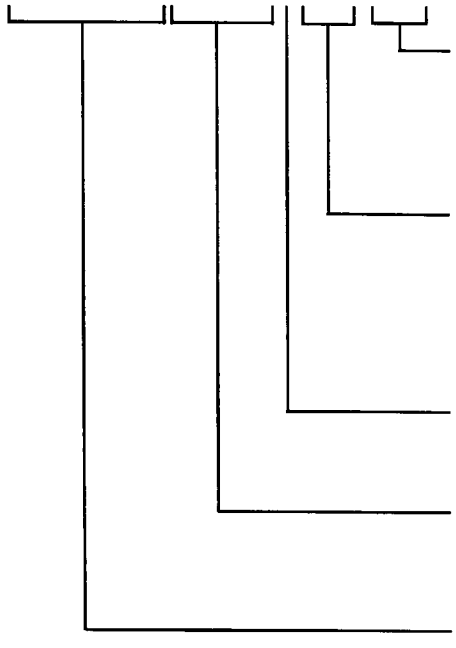
Plastic 68 Pin JEDEC Surface mount PLCC



Mosaic Semiconductor, Inc., 7420 Carroll Rd. Suite 300, San Diego, CA 92121
Tel: 619.271.4565 Fax: 619.271.6058

Ordering Information

PUMA 68S4000LMB-020



Speed	020	=	20 ns
	025	=	25 ns
	35	=	35 ns
	45	=	45 ns
Temp. range/screening	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
	M	=	Military Temperature
	MB	=	Screened in accordance with MIL STD-883
Power Consumption	Blank	=	Standard
	L	=	Low Power
Memory Organisation	S4000	=	128K x 32 SRAM configurable as 256K x 16 and 512K x 8
Package	PUMA 68	=	68 pin "J" Leaded PLCC