MOTOROLA

Military 54F373

Octal Transparent Latch With Active Low Enable 3-State Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/34601

The 54F373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

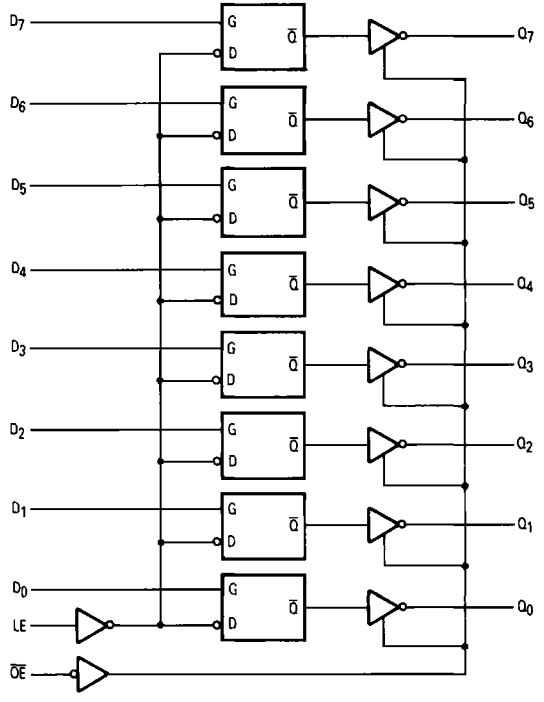
- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing

AVAILABLE AS:

1) JAN: JM38510/34601BXA
2) SMD: *
3) 883C: 54F373/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2
***Call Factory for latest update**

LOGIC DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{OE}$	1	1	1	V_{CC}
Q_0	2	2	2	OPEN
D_0	3	3	3	V_{CC}
D_1	4	4	4	V_{CC}
Q_1	5	5	5	OPEN
Q_2	6	6	6	OPEN
D_2	7	7	7	V_{CC}
D_3	8	8	8	V_{CC}
Q_3	9	9	9	OPEN
GND	10	10	10	GND
LE	11	11	11	V_{CC}
Q_4	12	12	12	OPEN
D_4	13	13	13	V_{CC}
D_5	14	14	14	V_{CC}
Q_5	15	15	15	OPEN
Q_6	16	16	16	OPEN
D_6	17	17	17	V_{CC}
D_7	18	18	18	V_{CC}
Q_7	19	19	19	OPEN
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

5

FUNCTIONAL DESCRIPTION

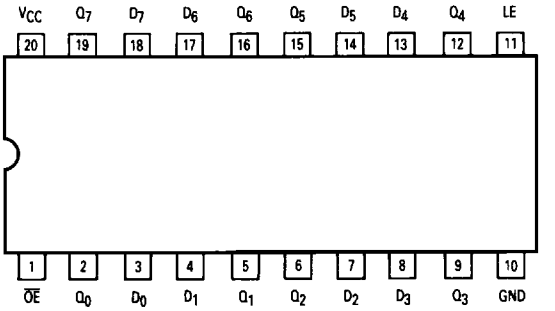
The 'F373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs at setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

TRUTH TABLE

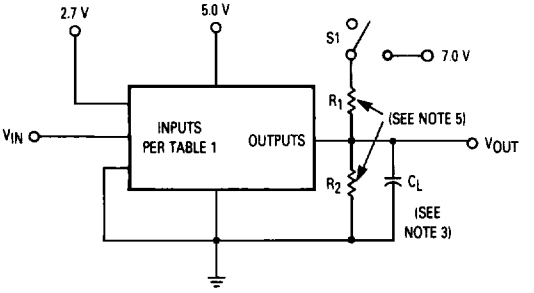
Inputs			Output
D_n	LE	OE	Q_n
H	H	L	H
L	H	L	L
X	H	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

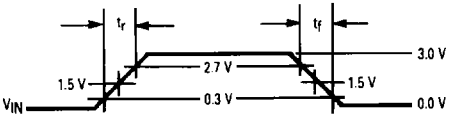
CONNECTION DIAGRAM



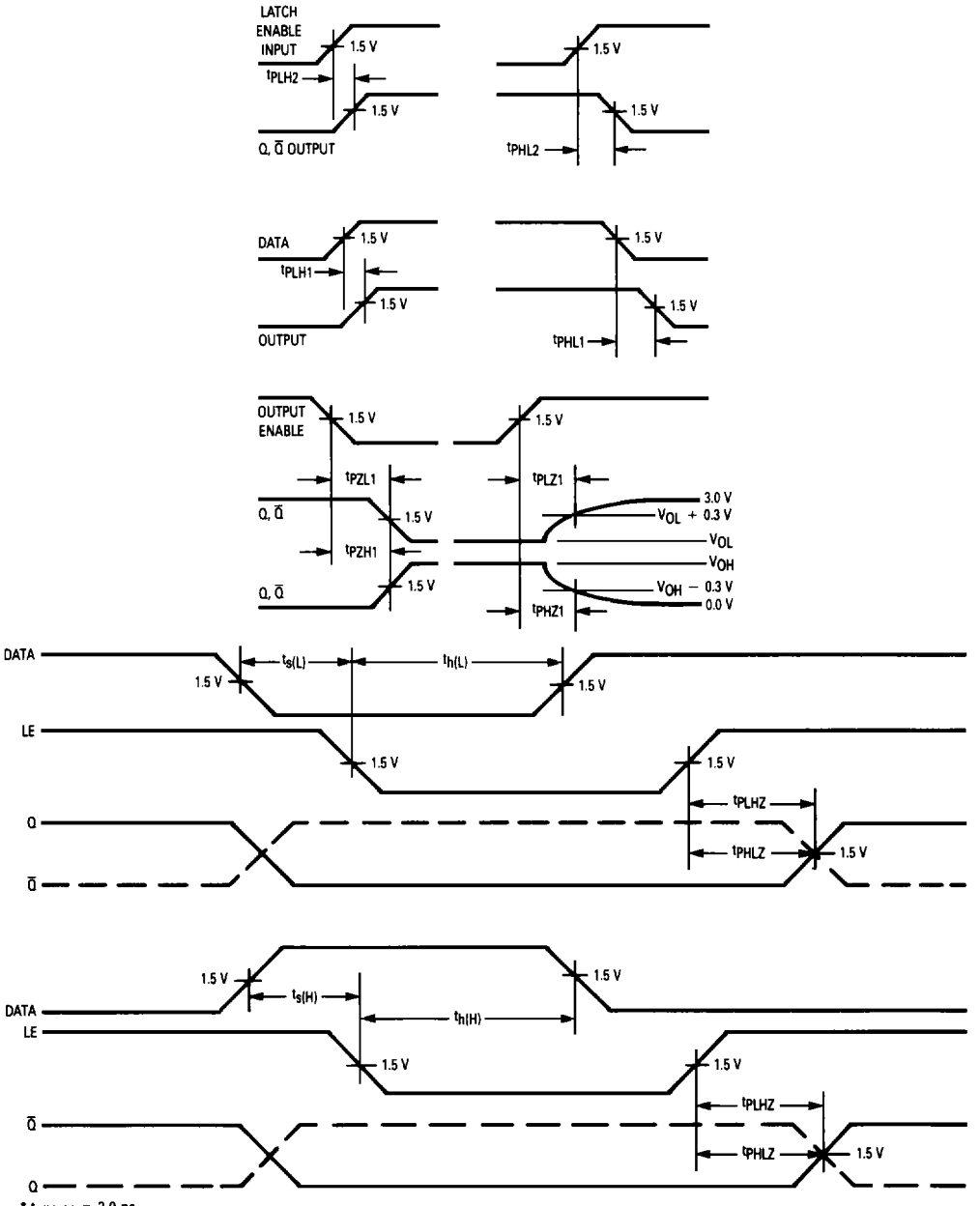
AC TEST CIRCUIT



Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed



WAVEFORMS



* $t_{s(H, L)}$ = 2.0 ns.
* $t_{h(H, L)}$ = 3.0 ns.
* Setup and Hold times are for information only. No testing required.

5

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IH} = 2.0 V, other inputs are open, $\overline{OE}$ = 0.8 V, LE = 2.0 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V, other inputs are open, LE = 2.0 V, $\overline{OE}$ = 0.8 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 4.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open.
I_{OD}	Diode Current	35		35		35		mA	V_{CC} = 4.5 V, V_{IN} = 0 V, other inputs are open, LE = 5.5 V, $\overline{OE}$ = 0 V, V_{OUT} = 2.5 V.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other inputs are open, V_{OUT} = 0 V, LE = 5.5 V, $\overline{OE}$ = 0 V.
I_{IOZH}	Output Off Current High		50		50		50	μA	V_{CC} = 5.5 V, V_{IN} = 0 V, other inputs are open, V_{OUT} = 2.4 V, $\overline{OE}$ = 2.0 V, LE = 5.5 V.
I_{IOZL}	Output Off Current Low		−50		−50		−50	μA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are open, V_{OUT} = 0.5 V, $\overline{OE}$ = 2.0 V, LE = 5.5 V.
I_{CCH}	Power Supply Current Off		55		55		55	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), LE = 5.5 V, $\overline{OE}$ = 0 V.
I_{CCL}	Power Supply Current Off		60		60		60	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), LE = 5.5 V, $\overline{OE}$ = 0 V.
I_{CCZ}	Power Supply Current Off		60		60		60	mA	V_{CC} = 5.5 V, all inputs are open, LE & $\overline{OE}$ = 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			
									per Truth Table with V_{CC} = 4.5 V, **(Repeat at)** V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

5

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output D_n to Q_n	2.0	5.0	2.0	7.0	2.0	7.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output D_n to Q_n	3.0	7.0	3.0	8.5	3.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL2}	Propagation Delay /Data-Output LE to Q_n	3.0	7.0	3.0	8.5	3.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output LE to Q_n	5.0	11.5	5.0	15	5.0	15	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLZ1}	Output Disable Time, $\overline{OE}$ to Q_n	1.5	6.5	1.5	7.0	1.5	7.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHZ1}	Output Disable Time, $\overline{OE}$ to Q_n	1.5	6.5	1.5	10	1.5	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PZL1}	Output Enable Time, $\overline{OE}$ to Q_n	2.0	7.5	2.0	10	2.0	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PZH1}	Output Enable Time, $\overline{OE}$ to Q_n	2.0	11	2.0	15	2.0	15	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.

NOTES:
1. Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz, $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_1 = R_2$ = 499 Ω ± 5.0%.

5