Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

CMOS Logic ICs - CD4000B Series

Features

The Harris High-Reliability CD4000B Series of high-voltage CMOS integrated circuits consists of a broad range of SSI, MSI-1, and MSI-2 (LSI) functions from simple gates to complex counters, registers, and arithmetic circuits. Specific design features for CMOS devices and the performance advantages of CMOS technology - low power consumption, high noise immunity, high speed, high fanout TTL and DTL logic compatibility, excellent temperature stability, and fully protected inputs and outputs - provide the logic system designer with a capability to achieve outstanding performance, high reliability and simplified circuitry in a wide variety of equipment designs.

- 100% Tested for Quiescent Current at 20V
- Maximum Input Current (Leakage of 1µA at 18V Over Full Package-Temperature Range; 100nA at 18V at +25°C
- Standardized Symmetrical Output Characteristics
- 5V, 10V, and 15V Parametric Ratings
- Noise Margin (Over Full Package-Temperature Range)
  - 1V at V_{DD} = 5V
  - 2V at V_{DD} = 10V
  - 2.5V at V_{DD} = 15V
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Buffered vs Unbuffered Gates

The new industry standard establishes a suffix "UB" for CMOS products that meet all B-Series specifications except that the logical outputs of the devices are not buffered and the V_{IL} and V_{IH} specifications are 20% and 80% of V_{DD}, respectively. See Application Note AN6558, "Understanding Buffered and Unbuffered CMOS Characteristics". See Section 8, "How to Use AnswerFAX", in this selection guide. The suffix "B" defines high voltage buffered output devices in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

Both buffered "B" and unbuffered "UB" versions of the popular NOR and NAND gates are supplied to make available to designers the advantages of both. The following table briefly compares the features of the two versions.

CHARACTERISTIC	BUFFERED VERSION "B"	UNBUFFERED VERSION "UB"
Propagation Delay (Speed)	Moderate	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Low
Output Oscillation for Slow Inputs	Yes	No
Input Capacitance	Low	High

Compliance to MIL-STD-883

Harris CD4000 Series parts are in full compliance with Paragraph 1.2.1 of MIL-STD-883. Product is provided to meet the requirements of Class B.

SMD or DESC drawing parts are in full compliance with Paragraph 1.2.1 of MIL-STD-883 and meet the SMD or DESC drawings.

Suffix 3A meets Class B requirements. Electrical tests are performed to parameters described in the Electrical Specifications.

Harris also provides CD4000 Series parts that meet the requirements of MIL-STD-883, Paragraph 1.2.2. This family of parts has the following designation.

Suffix 3 meets most of the requirements of a Class B part as described in details presented in the Lot Screening and Product Flow tables.

JAN M38535 CMOS ICs

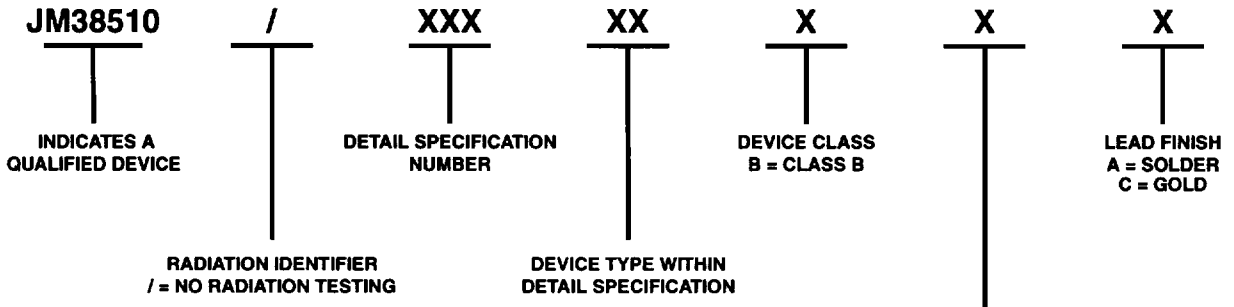
The Harris High-Reliability product line also provides devices that are manufactured and tested in accordance with the MIL-I-38535 (detailed and general) specification, which includes methods and procedures of the Military Standard MIL-STD-883.

SCREENING LEVELS FOR STANDARD HARRIS HIGH-RELIABILITY CD4000B-SERIES INTEGRATED CIRCUITS

SCREENING LEVELS		APPLICATION	DESCRIPTION	PACKAGE OPTIONS
3A	Class B (Full Compliance)	Mil. and Ind. For example, in Airborne Electronics	For devices intended for use where maintenance and replacement can be performed but are difficult and expensive.	F
3	Class B, Modified			D, K

Product Ordering Information

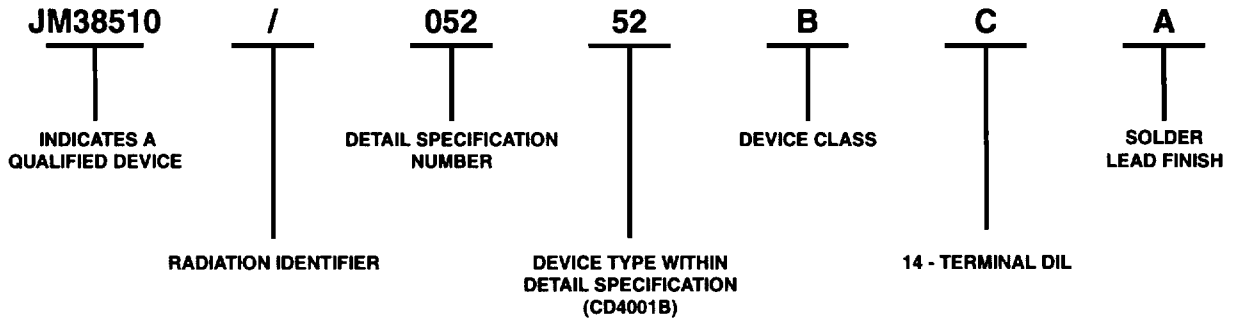
HOW TO ORDER HARRIS CD4000B SERIES MIL-I-38510 JAN-QUALIFIED PRODUCT



PACKAGE OUTLINE

LETTER = TERMINALS	PACKAGE	CASE OUTLINE	CONFIGURATION
C = 14	DIL	D-1	1
E = 16	DIL	D-2	1

EXAMPLE



Branding: JAN products are single branded with the MIL-I-38510 nomenclature.

Product Ordering Information (Continued)

HOW TO ORDER SMD AND DESC DRAWING PRODUCT

5962	XXXXX	XX	X	X
SMD ID NUMBER (DOES NOT CHANGE)	DESC AND SMD DRAWING NUMBER	DEVICE TYPE (PARAGRAPH 1.2.1 OF SMD/DESC DRAWING)		LEAD FINISH A = SOLDER

PACKAGE OUTLINE

LETTER = TERMINALS	CASE OUTLINE	CONFIGURATION
C = 14	D-1	1
E = 16	D-2	1
J = 24	D-3	1

SMD EXAMPLE

5962	90640	01	C	A
SMD ID NUMBER	SMD DRAWING NUMBER	DEVICE TYPE 01 = 4016B FROM DRAWING	14 - TERMINAL DIL	SOLDER LEAD FINISH

DESC EXAMPLE

77023	01	E	A
DESC DRAWING NUMBER	DEVICE TYPE 01 = 4520B FROM DRAWING	16 - TERMINAL DIL	SOLDER LEAD FINISH

Branding: SMD/DESC products are double branded with both the Harris nomenclature and SMD/DESC nomenclature.

HOW TO ORDER HARRIS STANDARD CD4000 SERIES /883 SCREENED PRODUCT

CD4000B	D	3
PART NUMBER CD4000B	PACKAGE DESIGNATOR D = DUAL-IN-LINE METAL SEAL CERAMIC K = FLAT PACK F = DUAL-IN-LINE FRIT SEAL CERAMIC	RELIABILITY SCREENING LEVEL 3A = CLASS B, MIL-STD-883 3 = CLASS B, MODIFIED

Description of Data Supplied

JAN or Class B Product

- Processing and Screening Compliance C of C
- Group A Attribute Summary
- Group B Attribute Summary
- Groups C and D Attribute Summary when tests are performed on product being supplied; or Date of Performance when tests are covered by another type from the same microcircuit group.

Suffix 3A Harris /883 Full Compliant

- Processing and Screening Compliance C of C
- Group A Attribute Summary
- Group B Attribute Summary
- Group C and D Attribute Summary Available Per Request at Added Cost

Suffix 3 Harris /883 Non Compliant

- Processing and Screening Compliance C of C
- Group A Attribute Summary

Product Number Selection Guide

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4000A	CD4000A	Dual 3-Input NOR Gate Plus Inverter	F	B	14
4000B	CD4000B	Dual 3-Input NOR Gate Plus Inverter	D	3	14
4000UB	CD4000UB	Dual 3-Input NOR Gate Plus Inverter	D	3	14
4001A	CD4001A	Quad 2-Input NOR Gate	F	B	14
			D, K	3	
4001B	CD4001B	Quad 2-Input NOR Gate	F	B	14
			F	3A	
			D, K	3	
4001UB	CD4001UB	Quad 2-Input NOR Gate	F	B	14
			D	3	
4002A	CD4002A	Dual 4-Input NOR Gate	D	3	14
4002B	CD4002B	Dual 4-Input NOR Gate	F	B	14
			F	3A	
			D, K	3	
4002UB	CD4002UB	Dual 4-Input NOR Gate	F	3A	14
			D, K	3	
4006A	CD4006A	18-Stage Static Shift Register	D	3	14
4006B	CD4006B	18-Stage Static Shift Register	F	3A	14
			D	3	
4007A	CD4007A	Dual Complementary Pair Plus Inverter	F	B	14
			D	3	
4007UB	CO4007UB	Dual Complementary Pair Plus Inverter	F	3A	14
			D	3	
4008B	CD4008B	4-Bit Full Adder with Parallel Carry-Out	F	3A	16
			D	3	
4009UB	CD4009UB	Hex Buffer/Converter (Inverting)	F	3A	16
			D, K	3	
4010B	CD4010B	Hex Buffer/Converter (Non-Inverting)	F	3A	16
			D, K	3	
4011A	CD4011A	Quad 2-Input NAND Gate	F	B	14
			D, K	3	
4011B	CD4011B	Quad 2-Input NAND Gate	F	B	14
			F	3A	
			D, K	3	
4011UB	CD4011UB	Quad 2-Input NAND Gate	F	3A	14
			D	3	
4012A	CD4012A	Dual 4-Input NAND Gate	D	3	14

Product Number Selection Guide (Continued)

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4012B	CD4012B	Dual 4-Input NAND Gate	F	B	14
			F	3A	
			D	3	
4013A	CD4013A	Dual "D" Flip-Flop with Set/Reset Capability	F	B	14
4013B	CD4013B	Dual "D" Flip-Flop with Set/Reset Capability	F	B	14
			F	3A	
			D, K	3	
4014A	CD4014A	8-Stage Static Shift Register	D	3	16
4014B	CD4014B	8-Stage Static Shift Register	F	3A	16
			D	3	
4015A	CD4015A	Dual 4-Stage Static Shift Register	D	3	16
4015B	CD4015B	Dual 4-Stage Static Shift Register	F	3A	16
			D, K	3	
4016A	CD4016A	Quad Bilateral Switch	D	3	14
4016B	CD4016B	Quad Bilateral Switch	F	3A	14
			D, K	3	
4017A	CD4017A	Decade Counter/Divider	F	B	16
			D	3	
4017B	CD4017B	Decade Counter/Divider	F	B	16
			F	3A	
			D	3	
4018A	CD4018A	Presettable Divide-By "N" Counter	D	3	16
4018B	CD4018B	Presettable Divide-By "N" Counter	F	B	16
			F	3A	
			D, K	3	
4019A	CD4019A	Quad AND/OR Select Gate	F	B	16
			D	3	
4019B	CD4019B	Quad AND/OR Select Gate	F	B	16
			F	3A	
			D, K	3	
4020A	CD4020A	14-Stage Binary Ripple Counter	F	B	16
			D, K	3	
4020B	CD4020B	14-Stage Binary Ripple Counter	F	B	16
			F	3A	
			D	3	
4021A	CD4021A	8-Stage Static Shift Register	D, K	3	16
4021B	CD4021B	8-Stage Static Shift Register	F	B	16
			F	3A	
			D, K	3	

Product Number Selection Guide (Continued)

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4022A	CD4022A	Divide-by-8 Counter/Divider	D	3	16
4022B	CD4022B	Divide-by-8 Counter/Divider	F	3A	16
			D	3	
4023A	CD4023A	Triple 3-Input NAND Gate	F	B	14
			D, K	3	
4023B	CD4023B	Triple 3-Input NAND Gate	F	B	14
			F	3A	
			D, K	3	
4023UB	CD4023UB	Triple 3-Input NAND Gate	D	3	14
4024A	CD4024A	7-Stage Binary Ripple Counter	F	B	14
			D, K	3	
4024B	CD4024B	7-Stage Binary Ripple Counter	F	B	14
			F	3A	
			D, K	3	
4025A	CD4025A	Triple 3-Input NOR Gate	F	B	14
			D	3	
4025B	CD4025B	Triple 3-Input NOR Gate	F	B	14
			F	3A	
			D	3	
4025UB	CD4025UB	Triple 3-Input NOR Gate	D	3	14
4027A	CD4027A	Dual "J-K" Flip-Flop with Set/Reset Capability	F	B	16
			D, K	3	
4027B	CD4027B	Dual "J-K" Flip-Flop with Set/Reset Capability	F	B	16
			F	3A	
			D, K	3	
4028A	CD4028A	BCD-to-Decimal Decoder	D	3	16
4028B	CD4028B	BCD-to-Decimal Decoder	F	3A	16
			D, K	3	
4029A	CO4029A	Presettable Up/Down Counter	D	3	16
4029B	CD4029B	Presettable Up/Down Counter	F	3A	16
			D, K	3	
4030A	CD4030A	Quad Exclusive-OR Gate	D	3	14
4030B	CD4030B	Quad Exclusive-OR Gate	F	B	14
			F	3A	
			D, K	3	
4031A	CD4031A	64-Stage Static Shift Register	D	3	16
4031B	CD4031B	64-Stage Static Shift Register	F	3A	16
			D, K	3	

Product Number Selection Guide (Continued)

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4033B	CD4033B	Decade Counter/Divider	D	3	16
4034B	CD4034B	8-Stage Static Shift Register	F	3A	24
			D	3	
4035B	CD4035B	4-Stage Parallel-In/Parallel-Out Shift Register	F	3A	24
			D, K	3	
4040A	CD4040A	12-Stage Binary Ripple Counter	D, K	3	16
4040B	CD4040B	12-Stage Binary Ripple Counter	F	3A	16
			D	3	
4041A	CD4041A	Quad True/Complement Butter	D	3	14
4041UB	CD4041UB	Quad True/Complement Buffer	F	3A	14
			D, K	3	
4042A	CD4042A	Quad Clocked "D" Latch	D, K	3	16
4042B	CD4042B	Quad Clocked "D" Latch	F	3A	16
			D, K	3	
4043A	CD4043A	Quad NOR R/S Latch (Three-State Outputs)	D	3	16
4043B	CD4043B	Quad NOR R/S Latch (Three-State Outputs)	F	3A	16
			D	3	
4044A	CD4044A	Quad NAND R/S Latch (Three-State Outputs)	D	3	16
4044B	CO4044B	Quad NAND R/S Latch (Three-State Outputs)	F	3A	16
			D	3	
4046A	CD4046A	Micropower Phase-Locked Loop	D	3	16
4046B	CD4046B	Micropower Phase-Locked Loop	F	3A	16
			D, K	3	
4047B	CD4047B	Monostable/Astable Multivibrator	F	3A	14
			D	3	
4048A	CD4048A	Multifunctional Expandable 8-Input Gate (Three-State Output)	D	3	16
4048B	CD4048B	Multifunctional Expandable 8-Input Gate (Three-State Outputs)	F	3A	16
			D	3	
4049A	CD4049A	Hex Buffer/Converter (Inverting)	F	B	16
			D	3	
4049UB	CD4049UB	Hex Buffer/Converter (Inverting)	F	B	16
			F	3A	
			D, K	3	
4050A	CD4050A	Hex Buffer/Converter (Non-Inverting)	F	B	16
			D	3	
4050B	CD4050B	Hex Buffer/Converter (Non-Inverting)	F	B	16
			F	3A	
			D, K	3	

Product Number Selection Guide (Continued)

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4051B	CD4051B	8-Channel Analog Multiplexer/Demultiplexer	F	3A	16
			D, K	3	
4052B	CD4052B	4-Channel Analog Multiplexer/Demultiplexer	F	3A	16
			D, K	3	
4053B	CD4053B	Analog Multiplexers/Demultiplexers Triple 2-Channel	F	3A	16
			D	3	
4054B	CD4054B	4-Segment Display Driver	F	3A	16
4056B	CD4056B	BCD-to-7-Segment Decoder/Driver with Strobed-Latch Function	F	3A	16
4059A	CD4059A	Programmable Divide-by-"N" Counter	D	3	24
4060A	CD4060A	14-Stage Binary Ripple Counter/Divider and Oscillator	D	3	16
4060B	CD4060B	14-Stage Binary Ripple Counter/Divider and Oscillator	F	3A	16
			D	3	
4063B	CD4063B	4-Bit Magnitude Comparator	F	3A	16
			D, K	3	
4066B	CD4066B	Quad Bilateral Switch	F	B	14
			F	3A	
			D, K	3	
4067B	CD4067B	16-Channel Analog Multiplexers/Demultiplexers	F	3A	24
			D	3	
4068B	CD4068B	8-Input NAND/AND Gate	F	3A	14
			D	3	
4069UB	CD4069UB	Hex Inverter	F	B	14
			F	3A	
			D	3	
4070B	CD4070B	Quad Exclusive-OR Gate	F	B	14
			F	3A	
			D	3	
4071B	CD4071B	Quad 2-Input OR Gate	F	B	14
			F	3A	
			D, K	3	
4072B	CD4072B	Dual 4-Input OR Gate	F	3A	14
			D	3	
4073B	CD4073B	Triple 3-Input AND Gate	F	B	14
			F	3A	
			D	3	

Product Number Selection Guide (Continued)

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4075B	CD4075B	Triple 3-Input OR Gate	F	B	14
			F	3A	
			D, K	3	
4076B	CD4076B	4-Bit "D" Flip-Flop (Three-State Outputs)	F	3A	16
			D	3	
4077B	CD4077B	Quad Exclusive-NOR Gate	F	3A	14
			D	3	
4078B	CD4078B	8-Bit NOT/OR Gate	F	3A	14
			D	3	
4081B	CD4081B	Quad 2-Input AND Gate	F	B	14
			F	3A	
			D, K	3	
4082B	CD4082B	Dual 4-Input AND Gate	F	B	14
			F	3A	
			D	3	
4085B	CD4085B	Dual 2-Wide, 2-Input AND/OR/INVERT (AOI) Gate	F	3A	14
			D	3	
4086B	CD4086B	Expandable 4-Wide, 2-Input AND/OR/INVERT (AOI) Gate	F	3A	14
			D	3	
4089B	CD4089B	Binary Rate Multiplier	F	3A	16
			D	3	
4093B	CD4093B	Quad 2-Input NAND Schmitt Trigger	F	3A	14
			D	3	
4094B	CD4094B	8-Stage Shift-and-Store Bus Register	F	3A	16
			D	3	
4095B	CD4095B	Gated "J-K" Flip-Flop (Non-Inverting)	F	3A	14
			D	3	
4096B	CD4096B	Gated "J-K" Flip-Flop (Inverting and Non-Inverting)	D	3	14
4097B	CD4097B	8-Channel Analog Multiplexer/Demultiplexer	D	3	24
4098B	CD4098B	Dual Monostable Multivibrator	F	B	16
			F	3A	
			D, K	3	
4099B	CD4099B	8-Bit Addressable Latch	F	B	16
			F	3A	
			D, K	3	
4502B	CD4502B	Strobed Hex Inverter/Buffer	F	B	16
			F	3A	
			D, K	3	

Product Number Selection Guide (Continued)

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
4503B	CD4503B	Hex Buffer (Non-Inverting)	F	3A	16
			D	3	
4504B	CD4504B	Hex Voltage-Level Shifter for TTL-to-CMOS CMOS-to-CMOS Operation	F	3A	16
4508B	CD4508B	Dual 4-Bit Latch	F	3A	24
			D, K	3	
4510B	CD4510B	Presettable 4-Bit BCD Up/Down Counter	F	3A	16
			D	3	
4511B	CD4511B	BCD-to-7-Segment Latch Decoder/Driver	F	3A	16
			D, K	3	
4512B	CD4512B	8-Channel Data Selector (Three-State Output)	F	3A	16
			D	3	
4514B	CD4514B	4-Bit Latch/4-to-16 Line Decoder (Outputs Low)	F	3A	24
			D	3	
4515B	CD4515B	4-Bit Latch/4-to-16 Line Decoder (Outputs Low)	F	3A	24
			D	3	
4516B	CD4516B	Presettable 4-Bit Binary Up/Down Counter	F	3A	16
			D	3	
4517B	CD4517B	Dual 64-Bit Shift Register	F	3A	16
			D	3	
4518B	CD4518B	Dual BCD Up Counter	F	3A	16
			D	3	
4520B	CD4520B	Dual Binary Up Counter	F	3A	16
			D	3	
4527B	CD4527B	BCD Rate Multiplier	D	3	16
4532B	CD4532B	8-Input Priority Encoder	F	3A	16
			D	3	
4536B	CD4536B	Programmable Timer	F	3A	16
			D	3	
4541B	CD4541B	CMOS Programmable Timer	F	3A	14
4555B	CD4555B	Dual 1 of 4 Decoder/Demultiplexer (Outputs High)	F	3A	16
4556B	CD4556B	Dual Binary to 1 of 4 Decoder/Demultiplexers (Outputs Low)	F	3A	16
			D	3	
4585B	CD4585B	4-Bit Magnitude Comparator	F	3A	16
4724B	CD4724B	8-Bit Addressable Latch	F	3A	16
14538B	CD14538B	Dual Precision Monostable Multivibrator	F	3A	16
40100B	CD40100B	9-Bit Parity Generator/Checker	D	3	16

Product Number Selection Guide (Continued)

GENERIC PART NUMBER	TYPE NUMBER	CIRCUIT FUNCTION	PACKAGE DESIGNATOR	STANDARD SCREENING LEVELS	NUMBER OF PINS
40101B	CD40101B	9-Bit Parity Generator/Checker	F	3A	14
			D	3	
40102B	CD40102B	Presettable 2-Decade BCD Down Counter	D	3	16
40103B	CD40103B	Presettable 8-Bit Binary Down Counter	F	3A	16
			D	3	
40104B	CD40104B	4-Bit Bidirectional Universal Shift Register	D	3	16
40105B	CD40105B	4-Bit X 16 Word FiFo Buffer Register	F	3A	16
			D, K	3	
40106B	CD40106B	Hex Schmitt Trigger	F	3A	14
			D, K	3	
40107B	CD40107B	Dual 2-Input NAND Buffer/Driver	F	3A	14
			D	3	
40108B	CD40108B	4 X 4 Multiport Register	D	3	24
40109B	CD40109B	Quad Low-to-High Voltage Interface	F	3A	16
			D, K	3	
40116	CD40116	CMOS High Speed 8-Bit Directional CMOS/TTL Interface Level Converter (GP511 is Rad-Hard Version)	D	3	22
40160B	CD40160B	Synchronous Programmable 4-Bit Counter Decade with Asynchronous Clear	F	3A	16
40161B	CD40161B	Synchronous Programmable 4-Bit Counter Binary with Asynchronous Clear	F	3A	16
			D	3	
40163B	CD40163B	Synchronous Programmable 4-Bit Counter Binary with Synchronous Clear	F	3A	16
40174B	CD40174B	Hex "D" Type Flip-Flop	F	3A	16
			D	3	
40175B	CD40175B	Quad 'D' Type Flip-Flop	F	3A	16
40192B	CD40192B	CMOS Look-Ahead Carry Generator	F	3A	16
			D	3	
40193B	CD40193B	CMOS Presettable Up/Down Counters (Dual Clock with Reset)	F	3A	16
			D	3	
40194B	CD40194B	4-Bit Bidirectional Universal Shift Register	D, K	3	16
40257B	CD40257B	Quad 2-Line-to-1-Line Data Selector/Multiplexer	F	3A	16
			D	3	

MIL-I-38535 to Harris Hi-Rel Types Sorted by JAN Type

MIL-I DESIGNATION	HARRIS TYPE
JM38510/05001BCA	CD4011AFB
JM38510/05003BCA	CD4023AFB
JM38510/05051BCA	CD4011BFB
JM38510/05052BCA	CD4012BFB
JM38510/05053BCA	CD4023BFB
JM38510/05101BCA	CD4013AFB
JM38510/05102BEA	CD4027AFB
JM38510/05151BCA	CD4013BFB
JM38510/05152BEA	CD4027BFB
JM38510/05201BCA	CD4000AFB
JM38510/05202BCA	CD4001AFB
JM38510/05204BCA	CD4025AFB
JM38510/05252BCA	CD4001BFB
JM38510/05254BCA	CD4025BFB

MIL-I DESIGNATION	HARRIS TYPE
JM38510/05301BCA	CD4007AFB
JM38510/05302BEA	CD4019AFB
JM38510/05352BEA	CD4019BFB
JM38510/05353BCA	CD4030BFB
JM38510/05503BEA	CD4049AFB
JM38510/05504BEA	CD4050AFB
JM38510/05553BEA	CD4049UBFB
JM38510/05554BEA	CD4050BFB
JM38510/05601BEA	CD4017AFB
JM38510/05603BEA	CD4020AFB
JM38510/05605BCA	CD4024AFB
JM38510/05651BEA	CD4017BFB
JM38510/05652BEA	CD4018BFB
JM38510/05653BEA	CD4020BFB

MIL-I DESIGNATION	HARRIS TYPE
JM38510/05655BCA	CD4024BFB
JM38510/05754BEA	CD4021BFB
JM38510/05852BCA	CD4066BFB
JM38510/17001BCA	CD4081BFB
JM38510/17002BCA	CD4082BFB
JM38510/17003BCA	CD4073BFB
JM38510/17101BCA	CD4071BFB
JM38510/17103BCA	CD4075BFB
JM38510/17203BCA	CD4070BFB
JM38510/17401BCA	CD4069UBFB
JM38510/17403BEA	CD4502BFB
JM38510/17504BEA	CD4098BFB
JM38510/17601BEA	CD4099BFB

SMD or DESC Parts List

SMD OR DESC NUMBER	HARRIS PART NUMBER
7702002EA	CD4502BF3A
7702301EA	CD4520BF3A
7702402CA	CD4081BF3A
7702501EA	CD4094BF3A
7703201JA	CD4515BF3A
7703702EA	CD4585BF3A
7704402CA	CD4078BF3A
7704403CA	CD4002BF3A
7704701EA	CD4555BF3A
7704801EA	CD4556BF3A
7705102CA	CD4073BF3A
7705902CA	CD4082BF3A
7706002CA	CD4072BF3A
8101602EA	CD4029BF3A
8101801EA	CD4053BF3A
8102001CA	CD4047BF3A
5962-9064001CA	CD4016BF3A
5962-9055701EA	CD14538BF3A
7704602CA	CD4093BF3A
7901502EA	CD4052BF3A
8101701EA	CD4035BF3A

NOTE:

1. Product is dual branded with SMD/DESC and Harris part number.

Lot Screening Tests

The Total Lot Screening Table indicates the screening performed on JAN B, 3 and 3A devices. 3 and 3A are equivalent to MIL-STD-883 Class B screens to Method 5004. As shown in the Manufacturing and Conformance Testing table, the differences between a 3 and 3A is the lead finish and pellet mounting technique. It should be noted that all CD4XXXB-Series wafers are manufactured at the Harris JAN certified plant in Findlay, Ohio and any JAN type manufactured in the U.S. is completely assembled and tested on our JAN-certified line.

Total Lot Screening For High-Reliability CD4000B Series ICs

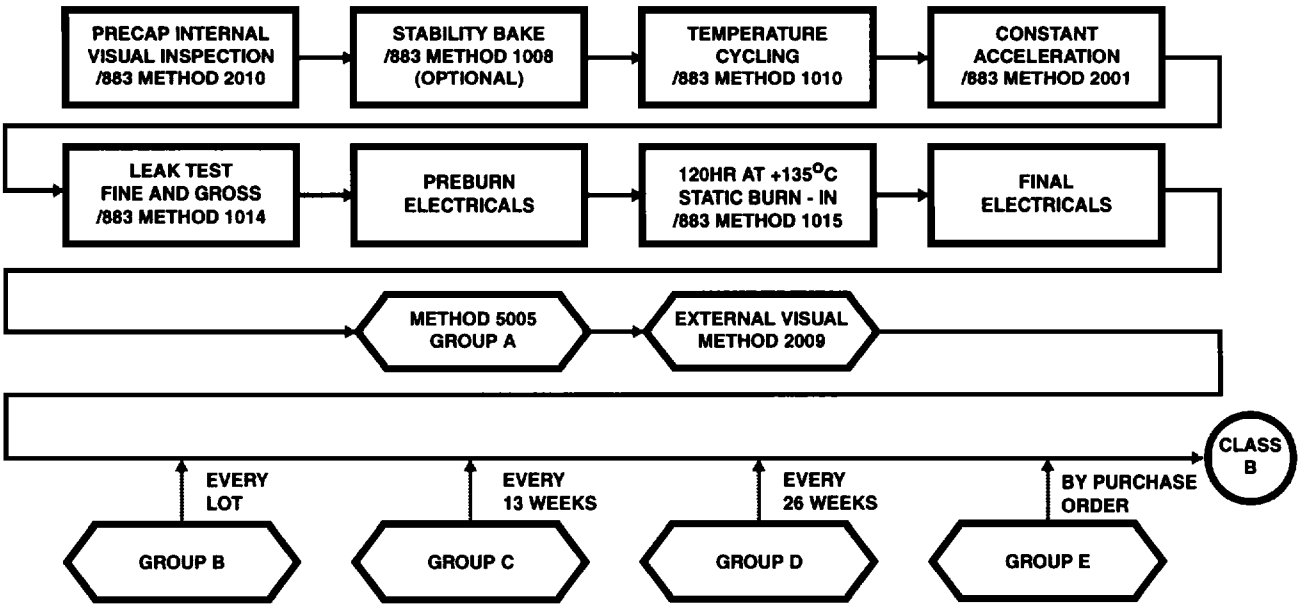
SCREENING TESTS	TEST CONDITIONS	METHOD	PRODUCT JAN B, 3, 3A, AND SMD	NOTES
Pre-Cap Visual at Assembly	Condition B	2010	X	-
PRECONDITIONING				
Stabilization Bake (Optional)	Condition C	1008	X	-
Temperature Cycle	Condition C	1010	X	-
Centrifuge	Condition E, Y1 Only	2001	X	-
Fine Leak	Condition B	1014	X	-
Gross Leak	Condition C	1014	X	-
TEST AND BURN-IN				
Initial Test		-	X	1
Static Burn-In 2 120 Hours	+135°C Inputs at V_{DD}, Outputs Open	1015	X	1, 2, 3, 4
Final Elec DC +25°C		-	X	-
Final Elec DC+125°C		-	X	-
Final Elec DC -55°C		-	X	-
Final Elec AC +25°C		-	X	-
FINAL INSPECTION				
Quality Conformance Inspection (Group A)		5005	X	-
100% Visual Inspect		2009	X	-

NOTES:

1. See individual data bulletins for electrical testing of specific types or JAN Slash Sheets as applicable.
2. Alternate time/temp regression used per /883 Method 1015.
3. PDA for 3 and 3A is 5%, one reburn allowed at 3%.
4. PDA's are based on Group A subgroup 1.

Product Flow Diagrams

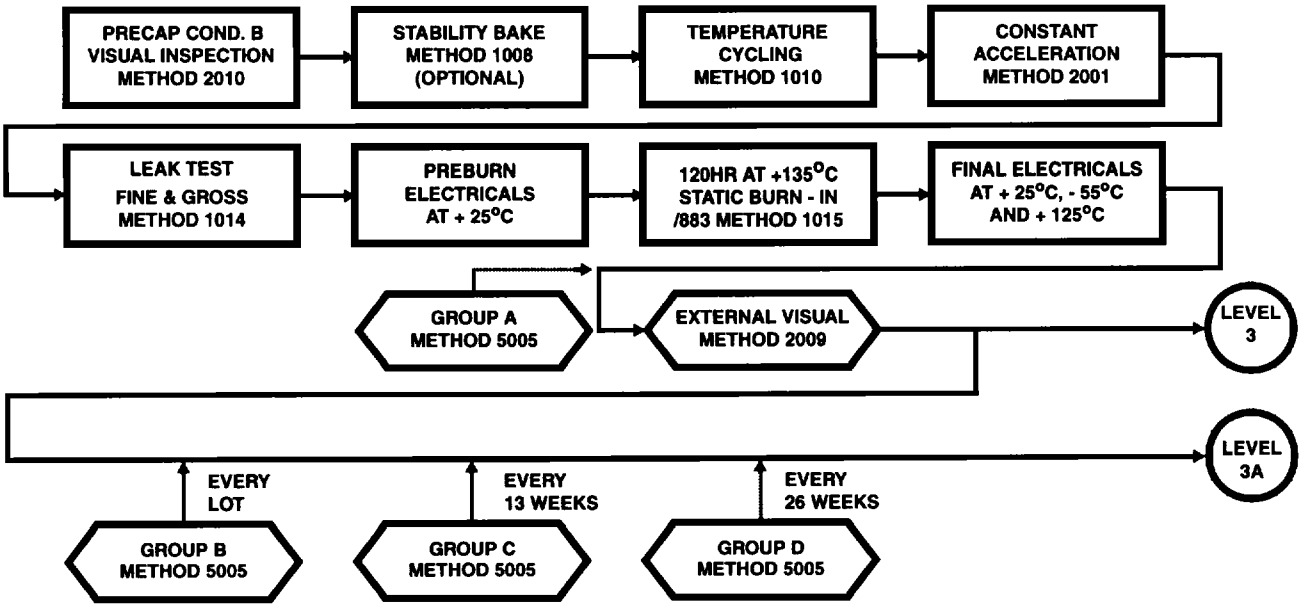
JAN CLASS B CMOS ICs



Class B Screening Tests

- Precap Visual Inspection
- Stability Bake (Optional)
- Temperature Cycling
- Constant Acceleration
- Fine and Gross Leak Tests
- Preburn Electrical
- 120 Hour Static Burn-In at +135°C
- Final Electrical
- External Visual

SMD, DESC, LEVEL 3, AND LEVEL 3A



Absolute Maximum Ratings

DC Supply-Voltage Range, V_{DD}
(Voltages Referenced to V_{SS} Terminal) ..... -0.5V to +20V
Input Voltage Range, All Inputs ..... -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input ..... ±10mA
Operating Temperature Range, T_A
Package Types D, F, K ..... -55°C to +125°C
Storage Temperature Range, T_{STG} ..... -65°C to +150°C
Lead Temperature (During Soldering)
At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)
From Case for 10s Maximum ..... +265°C

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
Package Types D and F	83.3°C/W	28°C/W
Package Type K	83.3°C/W	22°C/W

Maximum Power Dissipation Per Package, P_D
For T_A = -55°C to +100°C,
Package Types D, F, K 500mW
For T_A = +100°C to +125°C,
Package Types D, F, K ..... Derate Linearly at 12mW/°C to 200mW
Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
All Package Types 100mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

Supply Voltage Range
For T_A = Full Package Temperature Range ..... 3V to 18V

Device Classification for Leakage Current

The table below classifies the levels of device leakage as SSI, MSI-1 and MSI-2. In order to determine the limits which apply to specific device type, consult the Standard DC Electrical Specifications table.

Classification According To Circuit Complexity

GATES/INVERTERS (SSI)		BUFFERS/FLIP-FLOPS/ LATCHES/MULTILEVEL GATES (MSI-1)		COMPLEX LOGIC (MSI-2)		
CD4000B	CD4025B	CD4009UB (Note 1)	CD4085B	CD4006B	CD4056B (Note 1)	CD4541B
CD4000UB	CD4025UB	CD4010B (Note 1)	CD4086B	CD4008B	CD4060B	CD4555B
CD4001B	CD4048B	CD4013B	CD4093B (Note 1)	CD4014B	CD4063B	CD4556B
CD4001UB	CD4066B (Note 1)	CD4019B	CD4095B	CD4015B (Note 1)	CD4067B (Note 1)	CD4585B
CD4002B	CD4068B	CD4027B	CD4096B	CD4017B	CD4076B	CD4724B
CD4002UB	CD4069UB	CD4030B	CD4098B	CD4018B	CD4089B	CD14538B
CD4007UB	CD4071B	CD4041UB (Note 1)	CD4502B (Note 1)	CD4020B	CD4094B	CD40100B
CD4011B	CD4072B	CD4042B	CD4503B (Note 1)	CD4021B	CD4097B (Note 1)	CD40101B
CD4011UB	CD4073B	CD4043B	CD4504B (Note 1)	CD4022B	CD4099B	CD40102B
CD4012B	CD4075B	CD4044B	CD40106B (Note 1)	CD4024B	CD4508B	CD40103B
CD4016B (Note 1)	CD4078B	CD4047B	CD40107B (Note 1)	CD4028B	CD4510B	CD40104B
	CD4081B	CD4049UB (Note 1)	CD40109B (Note 1)	CD4029B	CD4511B (Note 1)	CD40105B
CD4023B	CD4082B	CD4050B (Note 1)	CD40174B	CD4031B (Note 1)	CD4512B	CD40108B
CD4023UB		CD4070B	CD40175B	CD4033B	CD4514B	CD40116 (Note 1)
		CD4077B	CD40257B	CD4034B	CD4515B	CD40160B
				CD4035B	CD4516B	CD40161B
				CD4040B	CD4517B	CD40163B
				CD4046B (Note 1)	CD4518B	CD40192B
				CD4051B (Note 1)	CD4520B	CD40193B
				CD4052B (Note 1)	CD4527B	CD40194B
				CD4053B (Note 1)	CD4532B	
				CD4054B (Note 1)	CD4536B	

NOTE:

1. Indicates type for which, because of design requirements, one or more DC Specifications differ from the standardized data. These differences are defined in separate DC Electrical Specifications table.

DC Electrical Specifications - Standard "B" Series Devices

For all CD4000B Series Standard Output CMOS Devices. Parameters are 100% Tested Unless Otherwise Specified.

PARAMETERS		TEST CONDITIONS			-55°C		+25°C		+125°C		UNITS
		V_O	V_{IN}	V_{DD}	MIN	MAX	MIN	MAX	MIN	MAX	
Functional Test (Notes 1 and 2)		-	-	-	-	-	-	-	-	-	
Quiescent Device Current I_{DD} See Classification Table	SSI Types (Note 3)	-	0, 5	5	-	0.25 (Note 2)	-	0.25 (Note 2)	-	7.5 (Note 2)	µA
		-	0, 10	10	-	0.5 (Note 2)	-	0.5 (Note 2)	-	15 (Note 2)	µA
		-	0, 15	15	-	1 (Note 2)	-	1 (Note 2)	-	30 (Note 2)	µA
		-	0, 20	20	-	5	-	5	-	150	µA
	MSI-1 (Note 3 and Note 4)	-	0, 5	5	-	1 (Note 2)	-	1 (Note 2)	-	30 (Note 2)	µA
		-	0, 10	10	-	2 (Note 2)	-	2 (Note 2)	-	60 (Note 2)	µA
		-	0, 15	15	-	4 (Note 2)	-	4 (Note 2)	-	120 (Note 2)	µA
		-	0, 20	20	-	20	-	20	-	600	µA
	MSI-2 (Note 3)	-	0, 5	5	-	5 (Note 2)	-	5 (Note 2)	-	150 (Note 2)	µA
		-	0, 10	10	-	10 (Note 2)	-	10 (Note 2)	-	300 (Note 2)	µA
		-	0, 15	15	-	20 (Note 2)	-	20 (Note 2)	-	600 (Note 2)	µA
		-	0, 20	20	-	100	-	100	-	3000	µA
Output Low Drive Current, I_{OL} Min		0.4	0, 5	5	0.64 (Note 2)	-	0.51	-	0.36 (Note 2)	-	mA
		0.5	0, 10	10	1.6 (Note 2)	-	1.3	-	0.9 (Note 2)	-	mA
		1.5	0, 15	15	4.2 (Note 2)	-	3.4	-	2.4 (Note 2)	-	mA
Output High Drive Current, I_{OH} Min		4.6	0, 5	5	-0.64	-	-0.51	-	-0.36 (Note 2)	-	mA
		2.5	0, 5	5	-2.0	-	-1.6	-	-1.15 (Note 2)	-	mA
		9.5	0, 10	10	-1.6	-	-1.3	-	-0.9 (Note 2)	-	mA
		13.5	0, 15	15	-4.2	-	-3.4	-	-2.4 (Note 2)	-	mA

DC Electrical Specifications - Standard "B" Series Devices (Continued)

For all CD4000B Series Standard Output CMOS Devices. Parameters are 100% Tested Unless Otherwise Specified.

PARAMETERS		TEST CONDITIONS			-55°C		+25°C		+125°C		UNITS
		V_O	V_{IN}	V_{DD}	MIN	MAX	MIN	MAX	MIN	MAX	
Output Voltage Low-Level, V_{OL} Max		-	0, 5	5	-	0.05 (Note 2)	-	0.05 (Note 2)	-	0.05 (Note 2)	V
		-	0, 10	10	-	0.05 (Note 2)	-	0.05 (Note 2)	-	0.05 (Note 2)	V
		-	0, 15	15	-	0.05	-	0.05	-	0.05	V
Output Voltage High-Level, V_{OH} Min		-	0, 5	5	4.95 (Note 2)	-	4.95 (Note 2)	-	4.95	-	V
		-	0, 10	10	9.95 (Note 2)	-	9.95 (Note 2)	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	14.95	-	V
Input Low Voltage V_{IL} Max	Buffered (B)	4.5	-	5	-	1.5	-	1.5	-	1.5	V
		9	-	10	-	3 (Note 2)	-	3	-	3	V
		13.5	-	15	-	4	-	4	-	4	V
	Unbuffered (UB)	4.5	-	5	-	1 (Note 2)	-	1	-	1	V
		9	-	10	-	2	-	2	-	2	V
		13.5	-	15		2.5		2.5		2.5	V
Input High Voltage V_{IH} Min	Buffered (B)	0.5, 4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	11	-	V
	Unbuffered (UB)	0.5, 4.5	-	5	4	-	4	-	4	-	V
		1, 9	-	10	8	-	8	-	8	-	V
		1.5, 13.5	-	15	12.5	-	12.5	-	12.5	-	V
Input Current I_{IN} (Note 3)		-	0, 20	20	-	±0.1	-	±0.1	-	±1	µA
Three-State Output Leakage Current, I_{OUT} (Note 3 and Note 5)		0, 20	0, 20	20	-	±0.4	-	±0.4	-	±12	µA

NOTES:

1. At +25°C V_{IN} = 0 - 20V, V_{DD} = 20V; +125°C V_{IN} = 0 -18V, V_{DD} = 18V; and at -55°C V_{IN} = 0 - 3V, V_{DD} = 3V.
2. These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
3. At -55°C, test is performed with V_{DD} of 18V.
4. CD4047B - Maximum DC supply voltage V_{DD} is 13V for radiation hardened version of this type when operating with RC network.
5. For applicable devices only.

Non-Standard DC Electrical Specifications

The table below indicates all devices which are considered to be non-standard. Non-standard devices are types such as bilateral switches (CD4066B), multiplexers (CD4051B), special sink or source currents (CD4049UB, CD4050B) and open drain buffer/drivers (CD40107B) which exhibit non-standard outputs or special parameters. This table shows the 100% electrical tests that are performed on these specialized devices. These tests take the place of corresponding parameters in the Standard Electrical Specifications table. For the types listed with R_{ON} tests, drive current and output voltage tests should be deleted from the Standard Electrical Specifications table.

Non-Standard DC Electrical Specifications "B" Series Devices

PARAMETERS	TEST CONDITIONS			-55°C	+25°C		+125°C	UNITS
	V_O	V_{IN}	V_{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	
CD4009UB, CD4010B								
Output Low Drive Current, I_{OL} Min (Note 2)	0.4	0, 5	4.5	3.2	2.6	-	1.8	mA
	0.4	0, 5	5	3.75	3 (Note 1)	-	2.1	mA
	0.5	0, 10	10	10.0	8 (Note 1)	-	5.6	mA
	1.5	0, 15	15	30.0	24 (Note 1)	-	16.0	mA
Output High Drive Current, I_{OH} Min (Note 2)	4.6	0, 5	5	-0.25	-0.2 (Note 1)	-	-0.15	mA
	2.5	0, 5	5	-1.0	-0.8 (Note 1)	-	-0.58	mA
	9.5	0, 10	10	-0.55	-0.45 (Note 1)	-	-0.33	mA
	13.5	0, 15	15	-1.65	-1.5 (Note 1)	-	-1.1	mA
CD4016B								
Control Input Voltage Low, V_{IL} Max (Note 2)	$V_{IS} = V_{SS}$, $V_{OS} = V_{DD}$ $V_{IS} = V_{DD}$, $V_{OS} = V_{SS}$ $\|I_{IS}\| < 10\mu A$		5	0.9 (Note 1)	-	0.7 (Note 1)	0.4 (Note 1)	V
			10	0.9	-	0.7	0.4	V
			15	0.9 (Note 1)	-	0.7 (Note 1)	0.4 (Note 1)	V
Control Input Voltage High, V_{IH} Min (Note 2)	-		5	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	V
			10	7.0	7.0	-	7.0	V
			15	11.0 (Note 1)	11.0 (Note 1)	-	11.0 (Note 1)	V
On-State Resistance, R_{ON} Max R_L = 10K Returned to $V_{DD} - V_{SS}/2$ (Note 2)	$V_{IS} = V_{DD}$ or V_{SS} V_{IS} = 4.75 or 5.75 $V_{IS} = V_{DD}$ or V_{SS} V_{IS} = 7.25 or 7.75		10	600 (Note 1)	-	660 (Note 1)	960 (Note 1)	Ω
			10	1870 (Note 1)	-	2000 (Note 1)	2600 (Note 1)	Ω
			15	360 (Note 1)	-	400 (Note 1)	600 (Note 1)	Ω
			15	775 (Note 1)	-	850 (Note 1)	1230 (Note 1)	Ω

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

PARAMETERS	TEST CONDITIONS			-55°C	+25°C		+125°C	UNITS
	V_O	V_{IN}	V_{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	
CD4031B								
Output Low Drive Current, I_{OL} Min Q (Note 2)	0.4	0, 5	5	2.56	2.04 (Note 1)	-	1.44	mA
	0.5	0, 10	10	6.4	5.2 (Note 1)	-	3.6	mA
	1.5	0, 15	15	16.8	13.6 (Note 1)	-	9.6	mA
$\overline{Q}$, Q', C_{LD} (Note 2)	0.4	0, 5	5	0.64	0.51 (Note 1)	-	0.36	mA
	0.5	0, 10	10	1.6	1.3 (Note 1)	-	0.9	mA
	1.5	0, 15	15	4.2	3.4 (Note 1)	-	2.4	mA
Output High Drive Current, I_{OH} Min Q, $\overline{Q}$, Q', C_{LD} (Note 2)	4.6	0, 5	5	-0.64	-0.51 (Note 1)	-	-0.36	mA
	2.5	0, 5	5	-2.0	-1.6 (Note 1)	-	-1.15	mA
	9.5	0, 10	10	-1.6	-1.3 (Note 1)	-	-0.9	mA
	13.5	0, 15	15	-4.2	-3.4 (Note 1)	-	-2.4	mA
CD4041UB								
Output Low Drive Current, I_{OL} Min (Note 2)	0.4	0, 5	5	2.1	1.6 (Note 1)	-	1.2	mA
	0.5	0, 10	10	6.25	5 (Note 1)	-	3.5	mA
	1.5	0, 15	15	24	19 (Note 1)	-	13	mA
Output High Drive Current, I_{OH} Min (Note 2)	4.6	0, 5	5	-2.1	-1.6 (Note 1)	-	-1.2	mA
	2.5	0, 5	5	-8.4	-6.4 (Note 1)	-	-4.6	mA
	9.5	0, 10	10	-6.25	-5 (Note 1)	-	-3.5	mA
	13.5	0, 15	15	-24	-19 (Note 1)	-	-13	mA
CD4046B								
Zener Diode Voltage (V_Z) (Note 3)	I_Z = 50μA			-	4.45 (Note 1)	6.5 (Note 1)	-	V
Quiescent Leakage, Phase Comparator Pin 14 Open, Pin 5 = V_{DD} (Note 3)	-	0, 5	5	0.2	-	0.2	-	mA
	-	0, 10	10	1.0	-	1.0	-	mA
	-	0, 15	15	1.5	-	1.5	-	mA
	-	0, 20	20	4.0 (Note 1)	-	4.0 (Note 1)	-	mA

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

PARAMETERS	TEST CONDITIONS			-55°C	+25°C		+125°C	UNITS
	V_O	V_{IN}	V_{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	
CD4046B (Continued)								
Quiescent Leakage, Phase Comparator Pin 14 = V_{SS} or V_{DD}, Pin 5 = V_{DD} (Note 3)	-	0, 5	5	20	-	20	-	µA
	-	0, 10	10	40	-	40	-	µA
	-	0, 15	15	80	-	80	-	µA
	-	0, 20	20	160 (Note 1)	-	160 (Note 1)	-	µA
CD4049UB, CD4050B								
Output Low Drive Current, I_{OL} Min (Note 2)	0.4	0, 5	4.5	3.3	2.6 (Note 1)	-	1.8	mA
	0.4	0, 5	5	4.0	3.2 (Note 1)	-	2.4	mA
	0.5	0, 10	10	10	8.0 (Note 1)	-	5.6	mA
	1.5	0, 15	15	26	24 (Note 1)	-	18	mA
Output High Drive Current, I_{OH} Min (Note 2)	4.6	0, 5	5	-0.81	-0.8 (Note 1)	-	-0.48	mA
	2.5	0, 5	5	-2.6	-3.2 (Note 1)	-	-1.55	mA
	9.5	0, 10	10	-2.0	-1.8 (Note 1)	-	-1.18	mA
	13.5	0, 15	15	-5.2	-6.0 (Note 1)	-	-3.1	mA
CD4051B, CD4052B, CD4053B, CD4067B, CD4097B								
ON-State Resistance, R_{ON} Max (Note 3)	R_L = 10K Returned to $V_{DD} - V_{SS}/2$ $V_{IS} = V_{SS}$ to V_{DD}		5	800 (Note 1)	-	1050 (Note 1)	1300 (Note 1)	Ω
			10	310 (Note 1)	-	400 (Note 1)	500 (Note 1)	Ω
			15	200 (Note 1)	-	240 (Note 1)	320 (Note 1)	Ω
Input Voltage Low, V_{IL} Max (Note 2)	$V_{EE} = V_{SS}$ R_L = 1K to V_{SS} $\|I_{IS}\| < 2\mu A$		5	1.5 (Note 1)	-	1.5 (Note 1)	1.5 (Note 1)	V
			10	3.0	-	3.0	3.0	V
			15	4.0 (Note 1)	-	4.0 (Note 1)	4.0 (Note 1)	V
Input Voltage High, V_{IH} Min (Note 2)	$V_{EE} = V_{SS}$ R_L = 1K to V_{SS} $\|I_{IS}\| < 2\mu A$		5	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	V
			10	7.0	7.0	-	7.0	V
			15	11.0 (Note 1)	11.0 (Note 1)	-	11.0 (Note 1)	V
Off Channel Leakage Current Any Channel Off Max (Note 3)	V_{SS} = 0	V_{EE} = 0	18	±100 (Note 1)	-	±100 (Note 1)	±1000 (Note 1)	nA
Off Channel Leakage Current All Channels (Common Out/In) Off Max (Note 3)	V_{SS} = 0	V_{EE} = 0	18	±100 (Note 1)	-	±100 (Note 1)	±1000 (Note 1)	nA

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

PARAMETERS			TEST CONDITIONS			-55°C	+25°C		+125°C	UNITS
			V_O	V_{IN}	V_{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	
CD4054B, CD4056B										
	V_{EE}	V_{SS}								
Output Low (Sink) Current, I_{OL} (Note 2)	-5	0	-4.5	-	5	0.98	0.8 (Note 1)	-	0.55	mA
	0	0	0.5	-	10	0.98	0.8 (Note 1)	-	0.55	mA
	0	0	1.5	-	15	3.6	2.9 (Note 1)	-	2	mA
Output High (Source) Current, I_{OH} (Note 2)	-5	0	4.5	-	5	-0.6	-0.45 (Note 1)	-	-0.3	mA
	0	0	9.5	-	10	-0.6	-0.45 (Note 1)	-	-0.3	mA
	0	0	13.5	-	15	-1.9	-1.5 (Note 1)	-	-1.1	mA
CD4066B										
On-State Resistance, R_{ON} Max (Note 3)			R_L = 10K Returned to $V_{DD} - V_{SS}/2$ $V_{IS} = V_{SS}$ to V_{DD}		5	800 (Note 1)	-	1050 (Note 1)	1300 (Note 1)	Ω
					10	310 (Note 1)	-	400 (Note 1)	550 (Note 1)	Ω
					15	200 (Note 1)	-	240 (Note 1)	320 (Note 1)	Ω
Control Input Voltage Low, V_{ILC} Max (Note 2)			$V_{IS} = V_{SS}$, $V_{OS} = V_{DD}$, $V_{IS} = V_{DD}$, $V_{OS} = V_{SS}$ $\|I_{IS}\| < 10\mu A$		5	1.0 (Note 1)	-	1.0 (Note 1)	1.0 (Note 1)	V
					10	2.0	-	2.0	2.0	V
					15	2.0 (Note 1)	-	2.0 (Note 1)	2.0 (Note 1)	V
Control Input Voltage High, V_{IHC} Min (Note 2)			-		5	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	V
					10	7.0	7.0	-	7.0	V
					15	11.0 (Note 1)	11.0 (Note 1)	-	11.0 (Note 1)	V
Input/Output Leakage Current (Switch Off) Effective Off Resistance $V_C = V_{SS}$ (Note 3)			0	0	18	±100	-	±100	±1000	nA
CD4093B										
Positive Trigger Threshold Voltage (Note 3)	V_P Min		-	(Note 4)	5	2.2 (Note 1)	2.2 (Note 1)	-	2.2 (Note 1)	V
			-	(Note 4)	10	4.6	4.6	-	4.6	V
			-	(Note 4)	15	6.8 (Note 1)	6.8 (Note 1)	-	6.8 (Note 1)	V
			-	(Note 5)	5	2.6 (Note 1)	2.6 (Note 1)	-	2.6 (Note 1)	V
			-	(Note 5)	10	5.6	5.6	-	5.6	V
			-	(Note 5)	15	6.3	6.3	-	6.3	V

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

PARAMETERS		TEST CONDITIONS V_O	TEST CONDITIONS V_{IN}	TEST CONDITIONS V_{DD}	-55°C MIN/MAX	+25°C MIN	+25°C MAX	+125°C MIN/MAX	UNITS
CD4093B (Continued)									
Positive Trigger Threshold Voltage (Note 3)	V_P Max	-	(Note 4)	5	3.6 (Note 1)	-	3.6 (Note 1)	3.6 (Note 1)	V
		-	(Note 4)	10	7.1	-	7.1	7.1	V
		-	(Note 4)	15	10.8 (Note 1)	-	10.8 (Note 1)	10.8 (Note 1)	V
		-	(Note 5)	5	4 (Note 1)	-	4 (Note 1)	4 (Note 1)	V
		-	(Note 5)	10	8.2	-	8.2	8.2	V
		-	(Note 5)	15	12.7	-	12.7	12.7	V
Negative Trigger Threshold Voltage (Note 3)	V_N Min	-	(Note 4)	5	0.9 (Note 1)	0.9 (Note 1)	-	0.9 (Note 1)	V
		-	(Note 4)	10	2.5	2.5	-	2.5	V
		-	(Note 4)	15	4 (Note 1)	4 (Note 1)	-	4 (Note 1)	V
		-	(Note 5)	5	1.4 (Note 1)	1.4 (Note 1)	-	1.4 (Note 1)	V
		-	(Note 5)	10	3.4	3.4	-	3.4	V
		-	(Note 5)	15	4.8	4.8	-	4.8	V
	V_N Max	-	(Note 4)	5	2.8 (Note 1)	-	2.8 (Note 1)	2.8 (Note 1)	V
		-	(Note 4)	10	5.2	-	5.2	5.2	V
		-	(Note 4)	15	7.4 (Note 1)	-	7.4 (Note 1)	7.4 (Note 1)	V
		-	(Note 5)	5	3.2 (Note 1)	-	3.2 (Note 1)	3.2 (Note 1)	V
		-	(Note 5)	10	6.6	-	6.6	6.6	V
		-	(Note 5)	15	9.6	-	9.6	9.6	V
Hysteresis Voltage (Note 3)	V_H Min	-	(Note 4)	5	0.3 (Note 1)	0.3 (Note 1)	-	0.3 (Note 1)	V
		-	(Note 4)	10	1.2	1.2	-	1.2	V
		-	(Note 4)	15	1.6 (Note 1)	1.6 (Note 1)	-	1.6 (Note 1)	V
		-	(Note 5)	5	0.3 (Note 1)	0.3 (Note 1)	-	0.3 (Note 1)	V
		-	(Note 5)	10	1.2	1.2	-	1.2	V
		-	(Note 5)	15	1.6	1.6	-	1.6	V

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

PARAMETERS		TEST CONDITIONS			-55°C	+25°C		+125°C	UNITS
		V_O	V_{IN}	V_{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	
CD4093B (Continued)									
Hysteresis Voltage (Note 3)	V_H Max	-	(Note 4)	5	1.6 (Note 1)	-	1.6 (Note 1)	1.6 (Note 1)	V
		-	(Note 4)	10	3.4	-	3.4	3.4	V
		-	(Note 4)	15	5 (Note 1)	-	5 (Note 1)	5 (Note 1)	V
		-	(Note 5)	5	1.6 (Note 1)	-	1.6 (Note 1)	1.6 (Note 1)	V
		-	(Note 5)	10	3.4	-	3.4	3.4	V
		-	(Note 5)	15	5	-	5	5	V
CD4502B									
Output Low Drive Current, I_{OL} Min (Note 2)		0.4	0, 5	5	3.84	3.06 (Note 1)	-	2.16	mA
		0.5	0, 10	10	9.6	7.8 (Note 1)	-	5.4	mA
		1.5	0, 15	15	25.2	20.4 (Note 1)	-	14.4	mA
CD4503B									
Output Low Drive Current, I_{OL} Min (Note 2)		0.4	0	5	2.6	2.1 (Note 1)	-	1.3	mA
		0.5	0	10	6.5	5.5 (Note 1)	-	3.8	mA
		1.5	0	15	19.2	16.1 (Note 1)	-	11.2	mA
Output High Drive Current, I_{OH} Min (Note 2)		4.6	5	5	-1.2	-1.02 (Note 1)	-	-0.7	mA
		2.5	5	5	-5.8	-4.8 (Note 1)	-	-3.0	mA
		9.5	10	10	-3.1	-2.6 (Note 1)	-	-1.8	mA
		13.5	15	15	-8.2	-6.8 (Note 1)	-	-4.8	mA
CD4504B									
		V_{CC}							
Input Low Voltage V_{IL} Max (Note 2)	TTL-CMOS	5	1	-	10	0.8	-	0.8	0.8	V
	TTL-CMOS	5	1	-	15	0.8 (Note 1)	-	0.8 (Note 1)	0.8 (Note 1)	V
	CMOS-CMOS	5	1	-	10	1.5 (Note 1)	-	1.5 (Note 1)	1.5 (Note 1)	V
	CMOS-CMOS	5	1.5	-	15	1.5	-	1.5	1.5	V
	CMOS-CMOS	10	1.5		15	3 (Note 1)	-	3 (Note 1)	3 (Note 1)	V

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

PARAMETERS			TEST CONDITIONS			-55°C	+25°C		+125°C	UNITS
			V_O	V_{IN}	V_{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	
CD4504B (Continued)										
Input High Voltage V_{IH} Min (Note 2)	TTL-CMOS	5	9	-	10	2	2	-	2	V
	TTL-CMOS	5	13.5	-	15	2 (Note 1)	2 (Note 1)	-	2 (Note 1)	V
	CMOS-CMOS	5	9	-	10	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	V
	CMOS-CMOS	5	13.5	-	15	3.5	3.5	-	3.5	V
	CMOS-CMOS	10	13.5		15	7 (Note 1)	7 (Note 1)	-	7 (Note 1)	V
CD4511B										
Output Voltage High-Level, V_{OH} Min (Note 3)			-	0, 5	5	4	4.1	-	4.2	V
			-	0, 10	10	9	9.1	-	9.2	V
			-	0, 15	15	14 (Note 1)	14.1 (Note 1)	-	14.2 (Note 1)	V
	I_{OH} (mA)									
Output Drive Voltage High Level, V_{OH} Min (Note 3)	0		-	-	5	4.0	4.1	-	4.2	V
	5		-	-	5	-	-	-	-	V
	10		-	-	5	3.8	3.9	-	3.9	V
	15		-	-	5	-	-	-	3.5	V
	20		-	-	5	3.55	3.4 (Note 1)	-	-	V
	25		-	-	5	3.4	3.1	-	-	V
Output Drive Voltage High Level, V_{OH} Min (Note 3)	0		-	-	10	9.0	9.1	-	9.2	V
	5		-	-	10	-	-	-	-	V
	10		-	-	10	8.85	9.0	-	9.0	V
	15		-	-	10	-	-	-	-	V
	20		-	-	10	8.7	8.6 (Note 1)	-	8.4	V
	25		-	-	10	8.6	8.3	-	-	V
Output Drive Voltage High Level, V_{OH} Min (Note 3)	0		-	-	15	14.0	14.10	-	14.20	V
	5		-	-	15	-	-	-	-	V
	10		-	-	15	13.90	14.0	-	14.0	V
	15		-	-	15	-	-	-	-	V
	20		-	-	15	13.75	13.70 (Note 1)	-	13.50	V
	25		-	-	15	13.65	13.50	-	-	V

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

PARAMETERS		TEST CONDITIONS			-55°C	+25°C		+125°C	UNITS
		V_O	V_{IN}	V_{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	
CD4541B									
Output Low Drive Current, I_{OL} Min (Note 2)		0.4	0, 5	5	1.9	1.55 (Note 1)	-	1.08	mA
		0.5	0, 10	10	5.0	4.0 (Note 1)	-	2.8	mA
		1.5	0, 15	15	12.6	10.0 (Note 1)	-	7.2	mA
Output High Drive Current, I_{OH} Min (Note 2)		4.6	0, 5	5	-1.9	-1.55 (Note 1)	-	-1.08	mA
		2.5	0, 5	5	-6.2	-5.0 (Note 1)	-	-3.0	mA
		9.5	0, 10	10	-5.0	-4.0 (Note 1)	-	2.8	mA
		13.5	0, 15	15	-12.6	-10.0 (Note 1)	-	-7.2	mA
CD40106B									
Positive Trigger Threshold Voltage (Note 3)	V_P Min	-	-	5	2.2 (Note 1)	2.2 (Note 1)	-	2.2 (Note 1)	V
		-	-	10	4.6 (Note 1)	4.6 (Note 1)	-	4.6 (Note 1)	V
		-	-	15	6.8 (Note 1)	6.8 (Note 1)	-	6.8 (Note 1)	V
	V_P Max	-	-	5	3.6 (Note 1)	-	3.6 (Note 1)	3.6 (Note 1)	V
		-	-	10	7.1 (Note 1)	-	7.1 (Note 1)	7.1 (Note 1)	V
		-	-	15	10.8 (Note 1)	-	10.8 (Note 1)	10.8 (Note 1)	V
Negative Trigger Threshold Voltage (Note 3)	V_N Min	-	-	5	0.9 (Note 1)	0.9 (Note 1)	-	0.9 (Note 1)	V
		-	-	10	2.5 (Note 1)	2.5 (Note 1)	-	2.5 (Note 1)	V
		-	-	15	4 (Note 1)	4 (Note 1)	-	4 (Note 1)	V
	V_N Max	-	-	5	2.8 (Note 1)	-	2.8 (Note 1)	2.8 (Note 1)	V
		-	-	10	5.2 (Note 1)	-	5.2 (Note 1)	5.2 (Note 1)	V
		-	-	15	7.4 (Note 1)	-	7.4 (Note 1)	7.4 (Note 1)	V
Hysteresis Voltage (Note 3)	V_H Min	-	-	5	0.3 (Note 1)	0.3 (Note 1)	-	0.3 (Note 1)	V
		-	-	10	1.2 (Note 1)	1.2 (Note 1)	-	1.2 (Note 1)	V
		-	-	15	1.6 (Note 1)	1.6 (Note 1)	-	1.6 (Note 1)	V

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

PARAMETERS	TEST CONDITIONS			-55°C	+25°C		+125°C	UNITS
	V_O	V_{IN}	V_{DD}	MIN/ MAX	MIN	MAX	MIN/ MAX	
CD40106B (Continued)								
Hysteresis Voltage V_H Max (Note 3)	-	-	5	1.6 (Note 1)	-	1.6 (Note 1)	1.6 (Note 1)	V
	-	-	10	3.4 (Note 1)	-	3.4 (Note 1)	3.4 (Note 1)	V
	-	-	15	5 (Note 1)	-	5 (Note 1)	5 (Note 1)	V
CD40107B								
Output Low Current, I_{OL} Min (Note 2)	0.4	0, 5	5	21	16 (Note 1)	-	12	mA
	1	0, 5	5	44	34 (Note 1)	-	25	mA
	0.5	0, 10	10	49	37 (Note 1)	-	28	mA
	1	0, 10	10	89	68 (Note 1)	-	51	mA
	0.5	0, 15	15	66	50 (Note 1)	-	38	mA
Output High Current, I_{OH} Min (Note 2)	NO INTERNAL PULL-UP DEVICE							
Input Low Voltage, V_{IL} Max (Note 2 and Note 6)	V_O	V_{IN}	V_{DD}					
	4.5	-	5	1.5 (Note 1)	-	1.5 (Note 1)	1.5 (Note 1)	V
	9	-	10	3.0	-	3.0	3.0	V
	13.5	-	15	4.0 (Note 1)	-	4.0 (Note 1)	4.0 (Note 1)	V
Input High Voltage V_{IH} Max (Notes 2 and 6)	0.5, 4.5	-	5	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	V
	1, 9	-	10	7.0	7.0	-	7.0	V
	1.5, 13.5	-	15	11 (Note 1)	11 (Note 1)	-	11 (Note 1)	V
CD40109B								
Input Low Voltage, V_{IL} Max (Note 2)	V_O	V_{CC}	V_{DD}					
	1, 9	5	10	1.5 (Note 1)	-	1.5 (Note 1)	1.5 (Note 1)	V
	1.5, 13.5	10	15	3 (Note 1)	-	3 (Note 1)	3 (Note 1)	V
Input High Voltage, V_{IH} Max (Note 2)	1, 9	5	10	3.5 (Note 1)	3.5 (Note 1)	-	3.5 (Note 1)	V
	1.5, 13.5	10	15	7 (Note 1)	7 (Note 1)	-	7 (Note 1)	V

Non-Standard DC Electrical Specifications "B" Series Devices (Continued)

PARAMETERS		TEST CONDITIONS V_O	V_{IN}	V_{DD}	-55°C MIN/MAX	+25°C MIN	+25°C MAX	+125°C MIN/MAX	UNITS
CD40116									
Quiescent Current (Note 3) From V_{DD} Supply I_{DD} Max		Enable = 1 Enable = 0			6.5 (Note 1)	-	5 (Note 1)	5 (Note 1)	mA
From V_{CC} Supply I_{CC} Max					6.5 (Note 1)	-	5 (Note 1)	5 (Note 1)	mA
					100 (Note 1)	-	100 (Note 1)	200 (Note 1)	µA
DATA FLOW - CMOS INPUTS TO TTL OUTPUTS									
Input Current, I_{IN} (Note 2)		V_{IN} = 0, 12V			±60 (Note 1)	-	±60 (Note 1)	±60 (Note 1)	µA
Output Current (Note 2)	I_{OH} Min	V_{OH} = 3V, V_{IL} = 2V			-7.5 (Note 1)	-6 (Note 1)	-	-4.2 (Note 1)	mA
	I_{OL} Min	V_{OL} = 0.4V, V_{IH} = 10V			7.5 (Note 1)	6 (Note 1)	-	4.2 (Note 1)	mA
TTL Three-State Leakage Current, I_{OUT} Max (Note 2)		Enable = 0			±100 (Note 1)	-	±100 (Note 1)	±100 (Note 1)	µA
DATA FLOW - TTL INPUTS TO CMOS OUTPUTS									
Input Current (Note 2)	I_{IL} Max	Any TTL Input V_{IL} = 0 to 0.7V V_{IH} = 2.3V			-600 (Note 1)	-	-500 (Note 1)	-500 (Note 1)	µA
	I_{IH} Max				-450 (Note 1)	-	-350 (Note 1)	-350 (Note 1)	µA
Output Current (Note 2)	I_{OH} Min	V_{OH} = 11.5V, V_{IL} = 0.7V			-4.3 (Note 1)	-3.5 (Note 1)	-	-2.5 (Note 1)	mA
	I_{OL} Min	V_{OL} = 0.5V, V_{IH} = 2.3V			4.3 (Note 1)	3.5 (Note 1)	-	2.5 (Note 1)	mA
CMOS Three-State Output Leakage Current (Note 2 and Note 8)		V_O = 0, 12V, V_{IN} = 0, 5V			±60	-	±60	±60	µA
ENABLE AND DISABLE INPUTS									
Input Current (Note 2)	I_{IL}	V_{IL} = 0 to 0.7V			-600 (Note 1)	-	-500 (Note 1)	-500 (Note 1)	µA
	I_{IH}	V_{IH} = 2.3V (TTL)			-450 (Note 1)	-	-350 (Note 1)	-350 (Note 1)	µA
	I_{IH}	V_{IH} = 12V (CMOS)			60	-	60	60	µA

NOTES:

1. These limits are tested 100%.
2. Replaces a STD parameter.
3. An Additive parameter.
4. Input on terminals 1, 5, 8, 12, or 2, 6, 9, 13; other inputs to V_{DD}.
5. Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD}.
6. Measured with external pull-up resistor, R_L = 10kΩ to V_{DD}.
7. At -55°C, test is performed with V_{DD} of 18V.
8. CMOS Three-State output leakage test is functionally identical to CMOS-to-TTL input current tests.

Switching Characteristics

The table below lists all Harris High-Reliability CD4000B Series devices and shows which switching parameters are 100% tested at final electrical and Group A. In general, Harris tests propagation delay, transition time, and maximum clock frequency at 5V where applicable. Harris warrants all other switching parameters shown in the commercial data sheet. Harris High-Reliability switching tests are performed on a one-input to one-output basis only.

Switching Characteristics at +25°C

TYPE	(NOTE 1) CONDITIONS V_{DD}= 5V, C_L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4000B	-	250	200	-
CD4000UB	-	120	200	-
CD4001B	-	250	200	-
CD4001UB	-	120	200	-
CD4002B	-	250	200	-
CD4002UB	-	120	200	-
CD4006B	-	400	200	2.5
CD4007UB	-	110	200	-
CD4008B	Sum In to Sum Out	800	200	-
	Carry In to Sum Out	740	-	-
	Sum In to Carry Out	400	-	-
	Carry In to Carry Out	200	-	-
CD4009UB	-	140 (Note 1)	350 (Note 1)	-
	-	60 (Note 2)	70 (Note 2	-
CD4010B	-	200 (Note 1)	350 (Note 1)	-
	-	130 (Note 2)	70 (Note 2)	-
CD4011B	-	250	200	-
CD4011UB	-	120	200	-
CD4012B	-	250	200	-
CD4013B	Clock to Q or $\overline{Q}$	300	200	3.5
	Set to Q or Reset to $\overline{Q}$	300 (Note 1)	-	-
	Set to $\overline{Q}$ or Reset to Q	400 (Note 2)	-	-
CD4014B	-	320	200	3

TYPE	(NOTE 1) CONDITIONS V_{DD}= 5V, C_L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4015B	Clock to Q	320	200	3
	Reset to Q	400 (Note 2)	-	-
CD4016B	Sig. Input to Sig. Output	100	-	-
	Turn On	70	-	-
CD4017B	Clock to Out	650	200	2.5
	Clock to Carry Out	600	-	-
	Reset to Out	530	-	-
CD4018B	Clock to Q	400	200	3
	Preset/Reset to Q	550	-	-
CD4019B	-	300	200	-
CD4020B	ϕ to Q1	360	200	3.5
	Qn to Qn + 1	330	-	-
	Reset to Q	280 (Note 2)	-	-
CD4021B	-	320	200	3
CD4022B	Clock to Carry Out	600	200	2.5
	Clock to Decode Out	650	-	-
	Reset to Output	530	-	-
CD4023B	-	250	200	-
CD4024B	ϕ to Q1	360	200	3.5
	Qn to Qn +1	330	-	-
	Reset to Q	280 (Note 2)	-	-
CD4025B	-	250	200	-
CD4025UB	-	120	200	-

Switching Characteristics at +25°C (Continued)

TYPE	(NOTE 1) CONDITIONS V_{DD}= 5V, C_L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4027B	Clock to Q or $\overline{Q}$	300	200	3.5
	Set to Q or Reset to $\overline{Q}$	300 (Note 1)	-	-
	Set to $\overline{Q}$ or Reset to Q	400 (Note 2)	-	-
CD4028B	-	350	200	-
CD4029B	Q Output	500	200	2
	Carry Output	560	-	-
	Preset Enable to Q	470	-	-
	Preset Enable to Carry Out	640	-	-
	Carry Input to Carry Out	340	-	-
CD4030B	-	280	200	-
CD4031B	Clock to $\overline{Q}$	500	200	2
	Clock to Q	500 (Note 1)	-	-
	Clock to Q	380 (Note 2)	-	-
	Clock to Q'	380	-	-
	$\overline{Clock}$ to C_{LD}	200	-	-
CD4033B	Clock to Carry Out	500	200	2.5
	Clock to Decode Out	700	-	-
	Reset to Carry Out	550 (Note 1)	-	-
	Reset to Decode Out	600	-	-
CD4034B	Parallel In to Parallel Out	700	200	2
	AE to "A" Out t_{PLZ}, t_{PZL}, t_{PHZ}, t_{PZH}	400	-	-
CD4035B	Clock to Q	500	200	2
	Reset to Q	460	-	-

TYPE	(NOTE 1) CONDITIONS V_{DD}= 5V, C_L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4040B	ϕ to Q1	360	200	3.5
	Qn to Qn + 1	330	-	-
	Reset to Q	280 (Note 2)	-	-
CD4041UB	-	120	80	-
CD4042B	Data In to Q	220	200	-
	Data In to $\overline{Q}$	300	-	-
	Clock to Q	450	-	-
	Clock to $\overline{Q}$	500	-	-
CD4043B, CD4044B	Set or Reset to Q	300	200	-
	Enable to Q; t_{PHZ}, t_{PZH}	230	-	-
	Enable to Q; t_{PLZ}, t_{PZL}	180	-	-
CD4046B	AC Coupled Signal Input Voltage Sensitivity (Peak to Peak) f_{IN} = 100Hz Sine Wave	360mV Max		
CD4047B	t_R to Q, $\overline{Q}$	1000	200	-
	Astable to Q, $\overline{Q}$	700	-	-
	Retrigger to Q, $\overline{Q}$	600	-	-
	Astable to Oscillator	400	-	-
	Reset to Q, $\overline{Q}$	500	-	-
CD4048B	Ka to Output	600	200	-
CD4049UB	-	120 (Note 1)	160 (Note 1)	-
	-	65 (Note 2)	60 (Note 2)	-
CD4050B	-	140 (Note 1)	160 (Note 1)	-
	-	110 (Note 2)	60 (Note 2)	-
CD4051B	Add to Signal Out	720	-	-

Switching Characteristics at +25°C (Continued)

TYPE	(NOTE 1) CONDITIONS V_{DD}= 5V, C_L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4052B, CD4053B	Inhibit to Signal Out - Channel On	720	-	-
	Inhibit to Signal Out - Channel Ott	450	-	-
CD4054B	V_{EE} = -5V	800	200	-
CD4056B	V_{EE} = -5V	1300	200	-
CD4060B	Input Pulse Operation ϕI to Q4	740	200	3.5
	Qn to Qn + 1	200	-	-
	Reset Operation	360 (Note 2)	-	-
CD4063B	Comparator Input to Output	1250	200	-
	Cascade Input to Output	1000	-	-
CD4066B	Signal Input to Signal Output R_L = 200k, V_C = V_{DD}, V_{SS} = GND, V_{IS} = Square Wave ≡ 5V and t_R, t_F = 20ns	40	-	-
	t_{PDC}; t_{RC}, t_{FC} = 20ns, R_L = 1K and V_{IS} < 5V	70	-	-
CD4067B	Add or inhibit to Signal Out Channel On	650	-	-
	Signal In to Out	60	-	-
CD4068B	-	300	200	-
CD4069UB	-	110	200	-
CD4070B	-	280	200	-
CD4071B, CD4072B, CD4073B, CD4075B	-	250	200	-
CD4076B	Clock to Q	600	200	-
CD4077B	-	280	200	-
CD4078B	-	300	200	3
CD4081B, CD4082B	-	250	200	-

TYPE	(NOTE 1) CONDITIONS V_{DD}= 5V, C_L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4085B, CD4086B	Data	450 (Note 2)	200	-
		620 (Note 1	-	-
	Inhibit	300 (Note 2)	-	-
		500 (Note 1)	-	-
CD4089B	Clock to Out	300	200	1.2
	Clear to Out	760	-	-
	Cascade to Out	180	-	-
CD4093B	-	380	200	-
CD4094B	Clock to Serial Out Qs	600	200	1.25
	Clock to Serial Out Q's	460	-	-
	Clock to Parallel Out	840	-	-
	Strobe to Parallel Out	580	-	-
	Out Enable to Parallel Out, t_{PHZ}, t_{PZH}	280	-	-
	Out Enable to Parallel Out, t_{PLZ}, t_{PZL}	200	-	-
CD4095B, CD4096B	Clock to Output	500	200	3.5
	Set or Reset	300	-	-
CD4097B	Address or Inhibit to Sig Out - Channel On	650	-	-
	Signal In to Out	60	-	-
CD4098B	Trigger to Q, $\overline{Q}$	500	200	-
CD4099B	Data to Output	400	200	-
CD4502B	Data or Inhibit Delay Time	380 (Note 1)	200 (Note 1)	-
		270 (Note 2)	120 (Note 2)	-
	Disable Delay Time, t_{PHZ}	120	-	-
	Disable Delay Time, t_{PZH}	220	-	-

Switching Characteristics at +25°C (Continued)

TYPE	(NOTE 1) CONDITIONS V_{DD}= 5V, C_L = 50pF			PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4502B (Continued)	Disable Delay Time, t_{PLZ}, t_{PZL}			250	-	-
CD4503B	-			150 (Note 1)	90 (Note 1)	-
	-			110 (Note 2)	70 (Note 2)	-
	t_{PHZ}, t_{PZH}			140	-	-
	t_{PLZ}, t_{PZL}			180	-	-
CD4504B	SHIFT MODE	V_{CC}	V_{DD}			
	TTL to CMOS $V_{DD} > V_{CC}$	5	10	280 (Note 2)	-	-
	CMOS to CMOS $V_{DD} > V_{CC}$	5	10	240 (Note 2)	-	-
	CMOS to CMOS $V_{CC} > V_{DD}$	10	5	550 (Note 2)	-	-
	TTL to CMOS $V_{DD} > V_{CC}$	5	10	280 (Note 1)	-	-
	CMOS to CMOS $V_{DD} > V_{CC}$	5	10	240 (Note 1)	-	-
	CMOS to CMOS $V_{CC} > V_{DD}$	10	5	400	-	-
	All Modes t_{THL}, t_{TLH}	-	5	200	-	-
		-	10	100	-	-
CD4508B	Strobe In to Data Out			260	200	-
CD4510B	Clock to Q Output			400	200	2
	Preset or Reset to Q			420	-	-
	Clock to Carry Out			480	-	-
	Carry In to Carry Out			250	-	-
	Preset or Reset to Carry Out			640	-	-

TYPE	(NOTE 1) CONDITIONS V_{DD}= 5V, C_L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4511B	Data to Output	1040 (Note 2)	310 (Note 2)	-
	-	1320 (Note 1)	80 (Note 1)	-
CD4512B	Inhibit to Output	280	200	-
	"A" Select to Output	400	-	-
	Data to Output	360	-	-
	t_{PHZ}, t_{PZH}	120	-	-
CD4514B, CD4515B	Strobe or Data	970	200	-
	Inhibit	500	-	-
CD4516B	Clock to Q Output	400	200	2
	Preset or Reset to Q	420	-	-
	Clock to Carry Out	480	-	-
	Carry In to Carry Out	250	-	-
	Preset or Reset to Carry Out	640	-	-
CD4517B	Clock to Q16	400	200	3
CD4518B, CD4520B	Clock to Output	560	200	1.5
	Reset to Output	650 (Note 2)	-	-
CD4527B	Clock to Out	300	200	1.2
	Clear to Out	760	-	-
	Cascade to Out	180	-	-
CD4532B	E_I to E_O, E_I to Gs	220	200	-
	Dn to Qm	440	-	-
	Dn to Gs, E_I to Qm	340	-	-
CD4536B	Clock to Q1 8 Bypass High	2000	200	0.5
	Clock to Q1 8 Bypass Low	5000	-	-
	Clock to Q16	8000	-	-
	Reset to Qn	6000 (Note 2)	-	-

Switching Characteristics at +25°C (Continued)

TYPE	(NOTE 1) CONDITIONS V_{DD}= 5V, C_L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD4541B	Clock to Q(2^8)	10500	200 (Note 2)	0.75
	Clock to Q(2^{16})	18000	360 (Note 1)	-
CD4555B, CD4556B	Select to Any Output	440	200	-
	$\overline{\text{Enable}}$ to Any Output	400	-	-
CD4585B	Comparator Inputs to Outputs	600	200	-
	Cascade Inputs to Outputs	400	-	-
CD4724B	Data to Outputs	400	200	-
	Write Disable to Output	400	-	-
	Reset to Output	350 (Note 2)	-	-
	Address to Output	450	-	-
CD14538B	Trigger to Q, $\overline{Q}$	600	200	-
	Reset to Q or $\overline{Q}$	500	-	-
CD40100B	-	720	200	1
CD40101B	Data In to Output	700	200	-
	Inhibit In to Output	280	-	-
CD40102B, CD40103B	Clock to Output	600	200	0.7
	Carry In/Counter Enable to Output	400	-	-
	Asynchronous Preset Enable to Output	1300 (Note 1)	-	-
	$\overline{\text{Clear}}$ to Output	750 (Note 2)	-	-
CD40104B	Clock to Q	440	200	3
	t_{PZH}, t_{PLZ}, t_{PZL}	160	-	-
	t_{PHZ}	90	-	-
CD40105B	Shift Out or Reset to Data Out Ready	370 (Note 2)	200	1.5
	Shift In to Data In Ready	320 (Note 2)	-	-
	Three-State Control to Data Out t_{PZH}	280	-	-
CD40105B (Continued)	Ripple Thru Delay Input to Out t_{PLH}	4000 (Note 1)	-	-
CD40106B	-	280	200	-
CD40107B	R_L = 120Ω	200	100	-
CD40108B	Clock or Write Enable to Q	720	200	1.5
	Read or Write Address to Q	600	-	-
	Disable Delay Time, t_{PZH}, t_{PHZ}	200	-	-
	Disable Delay Time, t_{PZL}, t_{PLZ}	260	-	-
CD40109B	DATA INPUT TO OUTPUT			

SHIFT MODE	V_{CC}	V_{DD}			
L-H	5V	10V	600 (Note 2)	100	-
L-H	5V	10V	260 (Note 1)	-	-
H-L	10V	5V	500 (Note 2)	200	-
H-L	10V	5V	460 (Note 1)	-	-

THREE-STATE DISABLE DELAY R_L = 1kΩ

	SHIFT MODE	V_{CC}	V_{DD}			
t_{PHZ}	L-H	5V	10V	120	-	-
t_{PHZ}	H-L	10V	5V	400	-	-
t_{PLZ}	L-H	5V	10V	740	-	-
t_{PLZ}	H-L	10V	5V	500	-	-
t_{PZH}	L-H	5V	10V	640	-	-
t_{PZH}	H-L	10V	5V	600	-	-
t_{PZL}	L-H	5V	10V	200	-	-
t_{PZL}	H-L	10V	5V	400	-	-

Switching Characteristics at +25°C (Continued)

TYPE	(NOTE 1) CONDITIONS V_{DD}= 5V, C_L = 50pF	PROP DELAY (ns)	TRANS TIME (ns)	MAX CLK INPUT FREQ (MHz)
CD40116	Data In to Data Out, CMOS In, TTL Out	35	40	-
	Data In to Data Out, TTL In, CMOS Out	45	-	-
	Disable to TTL Out, t_{PHZ}, t_{PLZ}	45	-	-
	Disable to TTL Out, t_{PZH}, t_{PZL}	50	-	-
	Enable to CMOS Out, t_{PHZ}, t_{PLZ}	30	-	-
	Enable to CMOS Out, t_{PZH}, t_{PZL}	60	-	-
CD40160B, CD40161B, CD40163B	Clock to Q	400	200	2
	Clock to C_{OUT}	450	-	-
	T_E to C_{OUT}	250	-	-
	Clear to Q (CD40160B and CD40161B Only)	500 (Note 2)	-	-
CD40174B	Clock to Output	300	200	3.5
	Clear to Output	200 (Note 2)	-	-
CD40192B, CD40193B	Clock Up or Clock Down to Q, Reset Q	500	200	2
	PE to Q	400	-	-
	Clock Up to Carry, Clock Down to Borrow	320	-	-
	Reset or PE to Borrow or Carry	600	-	-
CD40194B	Clock to Q	440	200	3
	Reset to Q	460 (Note 2)	-	-
CD40257B	Data Input to Output	300	200	-
	Select to Output	380	-	-
	Output Disable to Output	-	-	-
	t_{PZH}, t_{PHZ}	190	-	-
	t_{PZL}, t_{PLZ}	190	-	-

NOTES:

1. t_{TLH} or t_{PLH}
2. t_{THL} or t_{PHL}

Gate Count

TYPE NUMBER	GATE COUNT
CD4000B	12
CD4000UB	4
CD4001B	10
CD4001UB	4
CD4002B	9
CD4002UB	4
CD4006B	83
CD4007UB	2
CD4008B	34
CD4009UB	8
CD4010B	8
CD4011B	10
CD4011UB	4
CD4012B	9
CD4013B	20
CD4014B	57
CD4015B	54
CD4016B	6
CD4017B	50
CD4018B	40
CD4019B	10
CD4020B	85
CD4021B	57
CD4022B	40
CD4023B	11
CD4023UB	5
CD4024B	45
CD4025B	11
CD4025UB	5
CD4027B	25
CD4028B	26
CD4029B	64
CD4030B	11
CD4031B	271
CD4033B	72
CD4034B	106
CD4035B	45
CD4040B	75
CD4041UB	8
CD4042B	16
CD4043B	23

TYPE NUMBER	GATE COUNT
CD4044B	23
CD4046B	35
CD4047B	46
CD4048B	28
CD4049UB	3
CD4050B	6
CD4051B	58
CD4052B	40
CD4053B	46
CD4054B	28
CD4056B	70
CD4060B	83
CD4063B	56
CD4066B	9
CD4067B	75
CD4068B	11
CD4069UB	3
CD4070B	11
CD4071B	12
CD4072B	11
CD4073B	12
CD4075B	12
CD4076B	54
CD4077B	11
CD4078B	11
CD4081B	12
CD4082B	11
CD4085B	10
CD4086B	9
CD4089B	67
CD4093B	14
CD4094B	88
CD4095B	19
CD4096B	19
CD4097B	74
CD4098B	37
CD4099B	62
CD4502B	26
CD4503B	17
CD4504B	20
CD4508B	48

TYPE NUMBER	GATE COUNT
CD4510B	65
CD4511B	55
CD4512B	20
CD4514B	59
CD4515B	67
CD4516B	58
CD4517B	280
CD4518B	72
CD4520B	71
CD4527B	63
CD4532B	28
CD4536B	195
CD4541B	119
CD4555B	21
CD4556B	25
CD4585B	40
CD4724B	62
CD14538B	58
CD40100B	173
CD40101B	27
CD40102B	141
CD40103B	139
CD40104B	52
CD40105B	242
CD40106B	18
CD40107B	4
CD40108B	137
CD40109B	72
CD40116	76
CD40160B	66
CD40161B	66
CD40163B	66
CD40174B	37
CD40175B	28
CD40192B	80
CD40193B	87
CD40194B	52
CD40257B	35

NOTE:

1. Gate Count is based on four transistors per gate rounded off to nearest nondecimal integer.

Static Life Test and Burn-In Test Circuit Connections (Note 1 and Note 2)

TYPE	STATIC BURN-IN		
	OPEN	GND	V_{DD}
CD4000	1, 2, 6, 9, 10	7	3-5, 8, 11-14
CD4001	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14
CD4002	1, 6, 8, 13	7	2-5, 9-12, 14
CD4006	2, 8-13	7	1, 3-6, 14
CD4007	1, 5, 8, 12, 13	4, 7, 9	2, 3, 6, 10, 11, 14
CD4008	10-14	8	1-7, 9, 15, 16
CD4009 (Note 3)	2, 4, 6, 10, 12, 13, 15	8	1 (Note 4), 3, 5, 7, 9, 11, 14, 16 (Note 4)
CD4010 (Note 3)	2, 4, 6, 10, 12, 13, 15	8	1 (Note 4), 3, 5, 7, 9, 11, 14, 16 (Note 4)
CD4011	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14
CD4012	1, 6, 8, 13	7	2-5, 9-12, 14
CD4013	1, 2, 12, 13	7	3-6, 8-11, 14
CD4014	2, 3, 12	8	1, 4-7, 9-11, 13-16
CD4015	2-5, 10-13	8	1, 6, 7, 9, 14-16
CD4016	2, 3, 9, 10	7	1, 4-6, 8, 11-14
CD4017	1-7, 9-12	8, 14	13, 15, 16
CD4018	4-6, 11, 13	8	1-3, 7, 9, 10, 12, 14-16
CD4019	10-13	8	1-7, 9, 14-16
CD4020	1-7, 9, 12-15	8	10, 11, 16
CD4021	2, 3, 12	8	1, 4-7, 9-11, 13-16
CD4022	1-7, 9-12	8, 14	13, 15, 16
CD4023	6, 9, 10	7	1-5, 8, 11-14
CD4024	3-6, 8-13	7	1, 2, 14
CD4025	6, 9, 10	7	1-5, 8, 11-14
CD4027	1, 2, 14, 15	8	3-7, 9-13, 16
CD4028	1-7, 9, 14, 15	8	10-13, 16
CD4029	2, 6, 7, 11, 14	8	1, 3-5, 9, 10, 12, 13, 15, 16
CD4030	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14
CD4031	3-7, 9, 11-14	8	1, 2, 10, 15, 16
CD4033	4-7, 9-13	8	1-3, 14-16
CD4034	1-8	12	9-11, 13-24
CD4035	1, 13-15	8	2-7, 9-12, 16
CD4040	1-7, 9, 12-15	8	10, 11, 16

TYPE	STATIC BURN-IN		
	OPEN	GND	V_{DD}
CD4041	1, 2, 4, 5, 8, 9, 11, 12	7	3, 6, 10, 13, 14
CD4042	1-3, 9-12, 15	8	4-7, 13, 14, 16
CD4043	1, 2, 9, 10, 13	8	3-7, 11, 12, 14-16
CD4044	1, 2, 9, 10, 13	8	3-7, 11, 12, 14-16
CD4046	1, 2, 4, 6, 7, 10, 11, 13, 15	8	3, 5, 9, 12, 14, 16
CD4047	1, 2, 10, 11, 13	7	3-6, 8, 9, 12, 14
CD4048	1	8	2-7, 9-16
CD4049 (Note 3)	2-4, 6, 10, 12, 13, 15	8	1 (Note 4), 3, 5, 7, 9, 11, 14, 16 (Note 4)
CD4050 (Note 3)	2, 4, 6, 10, 12, 13, 15	8	1 (Note 4), 3, 5, 7, 9, 11, 14, 16 (Note 4)
CD4051 (Note 3)	3	7 (Note 4), 8 (Note 4)	1, 2, 4-6, 9-16
CD4052 (Note 3)	3, 13	7 (Note 4), 8 (Note 4)	1, 2, 4-6, 9-12, 14-16
CD4053 (Note 3)	4, 14, 15	7 (Note 4), 8 (Note 4)	1-3, 5, 6, 9-13, 16
CD4054 (Note 3)	3-6	7 (Note 4), 8	1, 2, 9-16
CD4056 (Note 3)	9-15	7 (Note 4), 8	1-6, 16
CD4060	1-7, 9, 10, 13-15	8	11, 12, 16
CD4063	5-7	3, 8	1, 2, 4, 9-16
CD4066	2, 3, 9, 10	7	1, 4-6, 8, 11-14
CD4067	1	12	2-11, 13-23
CD4068	1, 6, 8, 13	7	2-5, 9-12, 14
CD4069	2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14
CD4070	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14
CD4071	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14
CD4072	1, 6, 8, 13	7	2-5, 9-12, 14
CD4073	6, 9, 10	7	1-5, 8, 11-14
CD4075	6, 9, 10	7	1-5, 8, 11-14
CD4076	3-6	8	1, 2, 7, 9-16
CD4077	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14
CD4078	1, 6, 8, 13	7	2-5, 9-12, 14

Static Life Test and Burn-In Test Circuit Connections (Continued)

TYPE	STATIC BURN-IN		
	OPEN	GND	V_{DD}
CD4081	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14
CD4082	1, 6, 8, 13	7	2-5, 9-12, 14
CD4085	3, 4	7	1, 2, 5, 6, 8-14
CD4086	3, 4	7	1, 2, 5, 6, 8-14
CD4089	1, 5-7	8	2-4, 9-16
CD4093	3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12-14
CD4094	4-7, 9-14	8	1-3, 15, 16
CD4095	1, 6, 8	7	2-5, 9-14
CD4096	1, 6, 8	7	2-5, 9-14
CD4097	1, 17	12	2-11, 13-24
CD4098	2, 6, 7, 9, 10, 14	1, 8, 15	3-5, 11-13, 16
CD4099	1, 9-15	8	2-7, 16
CD4502	2, 5, 7, 9, 11, 14	8	1, 3, 4, 6, 10, 12, 13, 15, 16
CD4503	3, 5, 7, 9, 11, 13	8	1, 2, 4, 6, 10, 12, 14-16
CD4504	2, 4, 6, 10, 12, 15	8	16, (1 [Note 4], 3, 5, 7, 9, 11, 13, 14), Note 5
CD4508	5, 7, 9, 11, 17, 19, 21, 23	12	1-4, 6, 8, 10, 13-16, 18, 20, 22, 24
CD4510	2, 6, 7, 11, 14	8	1, 3-5, 9, 10, 12, 13, 15, 16
CD4511	9-15	8	1-7, 16
CD4512	14	8	1-7, 9-13, 15, 16
CD4514	4-11, 13-20	12	1-3, 21-24
CD4515	4-11, 13-20	12	1-3, 21-24
CD4516	2, 6, 7, 11, 14	8	1, 3-5, 9, 10, 12, 13, 15, 16
CD4517	1, 2, 5, 6, 10, 11, 14, 15	8	3, 4, 7, 9, 12, 13, 16
CD4518	3-6, 11-14	8	1, 2, 7, 9, 10, 15, 16
CD4520	3-6, 11-14	8	1, 2, 7, 9, 10, 15, 16
CD4527	1, 5-7	8	2-4, 9-16
CD4532	6, 7, 9, 14, 15	8	1-5, 10-13, 16
CD4536	4, 5, 13	8	1-3, 6, 7, 9-12, 14-16
CD4541	1, 2, 4, 8, 11	7	3, 5, 6, 9, 10, 12-14
CD4555	4-7, 9-12	8	1-3, 13-16
CD4556	4-7, 9-12	8	1-3, 13-16

TYPE	STATIC BURN-IN		
	OPEN	GND	V_{DD}
CD4585	3, 12, 13	8	1, 2, 4-7, 9-11, 14-16
CD4724	4-7, 9-12	8	1, 3, 13-16
CD14538	2, 6, 7, 9, 10, 14	1, 8, 15	3-5, 11-13, 16
CD40100	1, 4, 5, 7, 10, 12, 14, 15	8	2, 3, 6, 9, 11, 13, 16
CD40101	6, 9	7	1-5, 8, 10-14
CD40102	14	8	1-7, 9-13, 15, 16
CD40103	14	8	1-7, 9-13, 15, 16
CD40104	12-15	8	1-7, 9-11, 16
CD40105	2, 10-14	8	1, 3-7, 9, 15, 16
CD40106	2, 4, 6, 8, 10, 12	7	1, 3, 5, 9, 11, 13, 14
CD40107	1, 2, 5, 6, 8, 9, 12, 13	7	3, 4, 10, 11, 14
CD40108	1, 2, 4-7, 22, 23	12	3, 8-11, 13-21, 24
CD40109 (Note 3)	4, 5, 11-13	8	16, (1 [Note 4], 2, 3, 6, 7, 9, 10, 14, 15), Note 5
CD40116 (Note 3)	2-9	11, 12	1 (Note 4) 10 = V_{DD} (Note 6) 13-22 (Note 4) = V_{CC}
CD40160	11-15	8	1-7, 9, 10, 16
CD40161	11-15	8	1-7, 9, 10, 16
CD40163	11-15	8	1-7, 9, 10, 16
CD40174	2, 5, 7, 10, 12, 15	8	1, 3, 4, 6, 9, 11, 13, 14, 16
CD40175	2, 3, 6, 7, 10, 11, 14, 15	8	1, 4, 5, 9, 12, 13, 16
CD40193	2, 3, 6, 7, 12, 13	8	1, 4, 5, 9-11, 14-16
CD40194	12-15	8	1-7, 9-11, 16
CD40257	4, 7, 9, 12	8, 15	1-3, 5, 6, 10, 11, 13, 14, 16

NOTES:

1. For Type A devices, use V_{DD} = 12.5V. For Type B and UB devices, use V_{DD} = 18V.
2. Each pin except V_{DD} and V_{SS} must have resistors of 2kΩ to 47kΩ. In most cases, V_{SS} is at pin 7 (of a 14 pin IC), pin 8 (of a 16 pin IC) or pin 12 (of a 24 pin IC), while V_{DD} is at the highest numbered pin; exceptions are noted.
3. Non-standard pin arrangement, or multiple supply pins.
4. Connect pin(s) without using resistor.
5. Pin voltage is $V_{DD}/2$ for pins inside parentheses.
6. V_{DD} = 11.5V; V_{CC} = 6.5V; use 300Ω resistors at pins 10, 13-21.

MIL-STD-883, Notice 5

GROUP A ELECTRICAL TESTS FOR CLASS B (JAN) DEVICES (NOTE 1)

SUBGROUPS (NOTE 2) **QUALITY/ACCEPT NO. = 116/0** (NOTES 3, 4 AND 5)
Subgroup 1 DC Test at +25°C
Subgroup 2 DC Tests at Maximum Rated Operating Temperature
Subgroup 3 DC Tests at Minimum Rated Operating Temperature
Subgroup 4 AC Tests at +25°C
Subgroup 5 AC Tests at Maximum Rated Operating Temperature
Subgroup 6 AC Tests at Minimum Rated Operating Temperature
Subgroup 7 Functional Tests at +25°C
Subgroup 8A Functional Tests at Maximum Rated Operating Temperature
Subgroup 8B Functional Tests at Minimum Rated Operating Temperature
Subgroup 9 Switching Tests at +25°C
Subgroup 10 Switching Tests at Maximum Rated Operating Temperature
Subgroup 11 Switching Tests at Minimum Rated Operating Temperature

NOTES: (Group A)

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.
2. At the manufacturer's option, the applicable test required for group A testing (see Note 1) may be conducted individually or combined into sets of tests, subgroups (as defined in the Group A Electrical Tests Table), or sets of subgroups. However, the manufacturer shall predesignate these groupings prior to grouping a testing. Unless otherwise specified, the individual tests, subgroups, or sets of test/subgroups may be performed in any sequence.
3. The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in Note 2 above, shall be 116/0.
4. A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.
5. If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test setup for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/ subgroups. as applicable. For class S only, if this testing results in a percent defective greater than 5%, the (sub)lot shall be rejected, except that for (sub)lot previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of test/subgroups, as applicable, using a 116/0 sample.

Electrical Test Requirements for Non-JAN Lot Conformance Tests

GROUP A ELECTRICAL TESTS FOR HARRIS 3, 3A AND SMD PRODUCT

SUB GROUPS	WHERE USED
Subgroup 1 DC Tests at +25°C	All Types When Required
Subgroup 2 DC Tests at Maximum Rated Operating Temperature	All Types When Required
Subgroup 3 DC Tests at Minimum Rated Operating Temperature	All Types When Required
Subgroup 7 Functional Tests at +25°C	All Types When Required
Subgroup 8A Functional Tests at Maximum Rated Operating Temperatures	All Types When Required
Subgroup 8B Functional Test at Minimum Rated Operating Temperatures	All Types When Required
Subgroup 9 Switching Tests at +25°C	Digital Types When Required

CD4000 3, 3A AND SMD

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (PER METHOD 5005, GROUP A ELECTRICAL TESTS TABLE)
Group A Test Requirements (Method 5005)	1, 2, 3, 7, 8, 9
Groups B and C End-Point Electrical Parameter (Method 5005) (Class S and B)	1, 2, 3, 7, 8
Groups D End-Point Electrical Parameters (Method 5005)	1, 2, 3

Life Test Reliability Data

Reliability can be defined as "the probability of a device performing a function, under specific conditions for which designed, for a specific period of time." But because of the higher reliability levels required in today's integrated circuits, the extended time and high cost required to measure their reliability at application stress levels become prohibitive.

A practical method of meeting these concerns is through the use of accelerated life testing, a method by which devices are operated at, or subjected to, higher stress levels than they normally experience in a typical application.

Life tests are generally performed at elevated temperatures and maximum recommended operating voltage in order to accelerate time-dependent failure mechanisms related to conditions of temperature and electrical stress. Life testing is the principal method used in predicting the failure rates of components in actual field applications.

Activation Energy

The activation energy is defined as the minimum kinetic energy a molecule or atom in the initial state of a process must acquire before it can take part in a reaction. Failure mechanisms can differ markedly in terms of their reaction rates. A low activation energy implies that the reaction rate (failure rate) will not be accelerated as much by temperature as will a reaction with a high activation energy.

The acceleration factor used in predicting the failure rate from the life test condition depends directly on the activation energy.

The activation energy estimates reported in the semiconductor industry, as obtained from integrated circuit life test evaluations, fall in the range of approximately 0.3eV to 1.4eV. However, a value of 1.0eV has been shown to be fairly representative. This value has been demonstrated on Harris Logic CMOS integrated circuits using relatively large sample quantities and is the value used in Calculating Life Test Temperature Acceleration Factors.

Temperature Acceleration Factor

A variety of failure mechanisms can be accelerated by life testing. The reaction rates of most of these mechanisms are highly dependent of temperature and are best expressed by the Arrhenius model:

$R(T) = A \exp(-E/kT)$

where,

$R(T)$ = Reaction Rate

A = Constant

k = Boltzmann's Constant (8.63 x 10-5eV/°K)

E = Activation Energy (eV)

T = Absolute Temperature (°C +273)

For electronic components, the reaction rate refers to the failure rate. The acceleration factor, which relates the test failure rate to the end-use failure rate, can be determined from the Arrhenius equation for any activation energy, as follows:

$$F_A = \exp\left[\frac{E}{k}\left(\frac{1}{T_{USE}} - \frac{1}{T_{TEST}}\right)\right]$$

Reliability Data

PRODUCT CLASSIFICATION	QUANTITY TESTED	ACTUAL DEVICE HRS	TEST TEMP.	TEST VOLTS	NO. REJECTS	EQUIV. DEVICE HRS AT +55°C	FAILURE RATE AT 60% U.C.L.	
							%/1000 HRS AT +55°C	FITS AT +55°C
CD4000B-JAN B	4326	2,180,304	135	18	12	2.2×10^9	6.1×10^{-4}	6.1
CD4000A-JAN B	4209	2,121,336	135	12.5	14	2.2×10^9	7.2×10^{-4}	7.2
CD4000B 3A	539	539,000	125	18	0	1.1×10^9	3.6×10^{-4}	3.6
	722	861,000	135	18	3	1.1×10^9	3.6×10^{-4}	3.6
CD4000B 3	4280	4,280,000	125	18	0	5.7×10^9	1.1×10^{-4}	1.1
	7060	3,530,000	135	18	5	5.7×10^9	1.1×10^{-4}	1.1
CD4000A 3	2387	2,387,000	125	12.5	0	4.2×10^9	0.73×10^{-4}	0.7
	5920	2,960,000	135	12.5	2	4.2×10^9	0.73×10^{-4}	0.7