P54/74FCT273/A/C (P54/74PCT273/A/C)
OCTAL D FLIP-FLOP

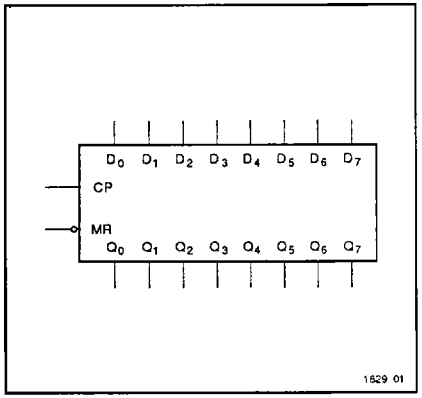
FEATURES

- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-C speed at 5.8ns max. (Com'l)
  FCT-A speed at 7.2ns max. (Com'l)
- CMOS V_{OH} Levels for Low Power Consumption
  — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'l), 48 mA (Mil)
  15 mA Source Current (Com'l), 12 mA (Mil)
- Edge Triggered D Flip-Flops
- 250MHz Typical Toggle Rate
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- Input Clamp Diode to Limit Bus Reflections
- Manufactured in 0.8 micron PACE Technology™

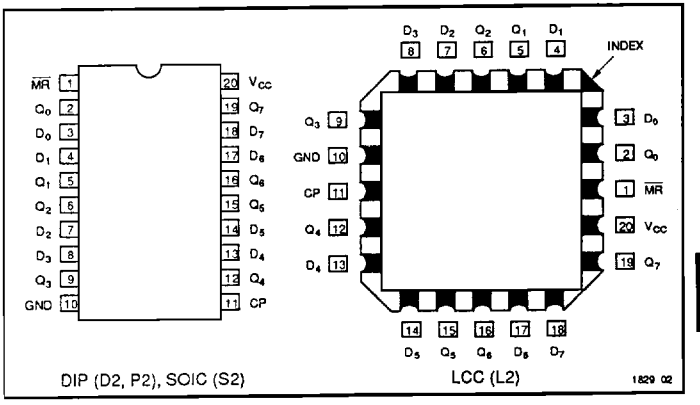
DESCRIPTION

The 'FCT273 consists of eight edge triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset ($\overline{MR}$) load and reset (clear) all flip-flops simultaneously. The 'FCT273 is an edge triggered register. The state of each D input (one setup time before the low-to-high clock transition) is transferred to the corresponding flip-flop's Q output. All outputs will be forced low by a low voltage level on the $\overline{MR}$ input.

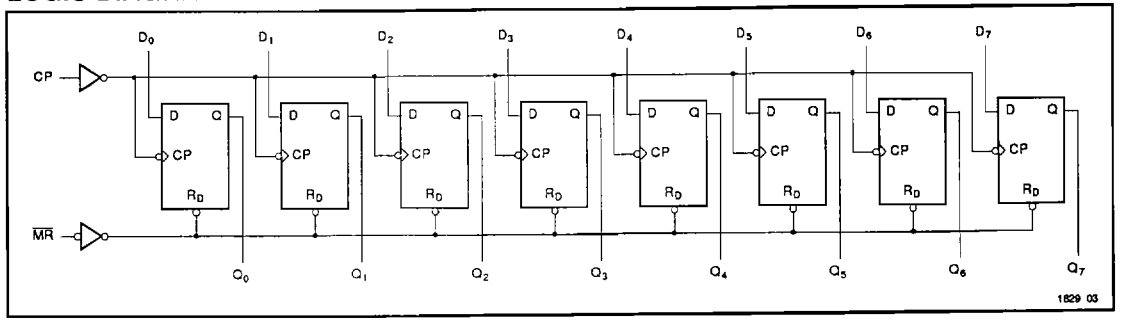
LOGIC SYMBOL



PIN CONFIGURATIONS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

1829 Tbl 01 1829 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1829 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1829 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{CD}	Input clamp diode voltage				–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH voltage	Military Commercial	2.4	3.3		V	MIN	I_{OH} = –12mA I_{OH} = –15mA
V_{OL}	Output LOW voltage	Military (TTL) Commercial (TTL)			0.5 0.5	V V	MIN MIN	I_{OL} = 32mA I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output short circuit[2]		–60			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input capacitance[3]			5	10	pF		All inputs
C_{OUT}	Output capacitance[3]			9	12	pF		All outputs

1829 Tbl 05

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs) Com'l Mil	0.003 0.003	0.3 0.5	mA mA	V_{CC} = MAX, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, f = 0, Outputs Open
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, $\overline{MR} = V_{CC}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, Outputs Open
I_C	Total Power Supply Current[5]		4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{MR} = V_{CC}$ and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{MR} = V_{CC}$ and V_{IN} = 3.4V or V_{IN} = GND
			7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{MR} = V_{CC}$ and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			16.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{MR} = V_{CC}$ and V_{IN} = 3.4V or V_{IN} = GND

1829 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs			Output
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load '1'	H	⌐	h	H
Load '0'	H	⌐	l	L

1829 Tbl 07

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH transistion
X = Don't Care
⌐ = LOW-to-HIGH clock transition

9

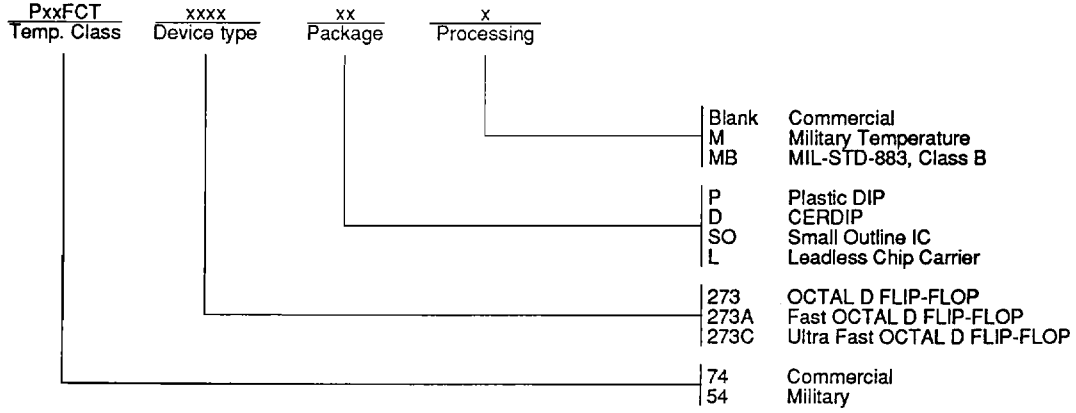
AC CHARACTERISTICS

Symbol	Parameter	'FCT273				'FCT273A				'FCT273C				Units	Fig. No.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	10.0	2.0	9.0	2.0	8.3	2.0	7.2	2.0	6.5	2.0	5.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output	2.0	12.5	2.0	11.0	2.0	8.3	2.0	7.2	2.0	6.8	2.0	6.1	ns	1, 6
$t_s(H)$ $t_s(L)$	Set-up Time HIGH or LOW D_n to CP	3.0	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW D_n to CP	1.0	—	1.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
$t_w(H)$ $t_w(L)$	Clock Pulse Width[2] HIGH or LOW	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns	5
$t_w(H)$ $t_w(L)$	$\overline{MR}$ Pulse Width LOW	6.0	—	6.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns	6
t_{rec}	Recovery Time $\overline{MR}$ to Clock	3.0	—	3.0	—	2.5	—	2.0	—	2.5	—	2.0	—	ns	6

1829 Tbl 08

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

ORDERING INFORMATION



1829 04