

Single-chip Type with Built-in FET type Switching Regulators

Flexible Step-down Switching Regulator with Built-in Power MOSFET



BD8643FV

No.10027EAT43

●Description

The BD8643FV is a synchronous step-down switching regulator that integrates 2 low resistances N-channel MOSFETs. It achieves 3A continuous output current over a wide input supply range. Current mode operation provides fast transient response and easy phase compensation.

●Feature

- 1) Synchronous rectification with built-in FET type DC/DC converter
- 2) 2.0A output current
- 3) Range of operation power-supply voltage 4.5V~18V
- 4) Reference voltage FB 0.8V±1%
- 5) Programmable frequency 100kHz~600kHz
- 6) Over current protection function
- 7) Thermal shutdown function
- 8) Under voltage protection
- 9) Soft start time out function / Soft start delay circuit
- 10) Programmable OFFLATCH time

●Applications

FPD,DVD,HDD Recorder,STB,Amusement,Other

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Input supply voltage	V _{IN}	20	V
BOOT terminal voltage	V _{BOOT}	28	V
EN terminal voltage	V _{EN}	GND-0.3 ~ V _{IN} +0.3	V
Input terminal voltage	V _{INP} ^{*1}	GND-0.3 ~ 7	V
SW terminal voltage	V _{SW}	GND-0.3 ~ V _{IN} +0.3	V
Output current	I _{OUT}	3.5	A
Power dissipation	P _d	1.19 ^{*2}	W
Operating temperature	T _{opr}	-20 ~ 85	°C
Storage temperature	T _{stg}	-55 ~ 150	°C

*1 VINP Application terminal: SS/DELAY, FB, FC, RT, PSET

*2 (70mm×70mm, thickness 1.6mm, and four layer glass epoxy substrates)When mounting substrate and the package back exposure part are connected with solder
Operating at higher than Ta=25°C, 9.5mW shall be reduced per 1

●Operating conditions

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Input supply voltage	V _{IN}	4.5	-	18.0	V
Output current	I _{OUT}	-	-	3.0	A

* This product is not designed for protection against radioactive rays.

●Electrical characteristic

(Unless otherwise noted $T_a=25^{\circ}\text{C}$, $V_{\text{IN}}=12\text{V}$, $V_{\text{EN}}=3\text{V}$)

Parameter	Symbol	Limits			UNIT	Condition
		Min.	Typ.	Max.		
V_{IN} supply current (operating)	$I_{\text{Q_active}}$	-	1.5	2.5	mA	$V_{\text{FB}} = 0.75\text{V}$
V_{IN} supply current (standby)	$I_{\text{Q_stby}}$	-	0.8	1.2	mA	$V_{\text{EN}} = 0\text{V}$
Reference voltage (V_{REF})	V_{FB}	0.792	0.800	0.808	V	FB-FC Short
Oscillation frequency	f_{OSC}	270	300	330	kHz	$R_{\text{RT}} = 56\text{k}\Omega$
High side FET ON resistance	R_{HFET}	-	120	170	m Ω	$I_{\text{SW}} = -1\text{A}$
Low side FET ON resistance	R_{LFET}	-	120	170	m Ω	$I_{\text{SW}} = 1\text{A}$
UVLO voltage	V_{UVLO}	3.8	4.0	4.2	V	V_{IN} Sweep
SW leak current	I_{LSW}	-	0	5	μA	$V_{\text{EN}} = 0\text{V}$
EN terminal H threshold voltage	V_{ENH}	1.6	-	-	V	
EN terminal L threshold voltage	V_{ENL}	-	-	0.4	V	
SS/DELAY terminal source current	I_{SSSO}	2.8	4.0	5.2	μA	$V_{\text{SS}} = 1\text{V}$
SS/DELAY – FB Offset voltage	V_{SSFBOST}	450	600	750	mV	$V_{\text{SS}} = 1\text{V}$
PSET terminal source current	I_{PSET}	3.0	5.0	7.0	μA	$V_{\text{PSET}} = 2\text{V}$
PSET terminal threshold voltage	V_{PSET}	0.8	1.0	1.2	V	

- V_{FB} :FB terminal voltage, V_{EN} :EN terminal voltage, V_{SS} :SS/DELAY terminal voltage, V_{PSET} :PSET terminal voltage, R_{RT} :RT resistor
- Current capability should not exceed Pd.

● Reference data

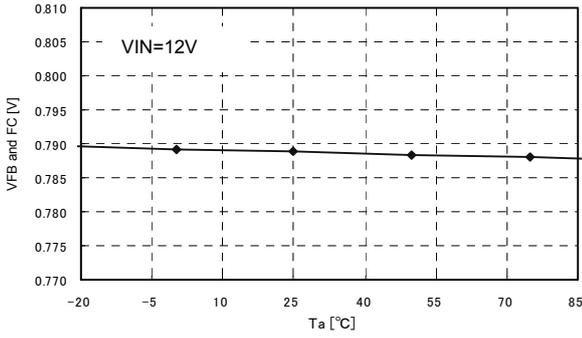


Fig.1 Reference voltage – temperature characteristic

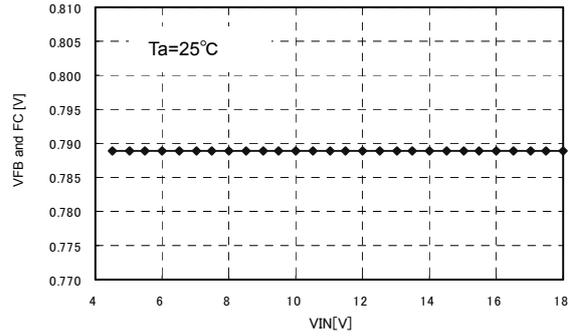


Fig.2 Reference voltage – VIN characteristic

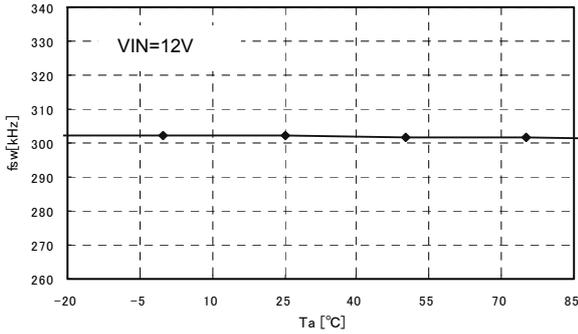


Fig.3 Frequency – temperature characteristic

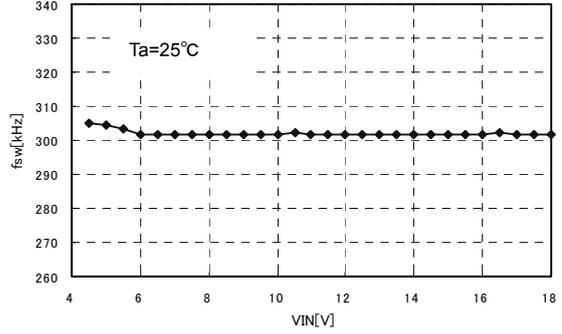


Fig.4 Frequency – VIN characteristic

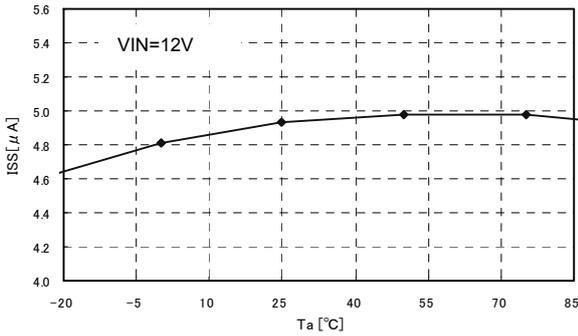


Fig.5 SS/DELAY charge current - temperature characteristic

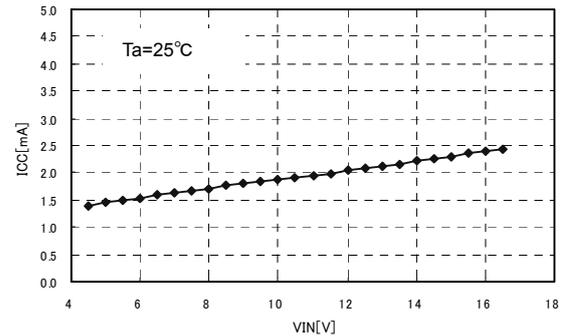


Fig.6 Circuit Current – VIN characteristic

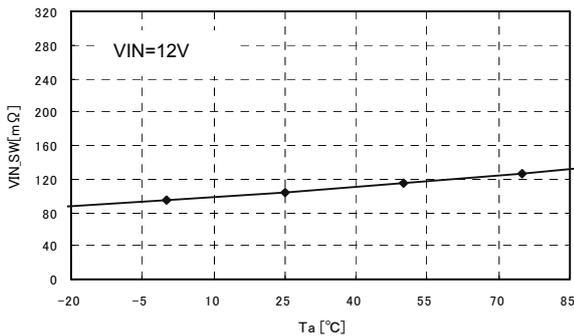


Fig.7 Hi side FET ON_R - temperature characteristic

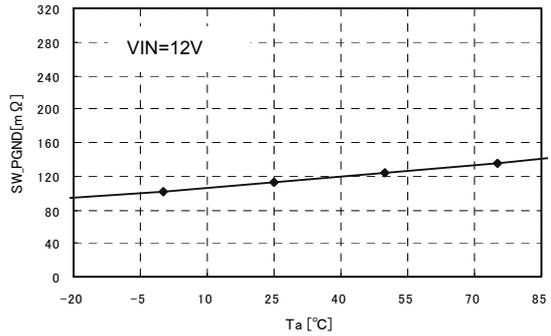


Fig.8 Low side FET ON_R - temperature characteristic

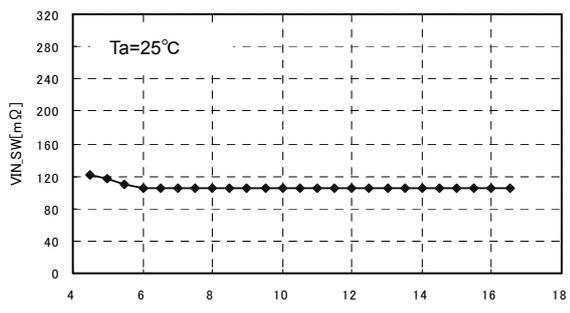


Fig.9 Hi side FET ON_R - VIN characteristic

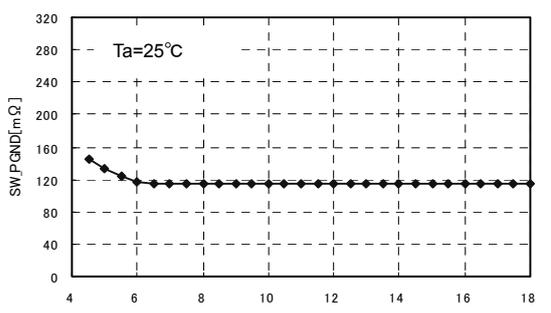


Fig.10 Low side FET ON_R – VIN characteristic

●Block Diagram

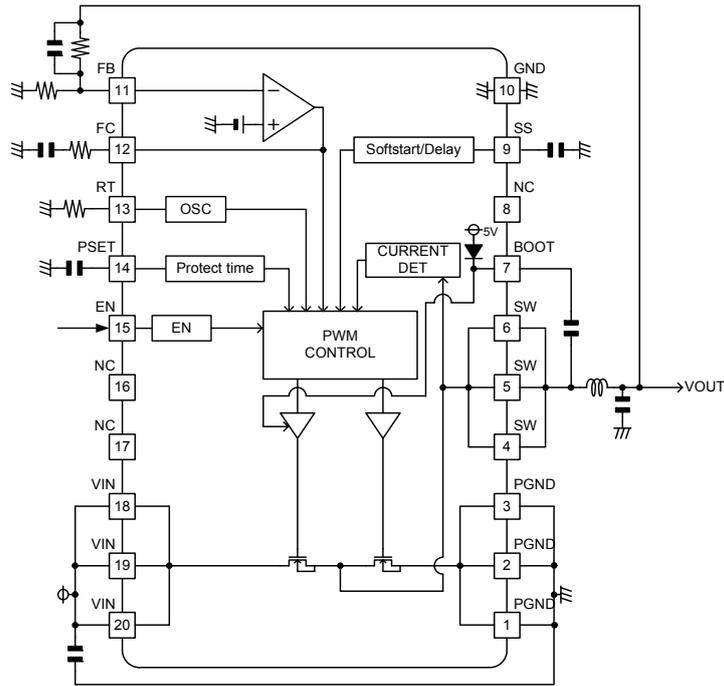
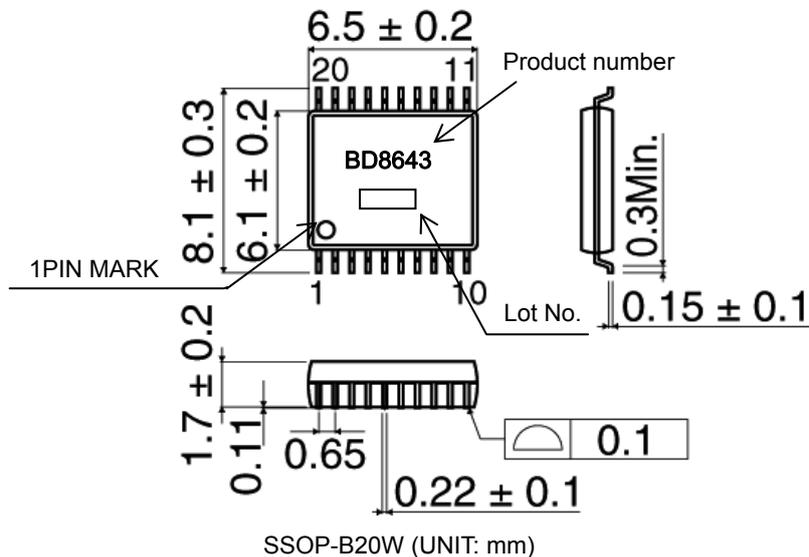


Fig.11 Block diagram

●terminal assignment

No.	Symbol	Description	No.	Symbol	Description
1	PGND	Power GND terminal	11	FB	Feedback terminal
2	PGND	Power GND terminal	12	FC	Phase amends terminal
3	PGND	Power GND terminal	13	RT	Frequency adjustment resistance connection terminal
4	SW	Switching output terminal	14	PSET	Adjust OFF LATCH time terminal
5	SW	Switching output terminal	15	EN	Enable input
6	SW	Switching output terminal	16	NC	-
7	BOOT	Boot strap terminal	17	NC	-
8	NC	-	18	VIN	Power supply input terminal
9	SS/DELAY	Soft start adjustment capacity connection terminal	19	VIN	Power supply input terminal
10	GND	Signal GND terminal	20	VIN	Power supply input terminal

●Package outline dimension



SSOP-B20W (UNIT: mm)

● Operation description

1 Enable control

The device can be controlled ON/OFF by EN terminal (15 pin) voltage.

An internal circuit starts when VEN reaches 1.4V.

When standing up of VIN is too steep (1msec or less), a defective start might be caused according to the state of Pascon between GND substrate pattern and power supply-when the terminal EN is short-circuited to the terminal VIN and it is used.

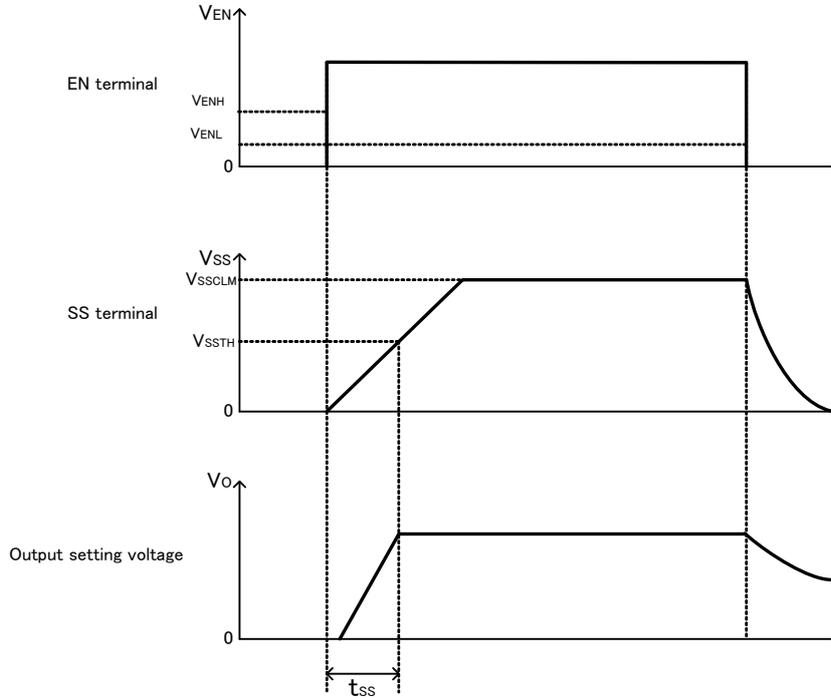


Fig.12 ON/OFF transition wave form in EN controlling

2 Soft start time set function

As for BD8643FV, output can do soft start without overshoot by charging soft start capacity (C_{SS}) connected between SS/DELAY (9 pin) and GND (10 pin) terminal.

Also, soft start time (t_{SS}) can be set by setting soft start capacity (C_{SS}) arbitrarily.(Refer to 5-2 soft start time setting method)

3 OSC oscillation frequency setting function

The output oscillation frequency can be set by connecting resistance between terminal RT (13 pin) and GND (range = 100kHz – 600kHz)

The relation between RT terminal resistance and the oscillation frequency follows Fig.13.

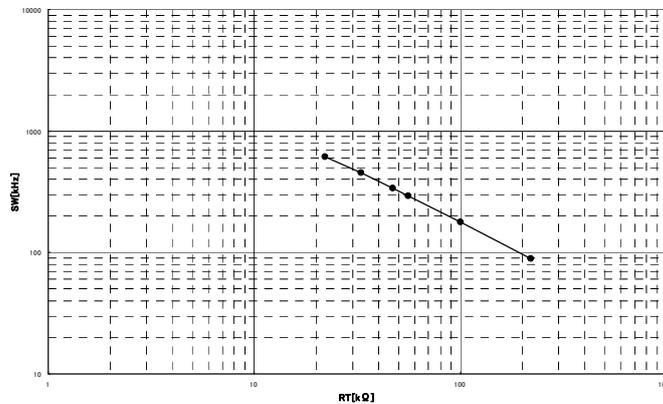


Fig.13 Oscillation frequency setting by RT resistance

●Protection function

Protection circuit is effective for destruction prevention due to accident so that avoid using under continuous protection operation.

1 Low voltage protection function (LVP)

The voltage of the terminal FB (11pin) is compared with internal reference voltage VREF.

If FB terminal voltage falls below $V_{LVP}(= VREF -120mV)$ and the state continues, output changes to low voltage and the state is fixed.

Table 1 output low voltage protection function

EN terminal	SS terminal	FB terminal	Low voltage Protection function	Low voltage Protection operation
$>V_{ENH}$	$>1.4V(typ)$	$<V_{LVP}$	Effective	ON
		$>V_{LVP}$		OFF
$<V_{ENL}$	$<1.4V(typ)$	-	Invalidity	OFF
	-	-	Invalidity	OFF

※ Low voltage protection function is available when SS terminal voltage becomes more than 1.4V (typ) in the transition to ON control (during soft start).

2 Over voltage protection function (OVP)

The voltage of the terminal FB is compared with internal reference voltage VREF.

If FB terminal voltage is over $V_{ovp}(=VREF +120mV)$ and the state is continues, output changes to low voltage and the state is fixed.

Table 2 output low voltage protection function

EN terminal	SS terminal	FB terminal	Low voltage Protection function	Low voltage Protection operation
$>V_{ENH}$	$>1.4V(typ)$	$>V_{OVP}$	Effective	ON
		$<V_{OVP}$		OFF
$<V_{ENL}$	$<1.4V(typ)$	-	Invalidity	OFF
	-	-	Invalidity	OFF

※ Over voltage protection function is available when SS terminal voltage becomes more than 1.4V (typ) in the transition to ON control (during soft start).

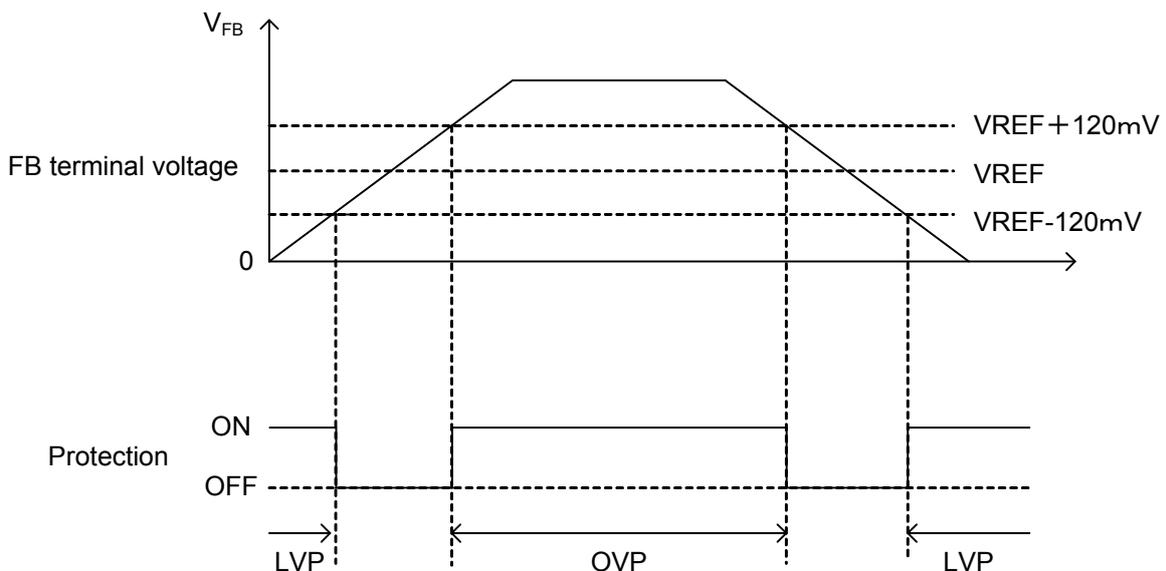


Fig.14 Output voltage error detection range

3 Under voltage lock out protection (UVLO)

As for BD8643FV, the power-supply voltage decrease detection protection circuit is built in. If the input voltage decrease below the UVLO voltage (4.0V typ), the device state changes to the standby mode (Moreover, to prevent the chattering of the output) hysteresis width of 300mV(typ) has been installed in the UVLO cancel voltage.

4 RT terminal open/short protection function (RTO/RTS)

RT terminal opening/short protection function prevent the clock from abnormal oscillation. If RT terminal open/short protection function is detected, output voltage changes to low level and is fixed.

5 Soft start time-out function

If VSS doesn't exceed VSSTH within 64msec (typ) since a soft start began, BD8643FV controls an off latch. Vo is fixed in a low level.

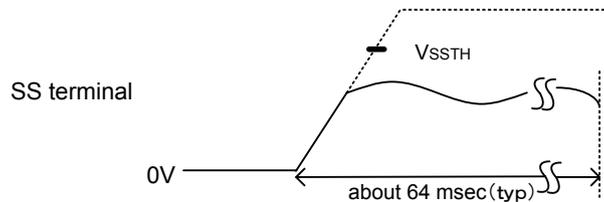


Fig.15 Soft start time-out

6 Thermal shut down function

Thermal shut down circuit (TSD circuit) is built into BD8643FV. When the temperature of the chip exceeds $T_{jmax}=175$, the DC/DC converter is fixed in a low voltage. TSD function is aimed to shut down IC from thermal reckless driving under an abnormal state to exceed $T_{jmax}=175$. It aims at neither protection nor the guarantee of the set. Therefore, please do not use this function to protect the set.

7 Over current protection function

The over current protection function has been achieved by limiting the current that flows on high side MOSFET. The current is controlled in every one cycle of the switching frequency. When an abnormal state continues, the output is fixed in a low level.

8 Error detection (off latch) release method

BD8643FV enters the state of an off latch when the protection function operates. To release the off latch state, VIN terminal voltage should be changed to less than UVLO level (=4.0V [typ]) once time.

●External parts setting method

1 Output voltage setting method

The output voltage can be arbitrarily set by external resistance.

$$V_o = \frac{(R1+R2)}{R2} V_{REF}$$

Please select the constant of R1 and R2 by this expression.

Please select the current that flows to R1 and R2 to become much smaller than output current.

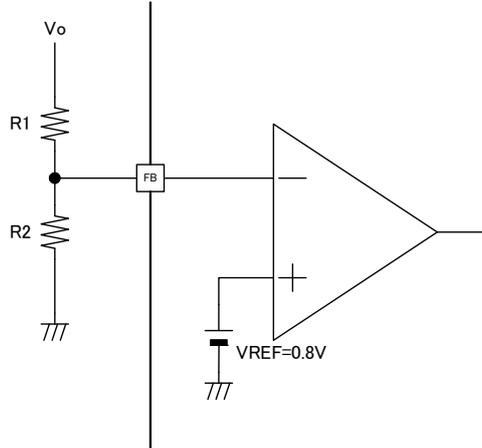


Fig.16 Output voltage setting circuit

2 Soft start time setting method

BD8643FV can soft start without overshoot because of a charge current to the soft start capacitance (CSS).

The soft start time can be set by connecting soft start capacity (CSS).

When the EN terminal voltage is set VIN_EN or more, the charge to the capacity between SS/DELAY and GND terminal is begun. The output voltage becomes soft start in proportion to a SS/DELAY terminal voltage rising. When the SS/DELAY terminal voltage exceeds VSSTH, the output voltage is fixed in a setting value.

Please set soft start time (tss) in 1msec-52.5msec.

$$T_{VO} = \underbrace{TW_{EN}(= 50\mu s)}_{\text{①}} + \underbrace{\frac{V_{OST}(= 0.6V) \times C_{SS}}{I_{SS}(= 4\mu A)}}_{\text{②}} + \underbrace{\frac{(V_{SSTH} - V_{OST}) \times C_{SS}}{I_{SS}(= 4\mu A)}}_{\text{③}}$$

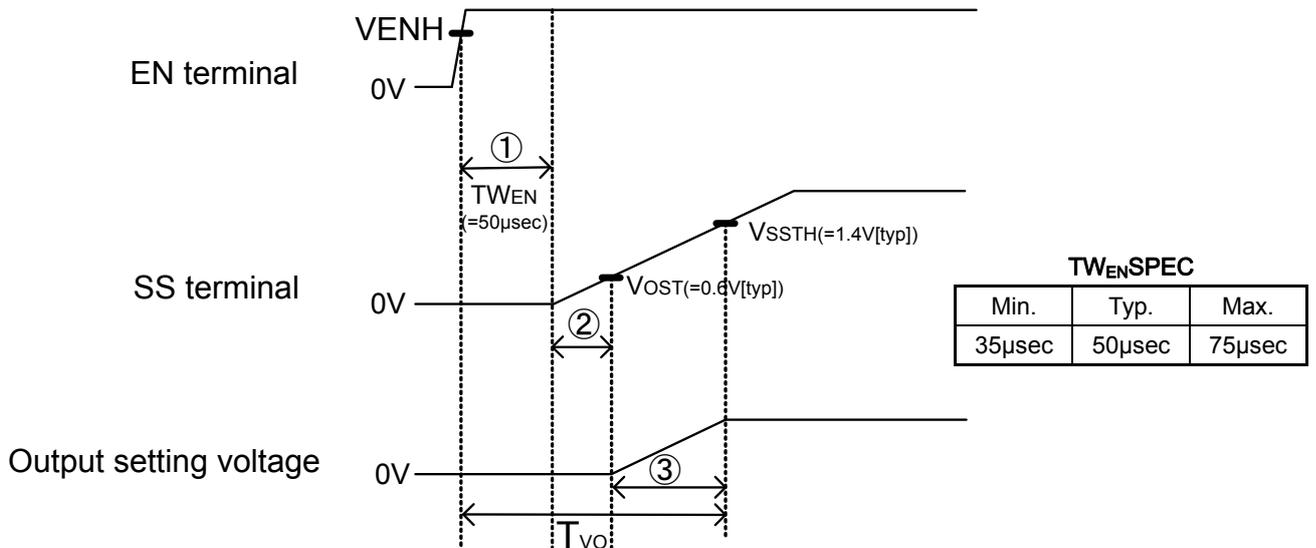


Fig.17 Soft start

3 Selection of inductor (L)

Please select the value of the inductor according to the following expressions.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f} \text{ [H]}$$

(ΔI_L : Output ripple current , f: Switching frequency)

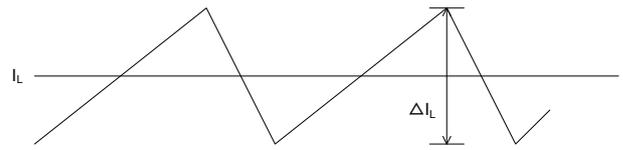


Fig.18 Current of output ripple

※Please have and select an enough margin so that the current peak should not exceed the ratings current value of the inductor.

4 Selection of input capacitor (Cin)

Please use a low ESR input capacitor which can be used with high voltage and ripple current to prevent a big transition voltage.

※Please put on the input capacitor near side by VIN-PGND.

5 Selection of diode

Please have and set the margin enough to the current rating of the diode for the maximum load current. Moreover, please similarly have and set the margin enough to a ratings reverse-voltage for the maximum input voltage.

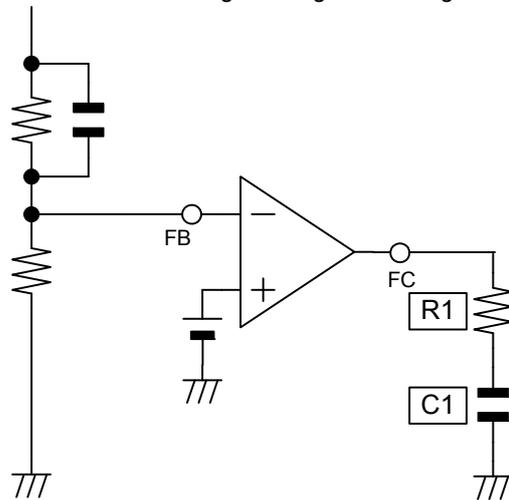


Fig.19 Phase amends part external circuit chart

6 OFFLATCH time setting method

If it continues abnormal state, BD8643FV output become low voltage and state is fixed. In this case, the OFFLATCH time can be set by connecting capacitor between PSET and GND. Please select the value of OFFLATCH time according to the following expression. Please set OFFLATCH time in 200μsec~5msec.

$$T_{TM} = \frac{C_{PSET}}{I_{PSET}(5\mu A \text{ typ})} \text{ [sec]} \cdot \cdot \cdot (11)$$

To release the off latch state, EN or VIN terminal voltage should be changed to low level once time.

● Typical application circuit

【Condition】

VOUT = 1.2V
fosc = 300kHz
OFFLATCH time = 500μsec

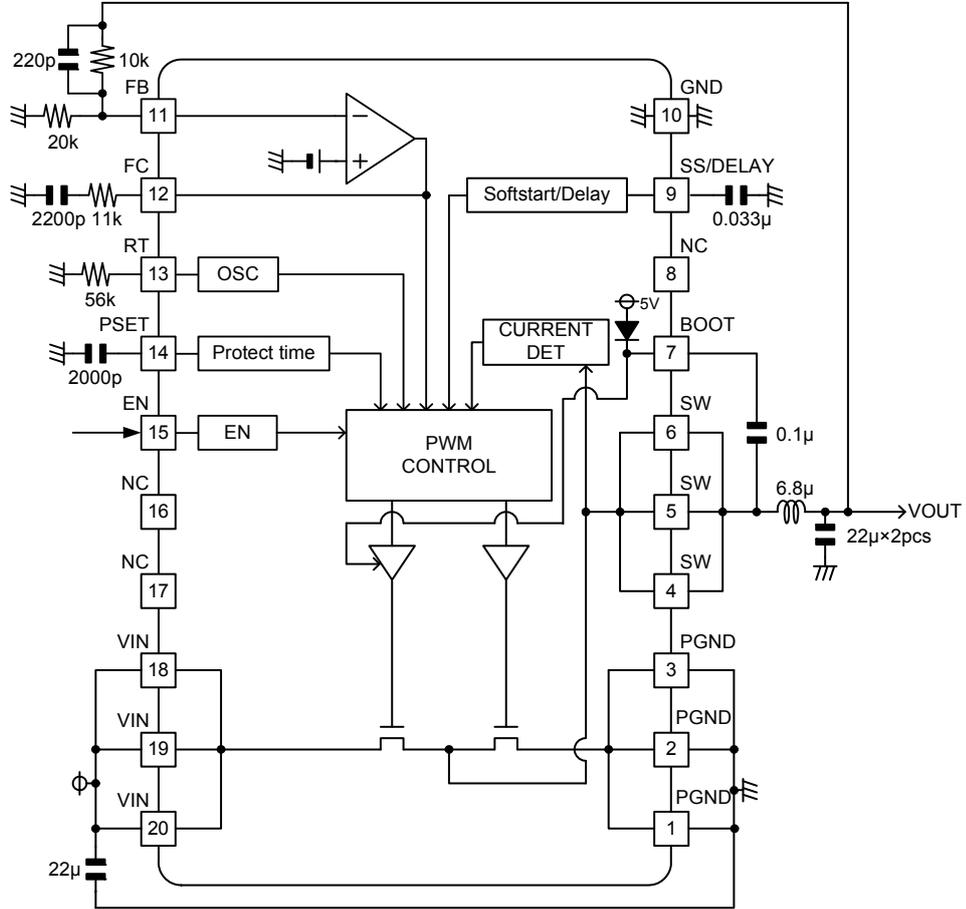
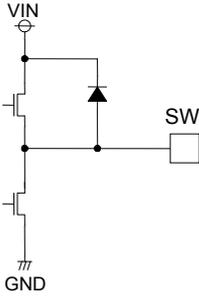
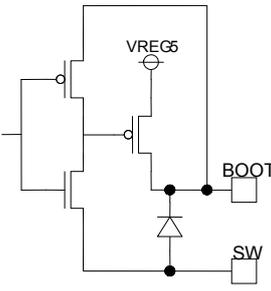
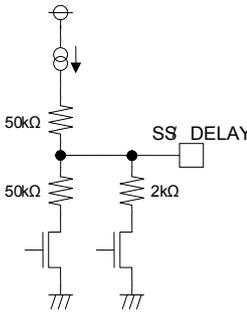
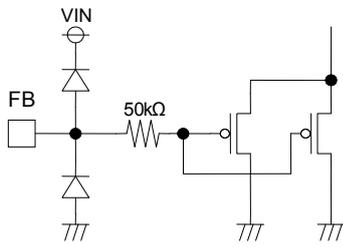
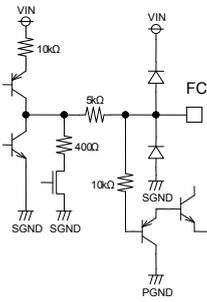
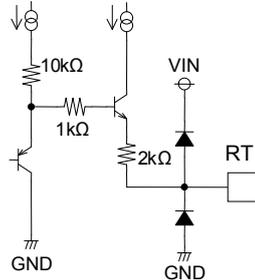
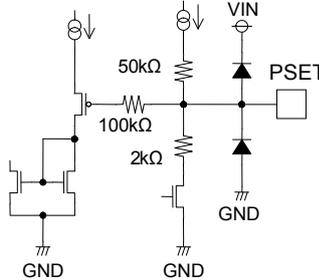
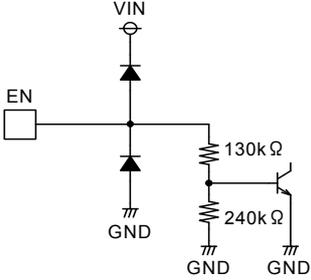


Fig.20 Typical application

● I/O equivalence circuit

4, 5, 6PIN(SW)	7PIN(BOOT)	9PIN(SS/DELAY)
		
11PIN(FB)	12PIN(FC)	13PIN(RT)
		
14PIN(PSET)	15PIN(EN)	
		

●Note for use

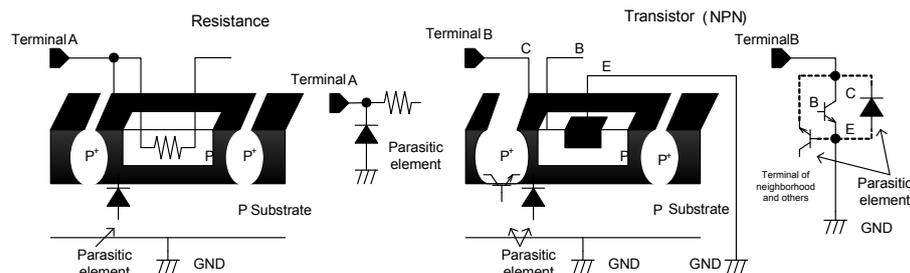
1. About the absolute maximum rating
Attention is brushed off enough to the quality control, it is likely to destroy when the absolute maximum rating such as impressed voltages (VCC_IN,DCIN) and ranges (Topr) of the operating temperature as it is exceeded, the mode of breakings of the short or the opening, etc. cannot be specified, and examine it in this IC to give physical measures for safety such as fuses when a special mode that exceeds the absolute maximum rating is assumed.
2. GND pin voltage
GND terminal should be connected the lowest voltage, under all conditions. And all terminals except SW should be under GND terminal voltage under all conditions including transient situations. If a terminal exists under GND, it should be inserting a bypass route.
3. Power dissipation
If IC is used on condition that the power loss is over the power dissipation, the reliability will become worse by heat up, such as reduced output current capability. Also, be sure to use this IC within a power dissipation range allowing enough of margin.
4. Input supply voltage
Input supply pattern layout should be as short as possible.
5. About the short and the miss-installation between terminals
Note the direction and the miss-registration of IC enough when you install it in the set substrate. IC might destroy it as well as reversely connecting the power supply connector when installing it by mistake. Moreover, there is fear of destruction when the foreign body enters between terminals, the terminal, the power supply, and grandeur and it is short-circuited.
6. About operation in strong electromagnetic field
In use in strong electromagnetic field, note that there is a possibility of malfunctioning.
7. About the inspection by the set substrate
It is likely to suffer stress to IC and discharge electricity every one process when you connect the capacitor with the pin with low impedance when inspecting it in the set substrate. Moreover, detach it after connecting after the power supply is turned off without fail when detaching it to G in the inspection process, inspecting, and turning off the power supply. In addition, be give the earth to the assembly process as a static electricity measures, and careful enough when it transports and you preserve it.
8. About each input terminal

This IC is a monolithic IC which has a P⁺ isolations and P substrate to isolate elements each other.

This P layer and an N layer in each element form a PN junction to construct various parasitic elements.

For instance, the potential difference operates in resistance as shown in the figure below when resistance and the playground connect it with the terminal and the playground (GND) >(terminal B) joint of PN operates as a parasitic diode in playground (GND) >(terminal A) transistor (NPN). In addition, the NPN transistor of parasitism works with N layer of the element of the above-mentioned parasitic diode and the neighborhood and others in transistor (NPN). A parasitic element in IC composition is inevitably formed because of the potential relation.

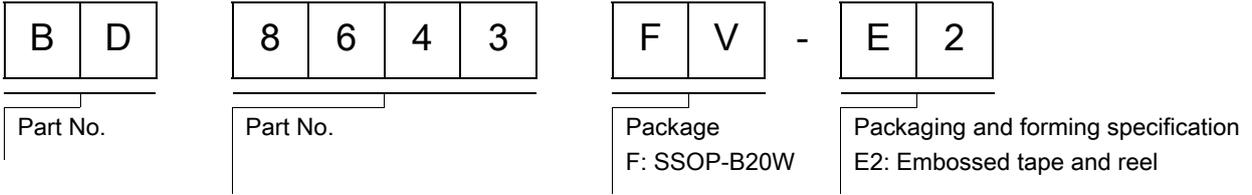
A parasitic element can operate, the interference with the circuit operation be caused, it malfunction, and, consequently, it cause destruction. Therefore, do not do the usage that a parasitic element operates as a voltage that is lower than the playground (GND;P substrate) is impressed to the input terminal enough. Moreover, do not impress the voltage to the input terminal when you do not impress the power-supply voltage to IC. Give each input terminal to me the voltage below the power-supply voltage or in the guarantee value of an electric characteristic when you similarly impress the power-supply voltage.



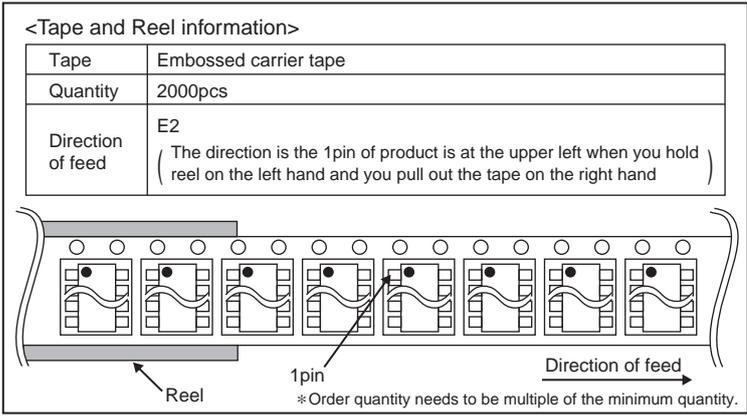
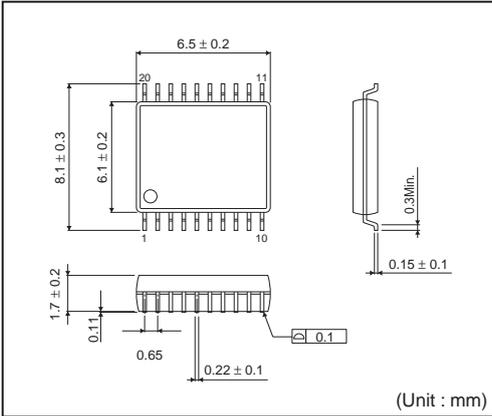
Example of IC of simple structure

9. Earth wiring pattern
If small signal GND and large current GND exist, disperse their pattern. In addition, for voltage change by pattern wiring impedance and large current not to change voltage of small signal GND, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned.
10. About each output terminal
We recommend to put Diode for protection purpose in case of output pin connected with large load of impedance or reserve current occurred at initial and output off.
11. Thermal Shut Down Circuit
A temperature control is built in the IC to prevent the damage due to overheat. Therefore, the outputs are turned off when the thermal circuit works.
12. Over Output Current Protection
SW Output terminal has over current protection circuit of 5A, with prevents IC from being damage by short circuit at over current. However, It is recommend not to use that continuously operates the protection circuit (For instance, always the load that greatly exceeds the output current ability is connected or the output is short-circuited, etc.) in these protection circuits by an effective one to the destruction prevention due to broken accident.

●Ordering part number



SSOP-B20W



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