

1024-Bit Serial (3V to 5V) Electrically Erasable PROM
with 2V Read Capability

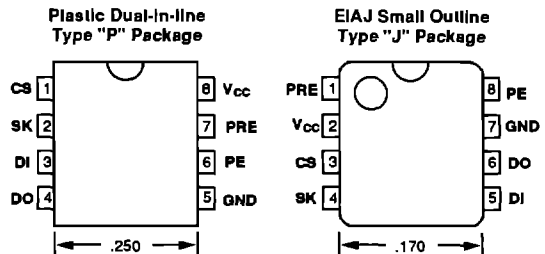
FEATURES

- **State-of-the-Art Architecture**
 - Nonvolatile data storage
 - Single supply - 3V to 5V operation
 - Full TTL compatible inputs and outputs
 - Auto Increment for efficient data dump
 - 1MHz operation
- **Hardware and Software Write Protection**
 - Defaults to write-disabled state at power up
 - Software instructions for write-enable/disable
 - Pin-enabled writes to memory and Protect Register
 - Temporary or permanent protection of selected registers
- **Low Power Consumption**
 - 1mA active (typical)
 - 1µA standby (typical)
- **Low Voltage Read Operations**
 - Reliable read operations down to 2.0 volts
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
 - Self-timed programming cycle
 - Automatic erase-before-write
 - Programming Status Indicator
 - Word and chip erasable
 - Stop SK anytime for power savings
- **Durable and Reliable**
 - 10-year data retention after 100K write cycles
 - Minimum of 100,000 write cycles per word
 - Unlimited read cycles
 - ESD protection

OVERVIEW

The XL93CS46-3 is a low cost 1024-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93CS46-3 provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Any number of the registers can be protected against data modification by programming the on-chip Protect Register. This register holds the

PIN CONFIGURATIONS



SERIAL
2
P DCTS

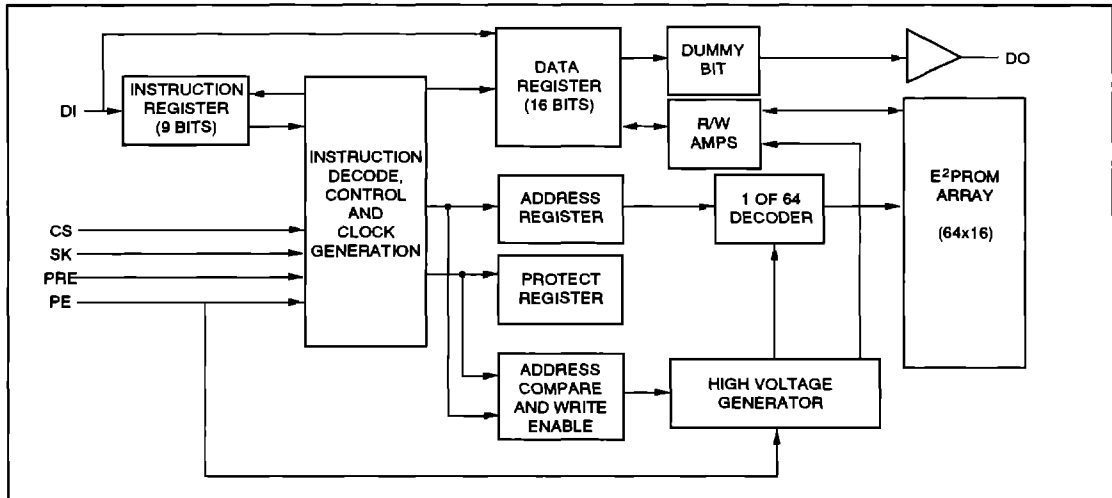
PIN NAMES

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
Vcc	Power Supply

address of the lowest memory register to be protected. The value in the Protect Register can be frozen, ensuring that the selected range of registers can never be altered. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. To protect against inadvertent writes, the WRITE instruction is accepted only while Program Enable (PE) is held HIGH, and only functions if the selected address is less than the address in the Protect Register. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/BUSY status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93CS46-3 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93CS46-3 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93CS46-3 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93CS46-3 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93CS46-3 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93CS46-3 is guaranteed to provide accurate data during read operations with VCC as low as 2.0V.

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93CS46-3 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around with CS HIGH until either the end of the array is reached or until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When VCC is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until VCC is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)

The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been applied to DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates

the self-timed programming cycle. While the WRITE instruction is being loaded, the PE pin must be held HIGH; then it becomes a DON'T-CARE.

After a minimum wait of 250ns from the falling edge of CS (tCS), if CS is brought HIGH, DO will indicate the READY/BUSY status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/BUSY flag. Therefore, it is important if you want to access the READY/BUSY flag, not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)

The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. The WRALL instruction functions only when the Protect Register has been cleared by a PRCLEAR instruction. While the WRALL instruction is being loaded, the PE pin must be held HIGH; then it becomes a DON'T-CARE.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tCS), the DO pin indicates the READY/BUSY status of the chip. (See Figure 6.)

Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When VCC is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of tCS, will cause DO to indicate the READY/BUSY status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. Registers protected by the protect register write (PRWRITE) or protect register disable (PRDS) commands cannot be erased. (See Figure 8)

Erase All (ERAL)

Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1."The erase all (ERAL)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data	PRE Pin	PE Pin
READ	1	10	(A5-A0)		0	X
WEN (Write Enable)	1	00	11XXXX		0	1
WRITE	1	01	(A5-A0)	D15-D0	0	1
WRALL (Write All Registers)	1	00	01XXXX	D15-D0	0	1
WDS (Write Disable)	1	00	00XXXX		0	X
PRREAD (Protect Register Read)	1	10	XXXXXX		1	X
PREN (Protect Register Enable)	1	00	11XXXX		1	1
PRCLEAR (Protect Register Clear)	1	11	111111		1	1
PRWRITE (Protect Register Write)	1	01	(A5-A0)		1	1
PRDS (Protect Register Disable)	1	00	000000		1	1
ERASE REGISTER	1	11	(A5-A0)		0	1
ERAL (Erase All Registers)	1	00	10XXXX		0	1

command will not erase registers protected by the protect register write (PRWRITE) or protect register disable (PRDS) commands. (See Figure 9.)

PROTECTION REGISTER LOGIC

Protect Register Read (PRREAD)

The protect register read (PRREAD) instruction causes the address stored in the Protect Register to be output on the DO pin. Data is transferred from the Protect Register into a serial-out shift register. A dummy bit (logical "0") precedes the actual output string. The data on the DO pin changes with the LOW to HIGH transition of the SK clock. While the PRREAD instruction is being loaded, the PRE pin must be held HIGH; then it becomes a DON'T-CARE. (See Figure 10.)

After a PRCLEAR instruction is executed, a PRREAD instruction will return all 1's, even though the highest register is NOT protected.

Protect Register Enable (PREN)

The protect register enable (PREN) instruction enables execution of the PRCLEAR, PRWRITE and PRDS instructions. It must be executed immediately before each of these instructions. (The PREN instruction functions only if the part has been write enabled; see the WEN instruction). Both the PRE and PE pins must be held HIGH while the PREN instruction is being loaded; then they become DON'T-CARES. (See Figure 11.)

Protect Register Clear (PRCLEAR)

The protect register clear (PRCLEAR) instruction clears the address stored in the Protect Register, making all registers accessible to the WRITE and WRALL instructions. If a PRDS instruction has been executed, the PRCLEAR instruction will not function. A PREN instruction must be executed immediately before a PRCLEAR instruction. While the PRCLEAR instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CARES.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tCS), the DO pin indicates the READY/BUSY status of the chip. (See Figure 12.)

Protect Register Write (PRWRITE)

The protect register write (PRWRITE) instruction is used to load the Protect Register with the address of the lowest register to be protected. After the PRWRITE instruction is executed, only registers with addresses less than the address in the Protect Register can be written by the WRITE instruction. The Protect Register must have been cleared (see the PRCLEAR instruction) before executing

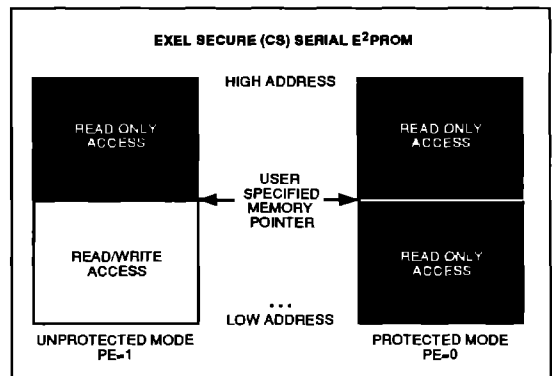
a PRWRITE instruction. A PREN instruction must be executed immediately before the PRWRITE instruction. While the PRWRITE instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CARES.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tCS), the DO pin indicates the READY/BUSY status of the chip. (See Figure 13.)

Protect Register Disable (PRDS)

The protect register disable (PRDS) instruction is effective exactly once per part. After this instruction has been executed, the Protect Register will accept no further modifications. All registers with addresses greater than or equal to the address in the Protect Register are permanently protected from the WRITE and WRALL operations. A PREN instruction must be executed immediately before the PRDS instruction. While the PRDS instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CARES.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tCS), the DO pin indicates the READY/BUSY status of the chip. (See Figure 14.)



The figure above shows the status of the memory array regions as defined by the pointer address and the state of the program enable (PE) pin. In the first case, programming operations are enabled through the application of a logic "1" to the PE control pin. All memory locations beneath that of the pointer address are available for data changes. All memory locations at or above the pointer address are protected against data alteration and serve as read only memory.

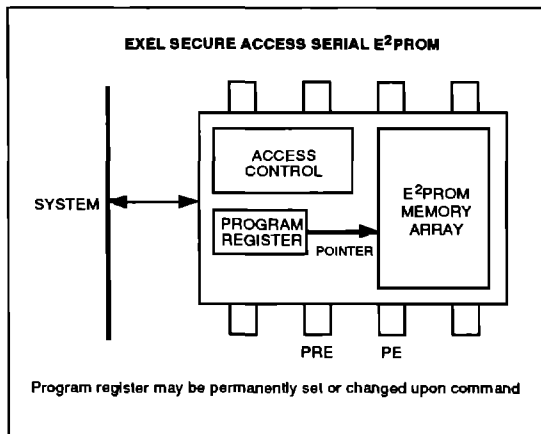
In the second case, the PE pin is held in a logic "0" state. While this condition is present the XL93CS46-3 is protected against any data changes.

The conceptual block diagram on the right shows the simplicity with which the security features of the XL93CS46-3 may be managed.

The program register is accessed for read or write operations whenever the program register enable (PRE) pin is in a logic "1" state. Normal write operations to the program register establish the E² memory array address defining the region to be protected.

When PRE is in a logic "0" state, all read and write operations directed to the XL93CS46-3 affect the E²PROM memory array locations.

Setting the address in the program register to the top of the XL93CS46-3 memory array renders the entire array to be writable. Setting the address to the bottom of the array renders the entire array to be a read only memory.



SERIAL
2
P DCTS

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: S93CS46-3	0°C to +70°C
E93CS46-3	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage with Respect to Ground	-0.3 to +6.5V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C or -40°C to +85°C for E93CS46-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	S93CS46-3		E93CS46-3		Units
			Min	Max	Min	Max	
I _{CC1}	Operating Current CMOS Input Levels	CS = V _{IH} , SK = 250KHz		2		2	mA
I _{CC3}	Standby Current	PRE = CS = 0V DI = SK = PE = V _{CC}		20		3	µA
I _{LI}	Input Leakage	V _{IN} = 0V to V _{CC} , PE and PRE	-15 0	15 0	-20 0	20 0	µA
I _{LI}	Input Leakage	V _{IN} = 0V to V _{CC} , CS, SK, DI	-1	1	-1	1	µA
I _{LO}	Output Leakage	V _{OUT} = 0V to V _{CC} , CS = 0V	-1	1	-1	1	µA
V _{IL}	Input Low Voltage		-0.1	0.15 V _{CC}	-0.1	0.15 V _{CC}	V
V _{IH}	Input High Voltage		0.8 V _{CC}	V _{CC}	0.8 V _{CC}		V
V _{OL1}	Output Low Voltage	I _{OL} = 1 0mA TTL		0.3		0.3	V
V _{OH1}	Output High Voltage	I _{OH} = -400µA TTL	2.4		2.4		V
V _{OL2}	Output Low Voltage	I _{OL} = 10µA CMOS		0.2		0.2	V
V _{OH2}	Output High Voltage	I _{OH} = -10µA CMOS	V _{CC} -0.2		V _{CC} -0.2		V

AC ELECTRICAL CHARACTERISTICS

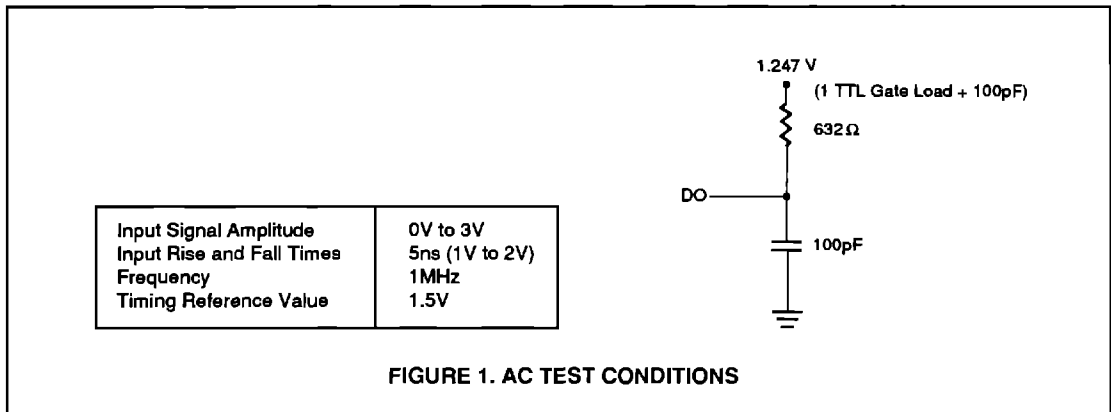
T_A = 0°C to +70°C or -40°C to +85°C for E93CS46-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	S93CS46-3		E93CS46-3		Units
			Min	Max	Min	Max	
fsk	SK Clock Frequency		0	250	0	250	KHz
tsKH	SK High Time		1		1		µs
tsKL	SK Low Time		1		1		µs
tcs	Minimum CS Low Time		1		1		µs
tcSS	CS Setup Time	Relative to SK	200		200		ns
tpRES	PRE Setup Time	Relative to SK	200		200		ns
tpES	PE Setup Time	Relative to SK	200		200		ns
tdIS	DI Setup Time	Relative to SK	400		400		ns
tCSH	CS Hold Time	Relative to SK	0		0		ns
tpEH	PE Hold Time	Relative to CS	200		200		ns
tpREH	PRE Hold Time	Relative to CS	200		200		ns
tdIH	DI Hold Time	Relative to SK	400		400		ns
tpD1	Output Delay to "1"	AC Test		2		2	µs
tpD0	Output Delay to "0"	AC Test		2		2	µs
tsV	CS to Status Valid	AC Test		2		2	µs
tdF	CS to DO in 3-state	CS = V _{IL}		400		400	ns
tWP	Write Cycle Time			25		25	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C _{OUT}	Output Capacitance	5	pF
C _{IN}	Input Capacitance	5	pF



DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C or -40°C to +85°C for E93CS46-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	S93CS46-3		E93CS46-3		Units
			Min	Max	Min	Max	
I _{CC1}	Operating Current CMOS Input Levels	CS = V _{CC} , SK = 1MHz		2		2	mA
I _{CC2}	Operating Current TTL Input Levels	CS = V _{IH} , SK = 1MHz		5		5	mA
I _{SB}	Standby Current	CS = DI = SK = 0V		2		2	µA
I _{IU}	Input Leakage	V _{IN} = 0V to V _{CC} , PE and PRE	-20.0	20.0	-20.0	20.0	µA
I _{IU}	Input Leakage	V _{IN} = 0V to V _{CC} , CS, SK, DI	-1	1	-1	1	µA
I _{LO}	Output Leakage	V _{OUT} = 0V to V _{CC} , CS = 0V	-1	1	-1	1	µA
V _{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V _{IH}	Input High Voltage		2	V _{CC}	2	V _{CC}	V
V _{OL1}	Output Low Voltage	I _{OL} = 2.1mA TTL		0.4		0.4	V
V _{OH1}	Output High Voltage	I _{OH} = -400µA TTL	2.4		2.4		V
V _{OL2}	Output Low Voltage	I _{OL} = 10µA CMOS		0.2		0.2	V
V _{OH2}	Output High Voltage	I _{OH} = -10µA CMOS	V _{CC} -0.2		V _{CC} -0.2		V

SERIAL
2
P DCTS

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C or -40°C to +85°C for E93CS46-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	S93CS46-3		E93CS46-3		Units
			Min	Max	Min	Max	
f _{SK}	SK Clock Frequency		0	1	0	1	MHz
t _{SKH}	SK High Time		400		400		ns
t _{SKL}	SK Low Time		250		250		ns
t _{CS}	Minimum CS Low Time		250		250		ns
t _{CSS}	CS Setup Time	Relative to SK ⌋	50		50		ns
t _{PRES}	PRE Setup Time	Relative to SK ⌋	50		50		ns
t _{PES}	PE Setup Time	Relative to SK ⌋	50		50		ns
t _{DIS}	DI Setup Time	Relative to SK ⌋	100		100		ns
t _{CSH}	CS Hold Time	Relative to SK ⌋	0		0		ns
t _{PEH}	PE Hold Time	Relative to CS ⌋	50		50		ns
t _{PREH}	PRE Hold Time	Relative to CS ⌋	50		50		ns
t _{DIH}	DI Hold Time	Relative to SK ⌋	100		100		ns
t _{PD1}	Output Delay to "1"	AC Test		500		500	ns
t _{PD0}	Output Delay to "0"	AC Test		500		500	ns
t _{SV}	CS to Status Valid	AC Test C _L = 100pF		500		500	ns
t _{DF}	CS to DO in 3-state	CS = Low to DO = HI-Z		100		100	ns
t _{WP}	Write Cycle Time	CS = Low to DO = Ready		10		10	ms

