MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC54/74HC4016

Advance Information

Quad Analog Switch/ Multiplexer/Demultiplexer

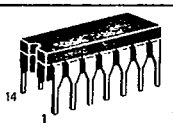
High-Performance Silicon-Gate CMOS

The MC54/74HC4016 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

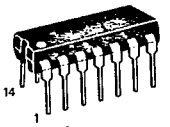
The HC4016 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

This device is identical in both function and pinout to the HC4066. The ON/OFF Control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316. For analog switches with lower R_{ON} characteristics, use the HC4066.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range (V_{CC} – GND) = 2.0 to 12.0 Volts
- Analog Input Voltage Range (V_{CC} – GND) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 32 FETs or 8 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

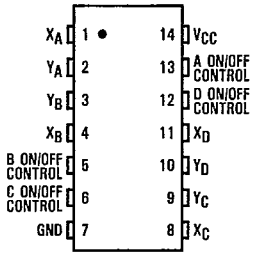
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

T_A = –55° to 125°C for all packages.
Dimensions in Chapter 7.

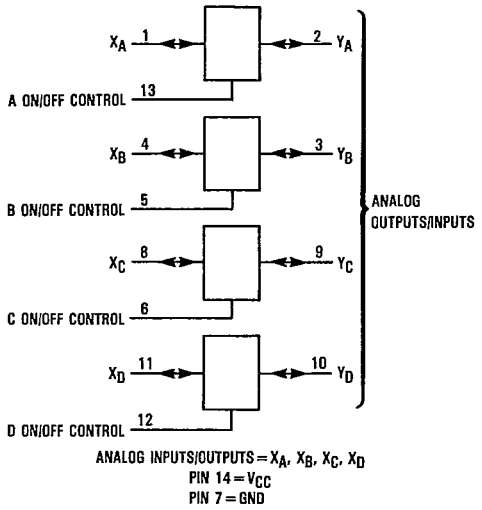
PIN ASSIGNMENT



FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

LOGIC DIAGRAM



ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D
PIN 14 = V_{CC}
PIN 7 = GND

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC54/74HC4016

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	−0.5 to +14.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
I	DC Current Into or Out of Any Pin	±25	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch	—	1.2	V
T_A	Operating Temperature, All Package Types	−55	+125	°C
t_r, t_f	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10)			ns
	V_{CC} = 2.0 V	0	1000	
	V_{CC} = 4.5 V	0	500	
	V_{CC} = 9.0 V	0	400	
	V_{CC} = 12.0 V	0	250	

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn, i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected uless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit 25°C to −55°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High-Level Voltage ON/OFF Control Inputs	R_{on} = per spec	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			9.0	6.3	6.3	6.3	
			12.0	8.4	8.4	8.4	
V_{IL}	Maximum Low-Level Voltage ON/OFF Control Inputs	R_{on} = per spec	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			9.0	1.8	1.8	1.8	
			12.0	2.4	2.4	2.4	
I_{in}	Maximum Input Leakage Current, ON/OFF Control Inputs	V_{in} = V_{CC} or GND	12.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND, V_{IO} = 0 V	6.0	2	20	40	μA
			12.0	8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 4.

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DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
R_{on}	Maximum "ON" Resistance	$V_{in}=V_{IH}$ $V_{IS}=V_{CC}$ to GND $I_S \le 2.0$ mA (Figures 1, 2)	2.0†	—	—	—	Ω
			4.5	320	400	480	
			9.0	170	215	255	
			12.0	170	215	255	
		$V_{in}=V_{IH}$ $V_{IS}=V_{CC}$ or GND (Endpoints) $I_S \le 2.0$ mA (Figures 1, 2)	2.0	—	—	—	
			4.5	180	225	270	
			9.0	135	170	205	
			12.0	135	170	205	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in}=V_{IH}$ $V_{IS}=1/2\ (V_{CC}-GND)$ $I_S \le 2.0$ mA	2.0	—	—	—	Ω
			4.5	30	35	40	
			9.0	20	25	30	
			12.0	20	25	30	
I_{off}	Maximum Off-Channel Leakage Current, Any One Channel	$V_{in}=V_{IL}$ $V_{IO}=V_{CC}$ or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μA
I_{on}	Maximum On-Channel Leakage Current, Any One Channel	$V_{in}=V_{IH}$ $V_{IS}=V_{CC}$ or GND (Figure 4)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V_{CC} − GND) approaching 2 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.
NOTE: Information on typical parametric values can be found in Chapter 4.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, ON/OFF Control Inputs: $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0	50	65	75	ns
		4.5	10	13	15	
		9.0	10	13	15	
		12.0	10	13	15	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	150	190	225	ns
		4.5	30	38	45	
		9.0	30	38	45	
		12.0	30	38	45	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	125	160	185	ns
		4.5	25	32	37	
		9.0	25	32	37	
		12.0	25	32	37	
C	Maximum Capacitance — ON/OFF Control Input	—	10	10	10	pF
	Control Input = GND Analog I/O	—	35	35	35	
	Feedthrough	—	1.0	1.0	1.0	

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

Symbol	Power Dissipation Capacitance (Per Switch) (Figure 13) Used to determine the no-load dynamic power consumption: $P_D = C_{PD}\ V_{CC}^2 f + I_{CC}\ V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V	Unit
C_{PD}		15	pF

MC54/74HC4016

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND unless noted)

Symbol	Parameter	Test Conditions	V_{CC} V	Limit* 25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads −3 dB R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off-Channel Feedthrough Isolation (Figure 6)	f_{in} = Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	−50 −50 −50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	−40 −40 −40	
—	Feedthrough Noise, Control to Switch (Figure 7)	V_{in} ≤ 1 MHz Square Wave ($t_r = t_f$ = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	60 130 200	mVpp
		R_L = 10 kΩ, C_L = 10 pF	4.5 9.0 12.0	30 65 100	
—	Crosstalk Between Any Two Switches (Figure 12)	f_{in} = Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	4.5 9.0 12.0	−70 −70 −70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	4.5 9.0 12.0	−80 −80 −80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 8.0 V_{PP} sine wave V_{IS} = 11.0 V_{PP} sine wave	 4.5 9.0 12.0	 0.10 0.06 0.04	%

*Guaranteed limits not tested. Determined by design and verified by qualification.

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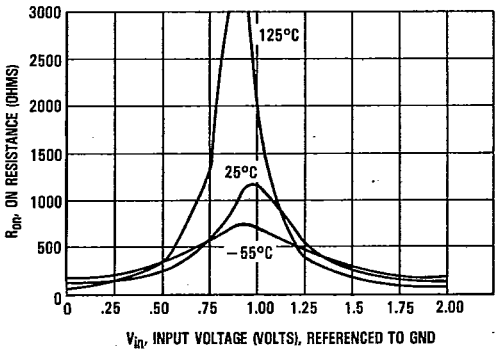


Figure 1a. Typical On Resistance, V_{CC}=2.0 V

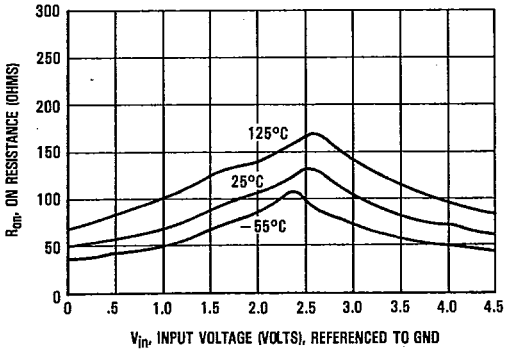


Figure 1b. Typical On Resistance, V_{CC}=4.5 V

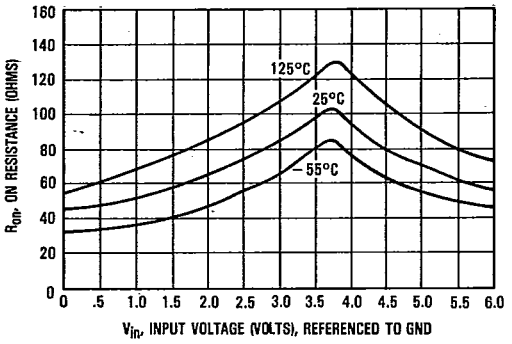


Figure 1c. Typical On Resistance, V_{CC}=6.0 V

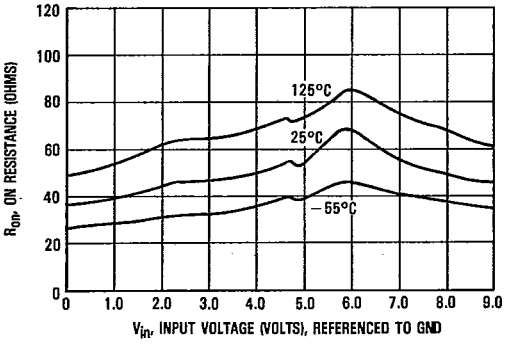


Figure 1d. Typical On Resistance, V_{CC}=9.0 V

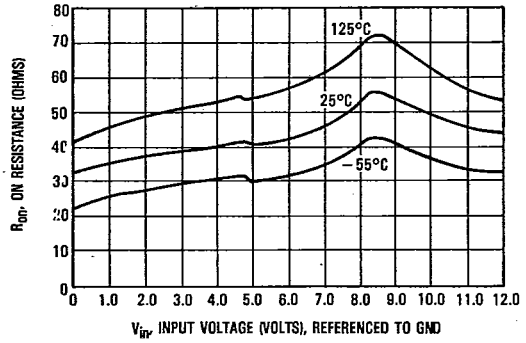


Figure 1e. Typical On Resistance, V_{CC}=12.0 V

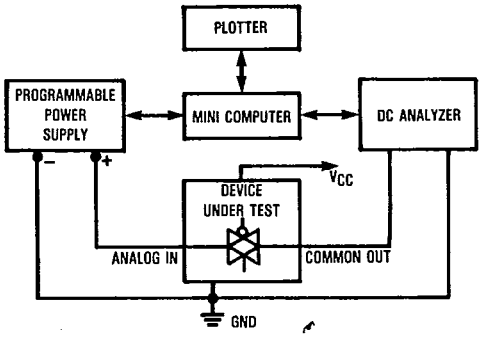


Figure 2. On Resistance Test Set-Up

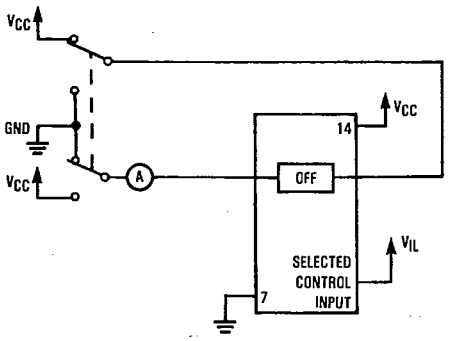


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

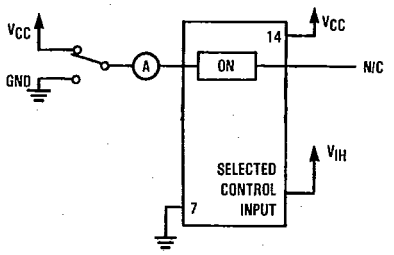
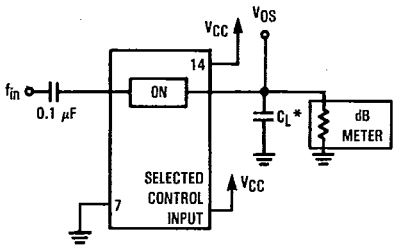
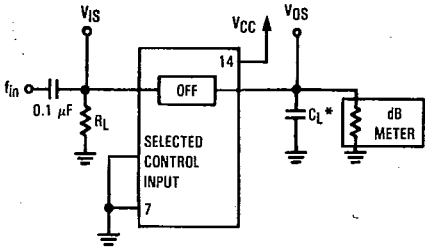


Figure 4. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



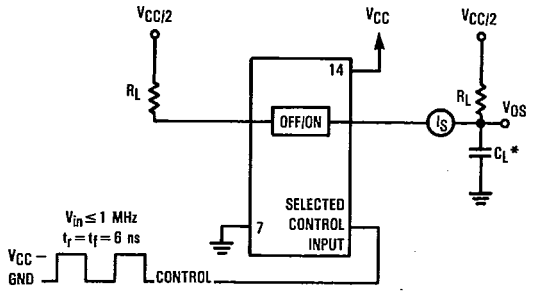
*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth Test Set-Up



*Includes all probe and jig capacitance.

Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

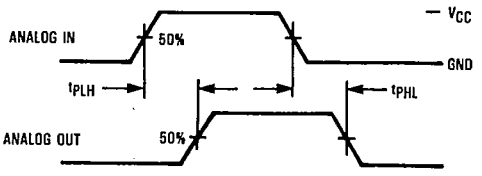
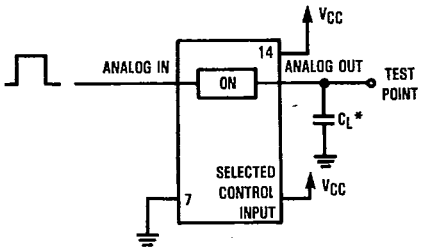


Figure 8. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

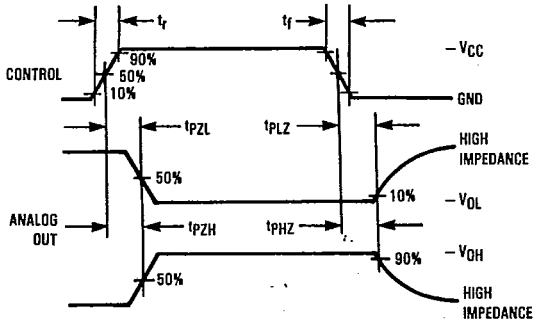
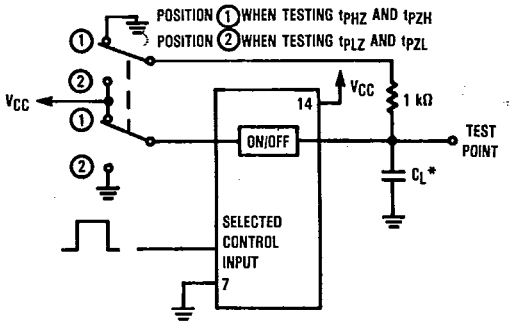
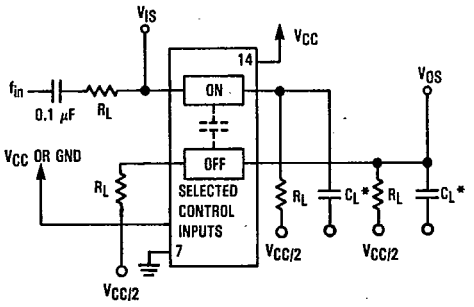


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

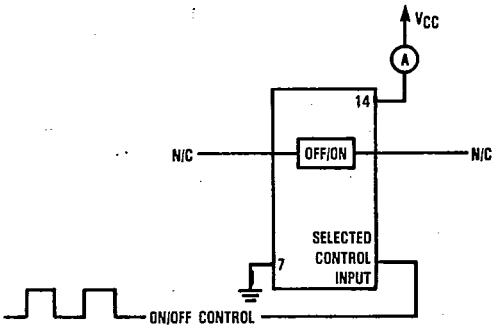
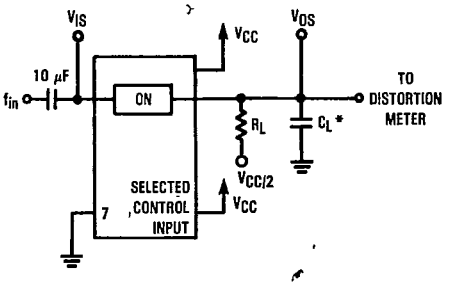


Figure 13. Power Dissipation Capacitance Test Set-Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up

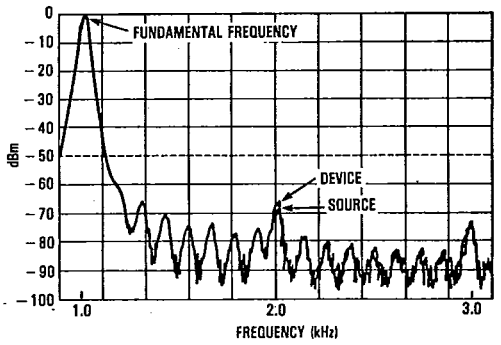


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The ON/OFF Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and GND. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below GND. In the example below, the difference between V_{CC} and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MO•sorbs (Motorola high current surge protectors). MO•sorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear-out mechanism.

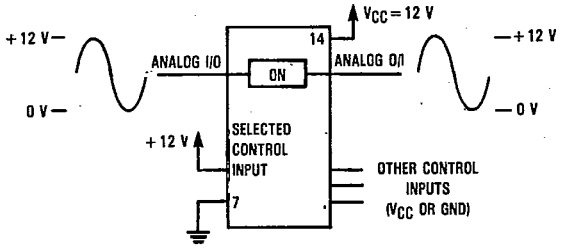


Figure 16. 12 V Application

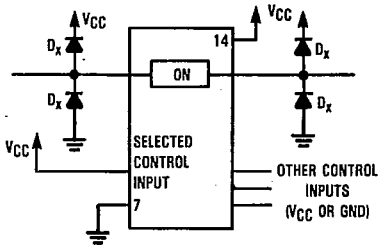
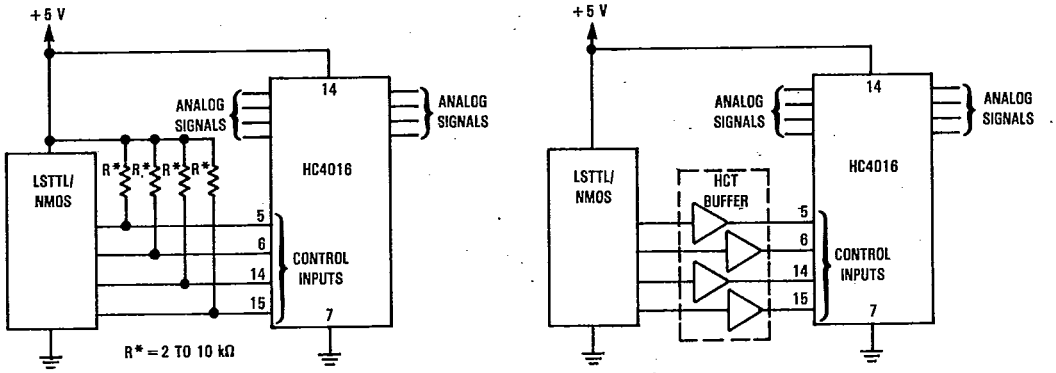


Figure 17. Transient Suppressor Application



a. Using Pull-Up Resistors

b. Using HCT Buffer

Figure 18. LSTTL/NMOS to HCMOS Interface

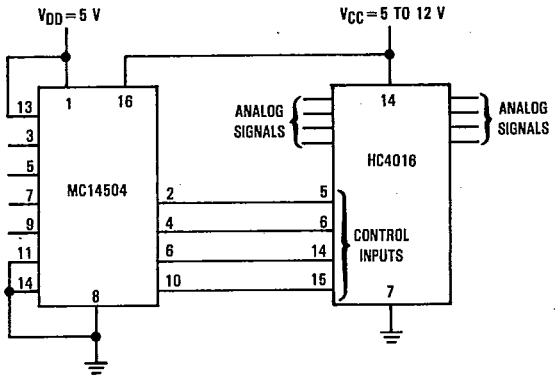


Figure 19. TTL/NMOS-to-CMOS Level Converter
Analog Signal Peak-to-Peak Greater than 5 V
(Also see HC4316)

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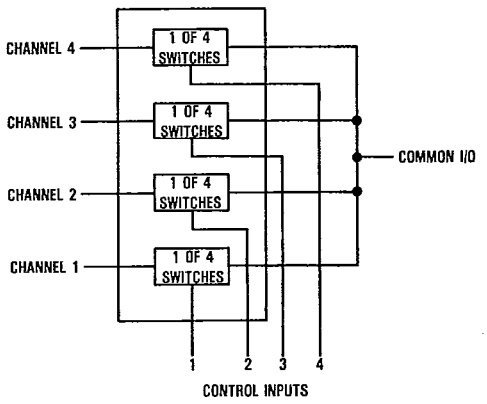

Figure 20. 4-Input Multiplexer

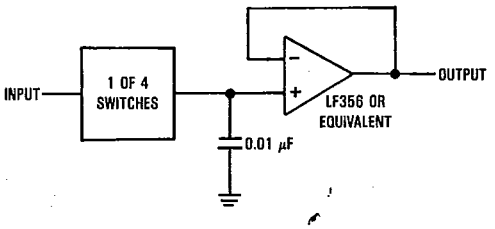

Figure 21. Sample/Hold Amplifier