μPD431004
262,144 x 4-Bit
Static CMOS RAM

Description

The μPD431004 is a 262,144-word by 4-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD431004 a high-speed device that requires very low power and no clock or refreshing.

The μPD431004 is available in standard 28-pin plastic SOJ packaging.

Features

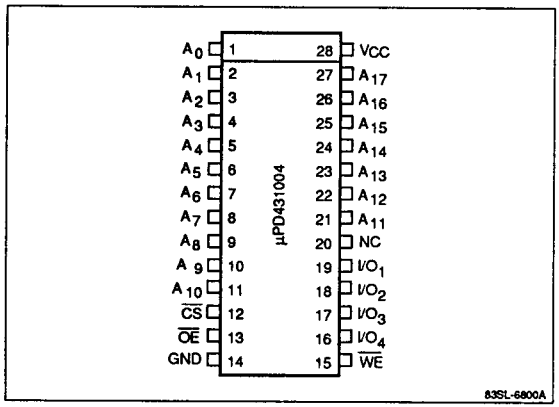
- 262,144-word x 4-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Low power dissipation
  - 150 mA max (active)
  - 2 mA max (standby)
- Standard 28-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD431004LE-20	20 ns	28-pin plastic SOJ
LE-25	25 ns	
LE-35	35 ns	

Pin Configuration

28-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.3
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V minimum for 10 ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz (Note 1)

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	I_{CC}
Not selected	H	X	X	High-Z	Standby
Output disable	L	H	H	High-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Notes:

(1) X = don't care.

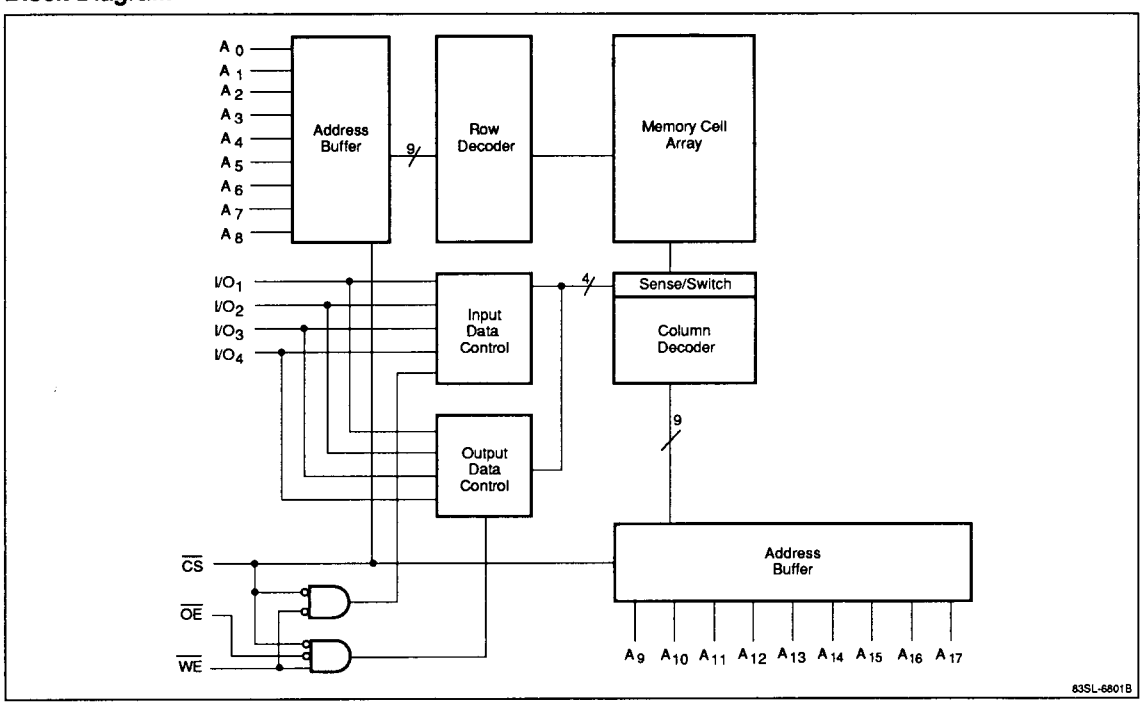
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V minimum for 10 ns pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD431004-20		μPD431004-25		μPD431004-35			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		150		140		120	mA	$\overline{CS}$ = V_{IL}; t_{RC} = t_{RC} (min); I_{DOUT} = 0 mA
Read cycle time	t_{RC}	20		25		35		ns	(Note 2)
Address access time	t_{AA}		20		25		35	ns	
Chip select access time	t_{ACS}		20		25		35	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Output enable access time	t_{OE}		10		10		15	ns	
Output enable to output in low-Z	t_{OLZ}	0		0		0		ns	(Note 3)
Output disable to output in high-Z	t_{OHZ}	0	8	0	10	0	15	ns	(Note 4)
Chip selection to output in low-Z	t_{CLZ}	5		5		5		ns	(Note 3)
Chip selection to output in high-Z	t_{CHZ}	0	8	0	10	0	15	ns	(Note 4)
Write Operation									
Write cycle time	t_{WC}	20		25		35		ns	(Note 2)
Chip select to end of write	t_{CW}	15		20		30		ns	
Address valid to end of write	t_{AW}	15		20		30		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	15		20		30		ns	
Write recovery time	t_{WR}	3		3		3		ns	
Data valid to end of write	t_{DW}	12		12		20		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}	0	8	0	8	0	10	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the load shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 2.

Figure 1. Output Load

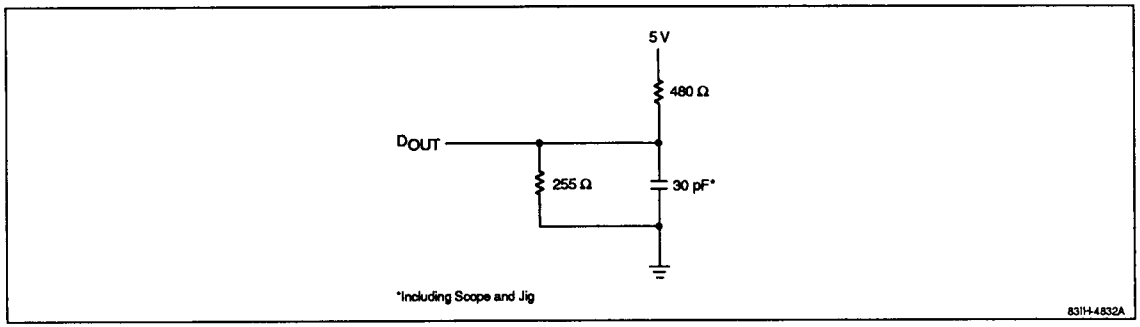
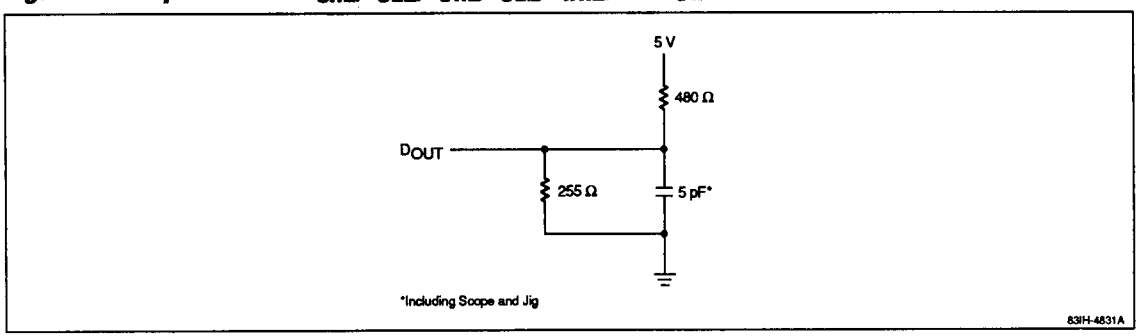
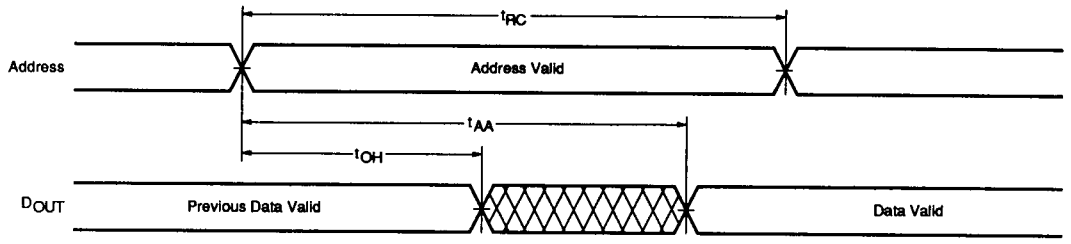


Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

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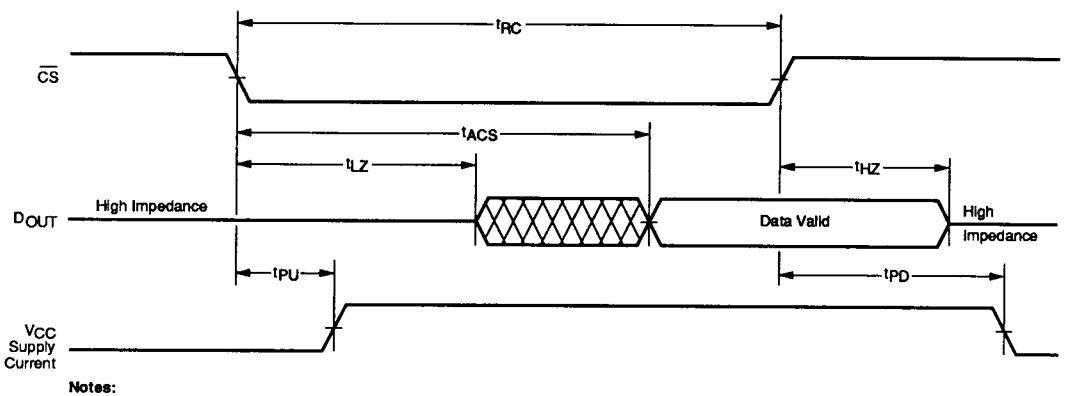
Chip Select Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.
[3] $\overline{OE} = V_{IL}$.

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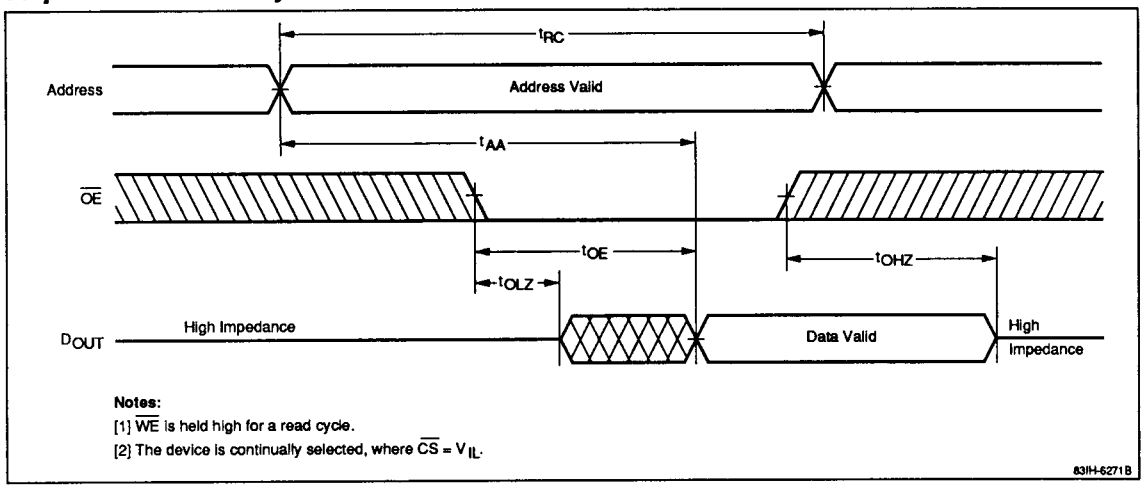
Timing Waveforms (cont)

Output Enable Access Cycle



Notes:

[1] $\overline{WE}$ is held high for a read cycle.

[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

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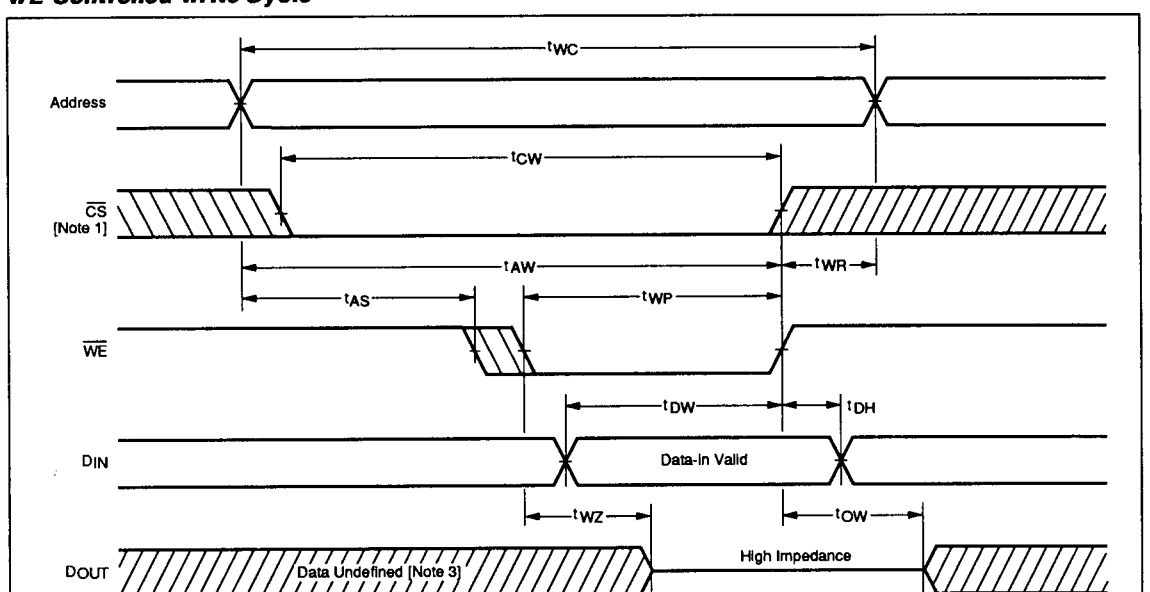
$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[3] During this period, the I/O pins may be active ($\overline{OE}$ low). Therefore, data input signals of opposite polarity to the outputs must not be applied.

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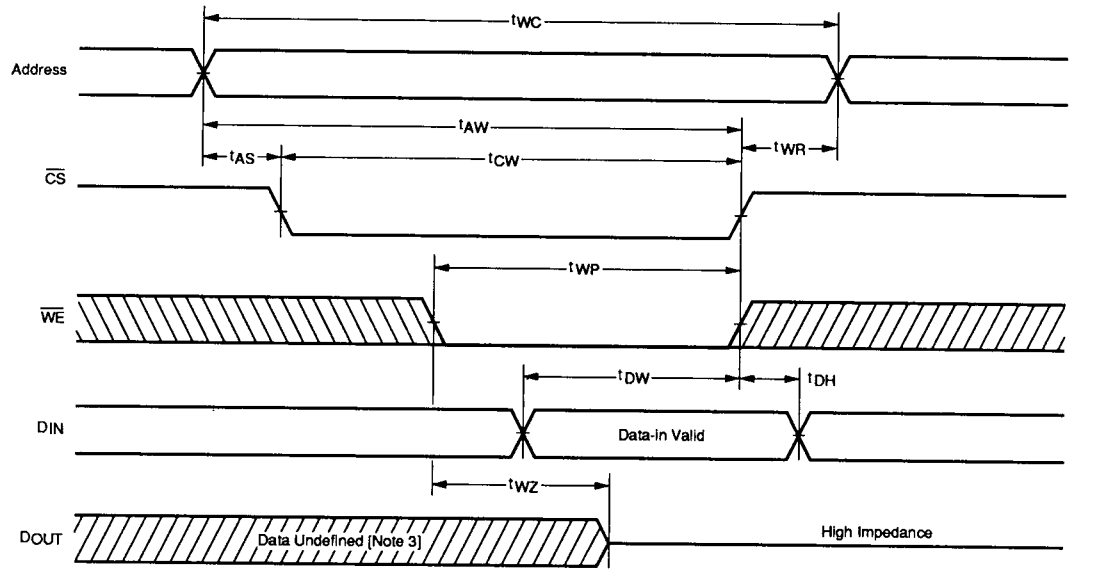
Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[3] During this period, the I/O pins may be active ($\overline{OE}$ low). Therefore, data input signals of opposite polarity to the outputs must not be applied.

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