

**REVISION HISTORY**

REVISION	DESCRIPTION	Released DATE
Preliminary Rev. 0.5	Original.	Mar, 2001
Rev. 1.0	1. The symbols CE# and OE# and WE# are revised as \overline{CE} and \overline{OE} and \overline{WE} . 2. Separate Industrial and Consumer SPEC. 3. Add access time 55ns range.	Jun 21,2001
Rev. 1.1	Add STSOP package	Aug 3,2001
Rev. 1.2	Add SOP package	Mar 25,2002
Rev. 1.3	1. Revised 36-pin TFBGA package outline dimension : a、 Rev. 1.2 : ball diameter=0.3mm b、 Rev. 1.3 : ball diameter=0.35mm 2. Revised DC ELECTRICAL CHARACTERISTICS : c、 Revised V_{IH} as 2.2V	May 3,2002
Rev. 1.4	1. Revised Operation current : - $I_{CC}(\max)$ 45/35/25mA→40/30/25mA - $I_{CC}(\text{Typ})$ 30/25/20mA→30/20/16mA 2. Revised Standby current : 20/3uA→20/2uA 3. Revised $V_{OH}(\text{Typ})$: NA→2.7V 4. Add $V_{IH}(\max)=V_{CC}+2.0V$ for pulse width less than 10ns. $V_{IL}(\min)=V_{SS}-2.0V$ for pulse width less than 10ns. 5. Revised AC Table t_{OHZ} characteristics 6. Add order information for lead free product	May 8,2003



FEATURES

- Fast Access time : 55/70/100ns
- CMOS Low power operating
 - Operating current : 40/30/25mA (Icc max.)
 - Standby current : 20µA (typ.) L-version
 - 2µA (typ.) LL-version
- Single 2.7V~3.6V power supply
- Operating Temperature :
 - Commercial : 0 ~70
 - Extended : -20 ~80
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min)
- Package : 32-pin 450 mil SOP
 - 32-pin 8mm x 20mm TSOP-
 - 32-pin 8mm x 13.4mm STSOP
 - 36-pin 6mm x 8mm TFBGA

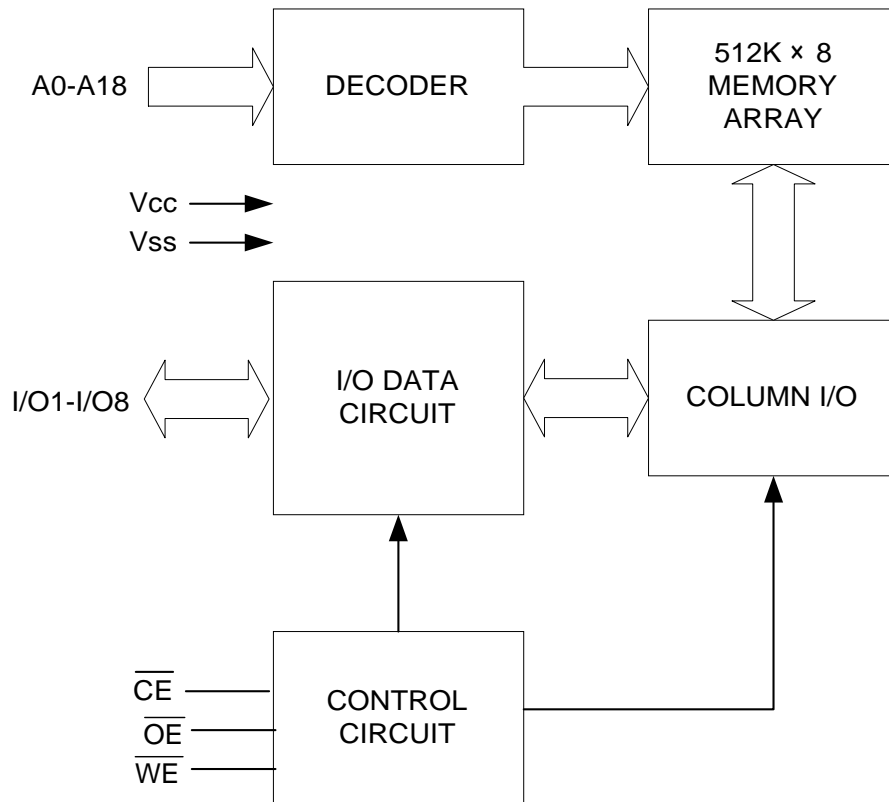
GENERAL DESCRIPTION

The UT62L5128 is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT62L5128 operates from a wide range 2.7V~3.6V power supply and supports extended operating temperature range.

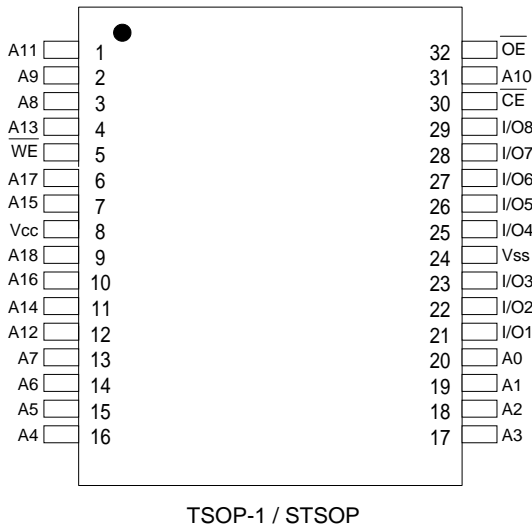
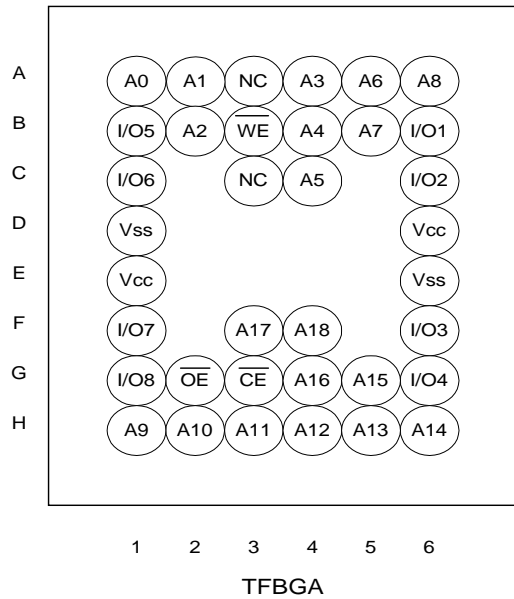
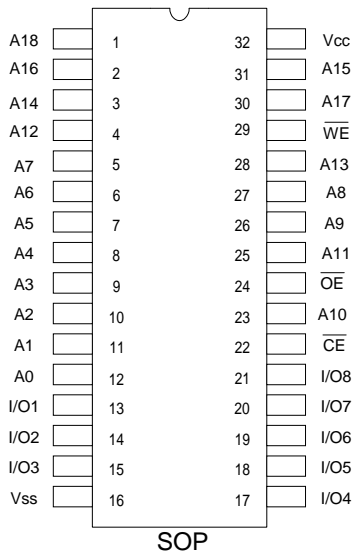
The UT62L5128 is designed for high density and low power memory applications. The device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.5V.

FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Commercial	0 to 70	
	Extended	-20 to 80	
Storage Temperature	T_{STG}	-65 to 150	
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 secs)	T_{solder}	260	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	\overline{WE}	\overline{CE}	\overline{OE}	I/O OPERATION	SUPPLY CURRENT
Standby	X	H	X	High - Z	I_{SB}, I_{SB1}
Output Disable	H	L	H	High - Z	I_{CC}, I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7V \sim 3.6V$, $T_A = 0$ to 70 / -20 to 80 (E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Power Voltage	V_{CC}		2.7	3.0	3.6	V		
Input High Voltage	V_{IH}^{*1}		2.2	-	$V_{CC}+0.3$	V		
Input Low Voltage	V_{IL}^{*2}		-0.2	-	0.6	V		
Input Leakage Current	I_{LI}	V_{SS}, V_{IN}, V_{CC}	-1	-	1	μA		
Output Leakage Current	I_{LO}	$V_{SS}, V_{I/O}, V_{CC}$, Output Disable	-1	-	1	μA		
Output High Voltage	V_{OH}	$I_{OH} = -1mA$	2.2	2.7	-	V		
Output Low Voltage	V_{OL}	$I_{OL} = 2.1mA$	-	-	0.4	V		
Operating Power Supply Current	I_{CC}	Cycle time=Min, 100% duty $I_{I/O} = 0mA, \overline{CE} = V_{IL}$	55	-	30	40	mA	
			70	-	20	30	mA	
			100	-	16	25	mA	
Average Operating Current	I_{CC1}	100% duty, $I_{I/O} = 0mA, \overline{CE} = 0.2$, other pins at 0.2V or $V_{CC}-0.2V$	TCycle=1 μs		-	4	5	mA
	I_{CC2}		TCycle=500ns		-	8	10	mA
Standby Current(TTL)	I_{SB1}	$\overline{CE} = V_{IH}$, other pins = V_{IH} or V_{IL}	-	0.3	0.5	mA		
Standby Current(CMOS)	I_{SB1}	$\overline{CE} = V_{CC}-0.2V$ other pins at 0.2V or $V_{CC}-0.2V$	-L	-	20	80	μA	
			-LL	-	2	20	μA	

Notes:

1. Overshoot : $V_{CC}+2.0v$ for pulse width less than 10ns.
2. Undershoot : $V_{SS}-2.0v$ for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

**CAPACITANCE** ($T_A=25$, $f=1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30\text{pF}+1\text{TTL}$, $I_{OH}/I_{OL} = -1\text{mA}/2.1\text{mA}$

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7\text{V}\sim 3.6\text{V}$, $T_A = 0$ to 70 / -20 to 80 (E))**(1) READ CYCLE**

PARAMETER	SYMBOL	UT62L5128-55		UT62L5128-70		UT62L5128-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	100	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t_{CLZ}^*	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}^*	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ}^*	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t_{OHZ}^*	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns

(2) WRITE CYCLE

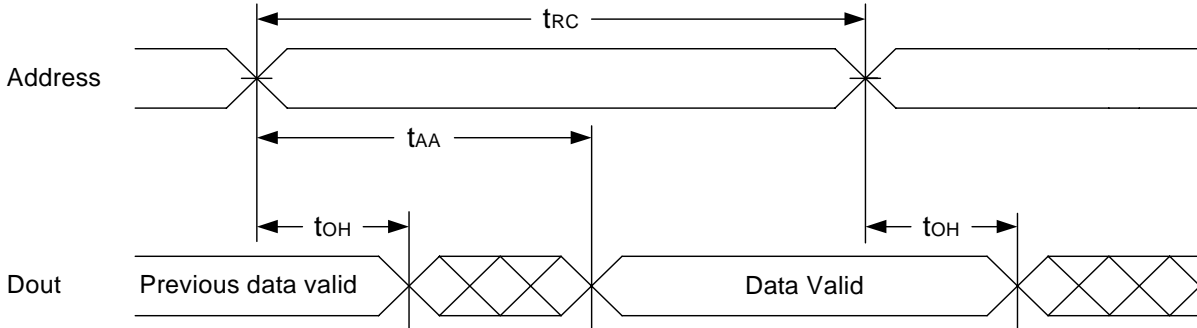
PARAMETER	SYMBOL	UT62L5128-55		UT62L5128-70		UT62L5128-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t_{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ}^*	-	30	-	30	-	40	ns

*These parameters are guaranteed by device characterization, but not production tested.

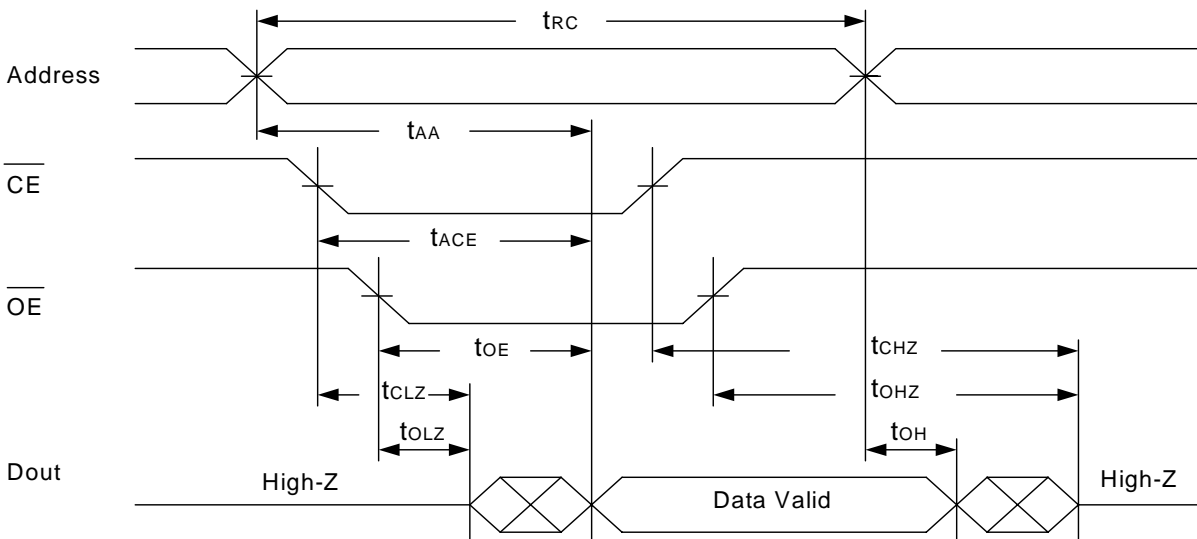


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (\overline{CE} and \overline{OE} Controlled) (1,3,4,5)

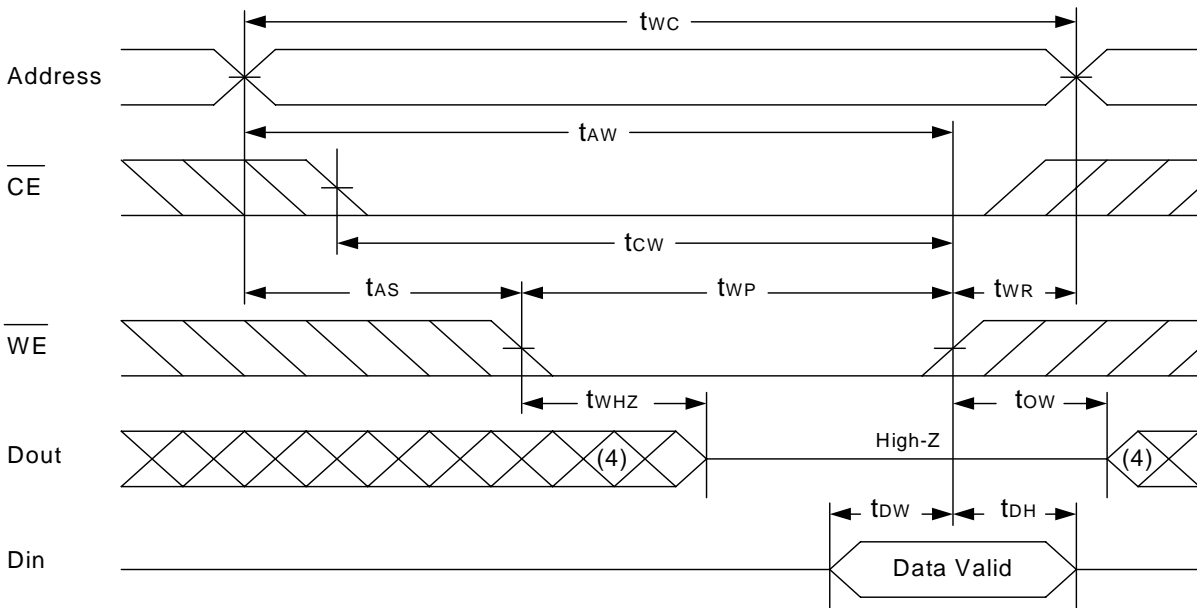


Notes :

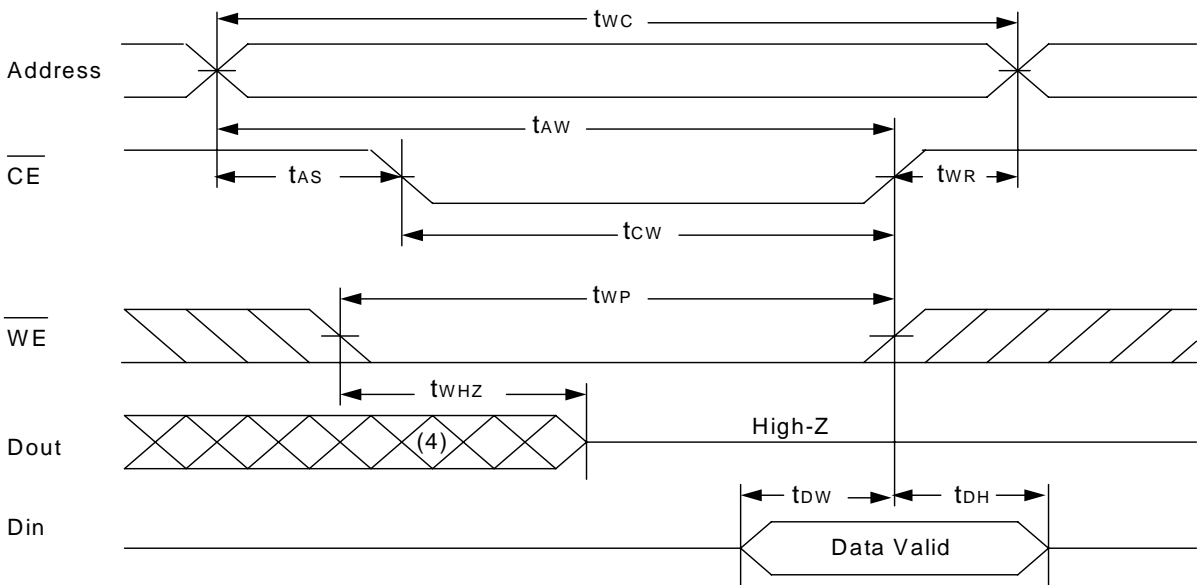
1. \overline{WE} is high for read cycle.
2. Device is continuously selected \overline{OE} =low, \overline{CE} =low.
3. Address must be valid prior to or coincident with \overline{CE} =low,; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L=5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (\overline{WE} Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (\overline{CE} Controlled) (1,2,5,6)





Notes :

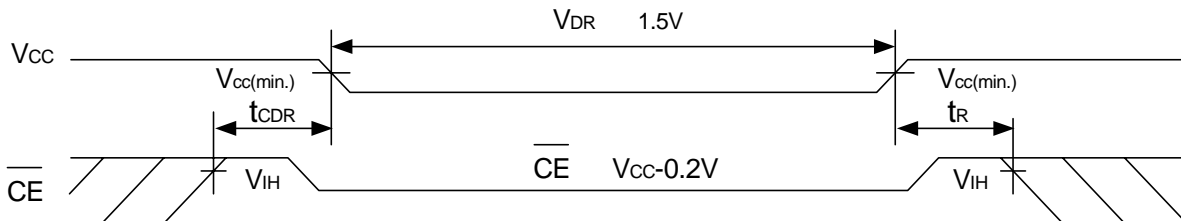
- 1. \overline{WE} , \overline{CE} must be high during all address transitions.
- 2. A write occurs during the overlap of a low \overline{CE} , low \overline{WE} .
- 3. During a \overline{WE} controlled write cycle with \overline{OE} low, t_{WP} must be greater than $t_{WHZ}+t_{bW}$ to allow the drivers to turn off and data to be placed on the bus.
- 4. During this period, I/O pins are in the output state, and input signals must not be applied.
- 5. If the \overline{CE} low transition occurs simultaneously with or after \overline{WE} low transition, the outputs remain in a high impedance state.
- 6. t_{bW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

DATA RETENTION CHARACTERISTICS ($T_A = 0$ to 70 / -20 to 80 (E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	\overline{CE} $V_{CC}-0.2V$	1.5	-	3.6	V
Data Retention Current	I_{DR}	$V_{CC}=1.5V$ \overline{CE} $V_{CC}-0.2V$	- L	1	50	μA
			- LL	0.5	20	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ms
Recovery Time	t_R		5	-	-	ms

DATA RETENTION WAVEFORM

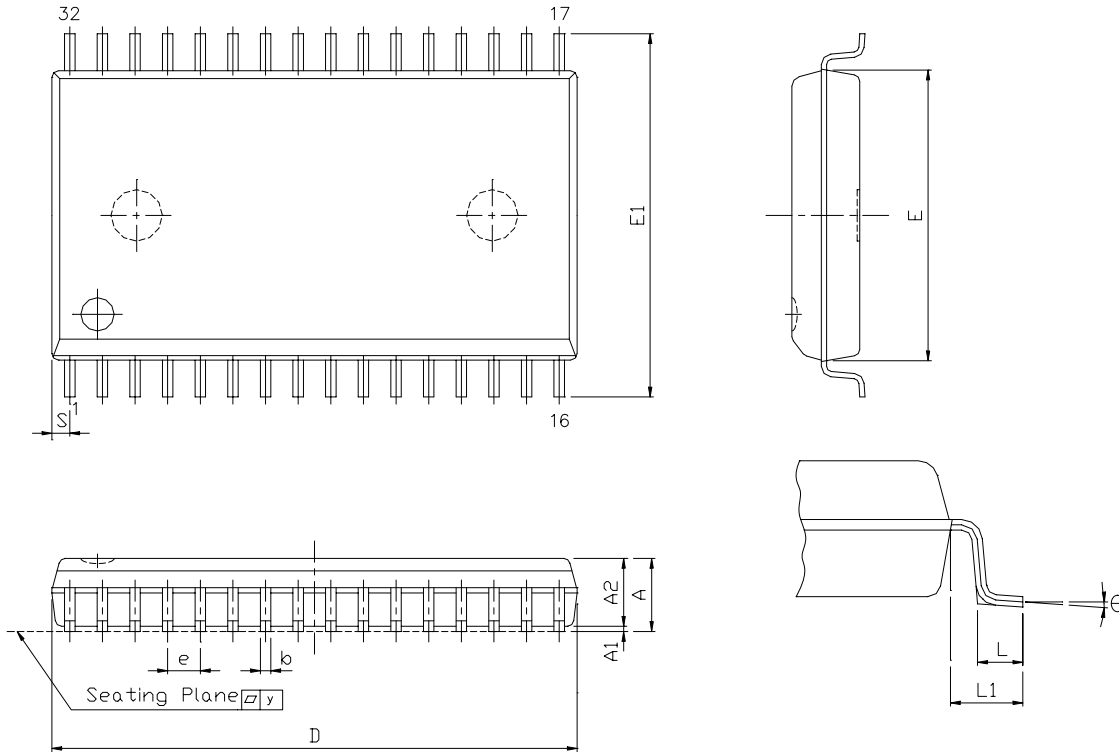
Low Vcc Data Retention Waveform (\overline{CE} controlled)





PACKAGE OUTLINE DIMENSION

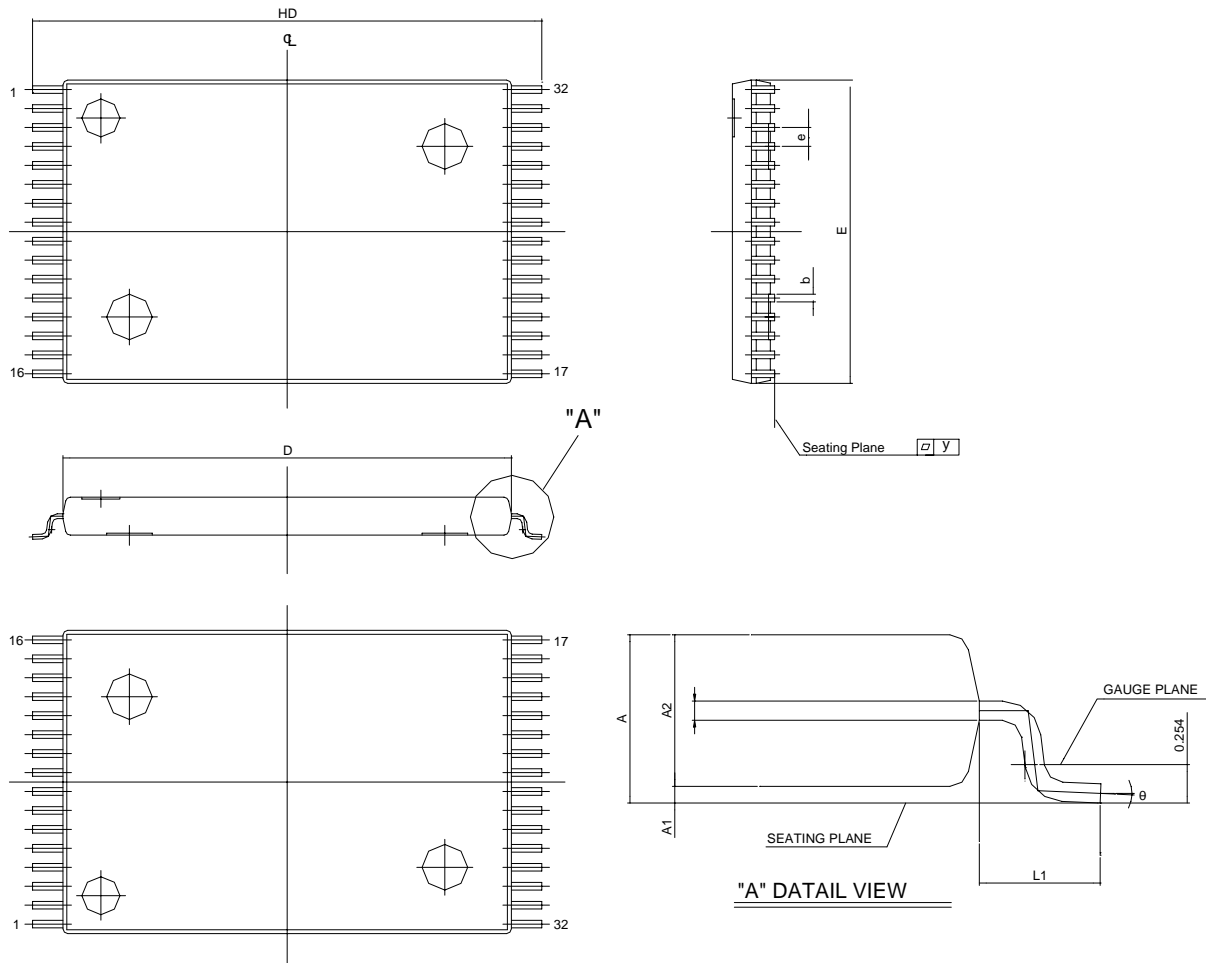
32-pin 450 mil SOP Package Outline Dimension



SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.118 (MAX)	2.997 (MAX)
A1		0.004 (MIN)	0.102 (MIN)
A2		0.111 (MAX)	2.82 (MAX)
b		0.016 (TYP)	0.406 (TYP)
D		0.817 (MAX)	20.75 (MAX)
E		0.445 ±0.005	11.303 ±0.127
E1		0.555 ±0.012	14.097 ±0.305
e		0.050 (TYP)	1.270 (TYP)
L		0.0347 ±0.008	0.881 ±0.203
L1		0.055 ±0.008	1.397 ±0.203
S		0.026 (MAX)	0.660 (MAX)
y		0.004 (MAX)	0.101 (MAX)
		0° ~10°	0° ~10°



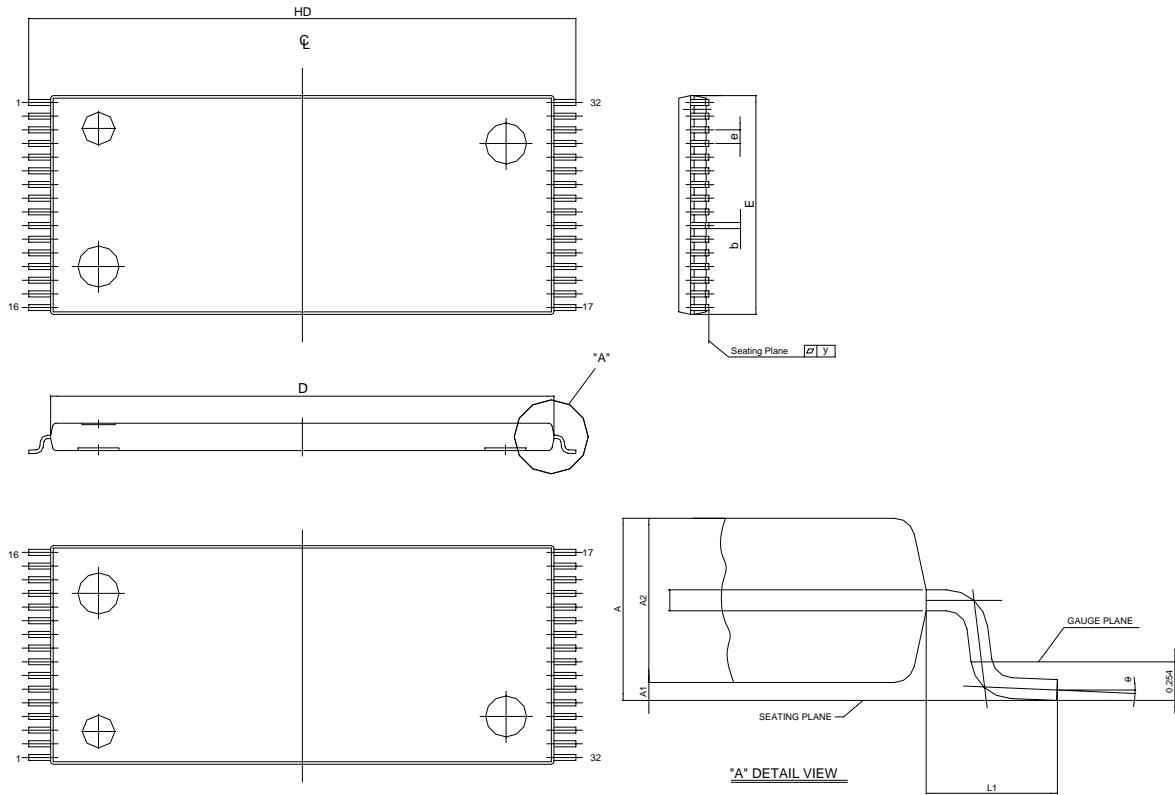
32-pin 8mm x 13.4mm STSOP Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 ±0.001	0.200 ±0.025
D	0.465 ±0.004	11.800 ±0.100
E	0.315 ±0.004	8.000 ±0.100
e	0.020 (TYP)	0.50 (TYP)
HD	0.528 ±0.008	13.40 ±0.20.
L1	0.0315 ±0.004	0.80 ±0.10
y	0.003 (MAX)	0.076 (MAX)
	0° 5°	0° 5°



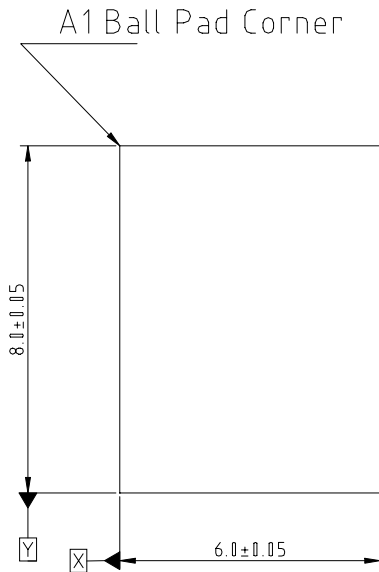
32-pin 8mm x 20mm TSOP- Package Outline Dimension



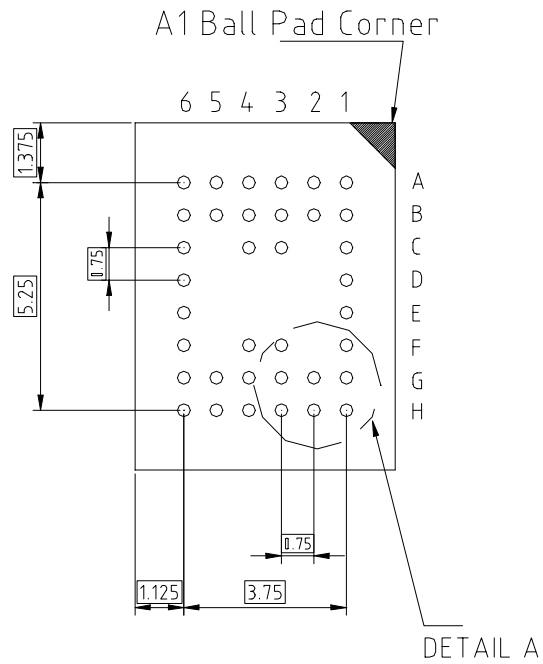
SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
D	0.724 ±0.004	18.40 ±0.10
E	0.315 ±0.004	8.00 ±0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L1	0.0315 ±0.004	0.80 ±0.10
y	0.003 (MAX)	0.076 (MAX)
	0° 5°	0° 5°



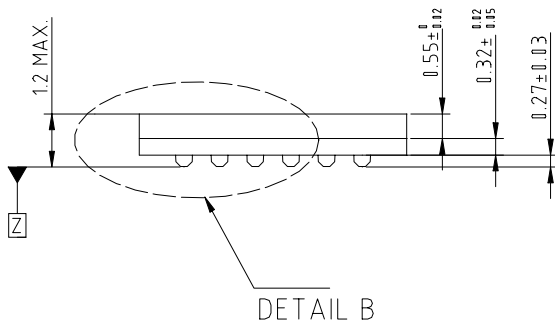
36-pin 6mm x 8mm TFBGA Package Outline Dimension



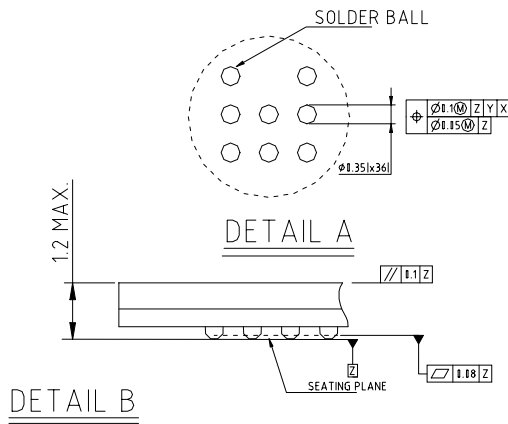
TOP VIEW | DIE VIEW |



BOTTOM VIEW | BALL SIDE |



SIDE VIEW



**ORDERING INFORMATION****COMMERCIAL TEMPERATURE**

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μ A) typ.	PACKAGE
UT62L5128SC-55L	55	20	32 PIN SOP
UT62L5128SC-55LL	55	2	32 PIN SOP
UT62L5128SC-70L	70	20	32 PIN SOP
UT62L5128SC-70LL	70	2	32 PIN SOP
UT62L5128LC-55L	55	20	32 PIN TSOP-
UT62L5128LC-55LL	55	2	32 PIN TSOP-
UT62L5128LC-70L	70	20	32 PIN TSOP-
UT62L5128LC-70LL	70	2	32 PIN TSOP-
UT62L5128LS-55L	55	20	32 PIN STSOP
UT62L5128LS-55LL	55	2	32 PIN STSOP
UT62L5128LS-70L	70	20	32 PIN STSOP
UT62L5128LS-70LL	70	2	32 PIN STSOP
UT62L5128BS-55L	55	20	36 PIN TFBGA
UT62L5128BS-55LL	55	2	36 PIN TFBGA
UT62L5128BS-70L	70	20	36 PIN TFBGA
UT62L5128BS-70LL	70	2	36 PIN TFBGA

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μ A) typ.	PACKAGE
UT62L5128SC-55LE	55	20	32 PIN SOP
UT62L5128SC-55LLE	55	2	32 PIN SOP
UT62L5128SC-70LE	70	20	32 PIN SOP
UT62L5128SC-70LLE	70	2	32 PIN SOP
UT62L5128LC-55LE	55	20	32 PIN TSOP-
UT62L5128LC-55LLE	55	2	32 PIN TSOP-
UT62L5128LC-70LE	70	20	32 PIN TSOP-
UT62L5128LC-70LLE	70	2	32 PIN TSOP-
UT62L5128LS-55LE	55	20	32 PIN STSOP
UT62L5128LS-55LLE	55	2	32 PIN STSOP
UT62L5128LS-70LE	70	20	32 PIN STSOP
UT62L5128LS-70LLE	70	2	32 PIN STSOP
UT62L5128BS-55LE	55	20	36 PIN TFBGA
UT62L5128BS-55LLE	55	2	36 PIN TFBGA
UT62L5128BS-70LE	70	20	36 PIN TFBGA
UT62L5128BS-70LLE	70	2	36 PIN TFBGA

**ORDERING INFORMATION (for lead free product)****COMMERCIAL TEMPERATURE**

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μ A) typ.	PACKAGE
UT62L5128SCL-55L	55	20	32 PIN SOP
UT62L5128SCL-55LL	55	2	32 PIN SOP
UT62L5128SCL-70L	70	20	32 PIN SOP
UT62L5128SCL-70LL	70	2	32 PIN SOP
UT62L5128LCL-55L	55	20	32 PIN TSOP-
UT62L5128LCL-55LL	55	2	32 PIN TSOP-
UT62L5128LCL-70L	70	20	32 PIN TSOP-
UT62L5128LCL-70LL	70	2	32 PIN TSOP-
UT62L5128LSL-55L	55	20	32 PIN STSOP
UT62L5128LSL-55LL	55	2	32 PIN STSOP
UT62L5128LSL-70L	70	20	32 PIN STSOP
UT62L5128LSL-70LL	70	2	32 PIN STSOP
UT62L5128BSL-55L	55	20	36 PIN TFBGA
UT62L5128BSL-55LL	55	2	36 PIN TFBGA
UT62L5128BSL-70L	70	20	36 PIN TFBGA
UT62L5128BSL-70LL	70	2	36 PIN TFBGA

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μ A) typ.	PACKAGE
UT62L5128SCL-55LE	55	20	32 PIN SOP
UT62L5128SCL-55LLE	55	2	32 PIN SOP
UT62L5128SCL-70LE	70	20	32 PIN SOP
UT62L5128SCL-70LLE	70	2	32 PIN SOP
UT62L5128LCL-55LE	55	20	32 PIN TSOP-
UT62L5128LCL-55LLE	55	2	32 PIN TSOP-
UT62L5128LCL-70LE	70	20	32 PIN TSOP-
UT62L5128LCL-70LLE	70	2	32 PIN TSOP-
UT62L5128LSL-55LE	55	20	32 PIN STSOP
UT62L5128LSL-55LLE	55	2	32 PIN STSOP
UT62L5128LSL-70LE	70	20	32 PIN STSOP
UT62L5128LSL-70LLE	70	2	32 PIN STSOP
UT62L5128BSL-55LE	55	20	36 PIN TFBGA
UT62L5128BSL-55LLE	55	2	36 PIN TFBGA
UT62L5128BSL-70LE	70	20	36 PIN TFBGA
UT62L5128BSL-70LLE	70	2	36 PIN TFBGA



Rev. 1.4

UTRON

UT62L5128
512K X 8 BIT LOW POWER CMOS SRAM

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