

# IC62LV2568L IC62LV2568LL



## 256K x 8 LOW POWER and LOW V<sub>CC</sub> CMOS STATIC RAM

### FEATURES

- Access times of 55, 70, 100 ns
- Low active power: 126 mW (max, L, LL)
- Low standby power: 36  $\mu$ W (max, L) and 7.2  $\mu$ W (max, LL) CMOS standby
- Low data retention voltage: 1.5V (min.)
- Available in Low Power (-L) and Ultra-Low Power (-LL)
- Output Enable ( $\overline{OE}$ ) and two Chip Enable
- TTL compatible inputs and outputs
- Single 2.7V-3.6V power supply
- Available in the 32-pin 8x20mm TSOP-1, 32-pin 8x13.4mm TSOP-1 and 48-pin 6\*8mm TF-BGA

### DESCRIPTION

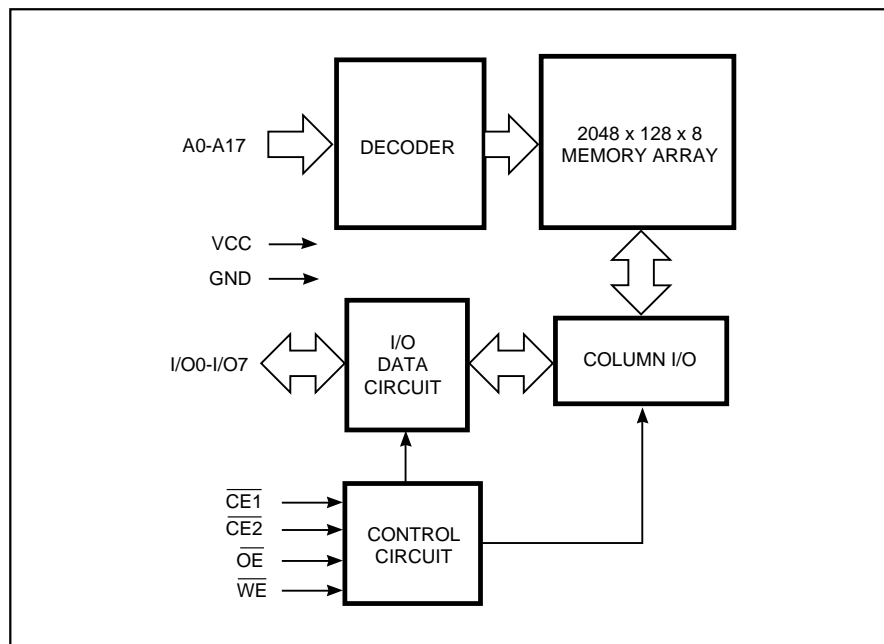
The *ICSI* IC62LV2568L and IC62LV2568LL are low power and low V<sub>CC</sub>, 262,144-bit words by 8 bits CMOS static RAMs. They are fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When  $\overline{CE1}$  is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs,  $\overline{CE1}$  and CE2. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

The IC62LV2568L and IC62LV2568LL are available in 32-pin 8\*20mm TSOP-1, 8\*13.4mm TSOP-1 and 48-pin 6\*8mm TF-BGA.

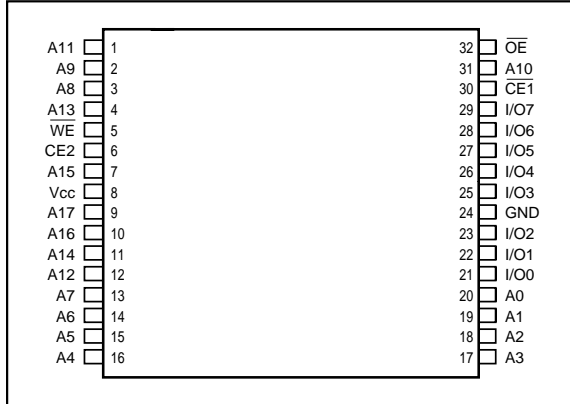
### FUNCTIONAL BLOCK DIAGRAM



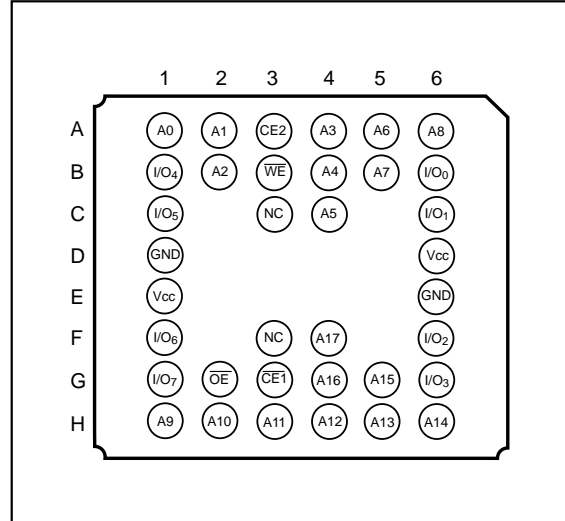
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PIN CONFIGURATIONS

32-Pin 8\*20mm TSOP-1, 8\*13.4mm STSOP-1



48-Pin 6\*8mm TF-BGA



PIN DESCRIPTIONS

A0-A17	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Data Input/Output
NC	No Connection
Vcc	Power
GND	Ground

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.7V - 3.6V
Industrial	-40°C to +85°C	2.7V - 3.6V

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	X	High-Z	IsB1, IsB2
(Power-down)	X	X	L	X	High-Z	IsB1, IsB2
Output Disabled	H	L	H	H	High-Z	Icc
Read	H	L	H	L	DOUT	Icc
Write	L	L	H	X	DIN	Icc

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>CC</sub>	V <sub>CC</sub> related to GND	-0.3 to +4.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.7	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE<sup>(1)</sup>

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.2	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub> <sup>(1)</sup>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.4	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>	-1	1	μA

Notes:

1. V<sub>IL</sub> = -2.0V for pulse width less than 10 ns.



IC62LV2568L POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		-55		-70		-100		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	–	40	–	30	–	20	mA
			Ind.	–	45	–	35	–	25	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , $\overline{CE1} \geq V_{IH}$ or CE2 ≤ V <sub>IL</sub> , f = 0	Com.	–	0.4	–	0.4	–	0.4	mA
			Ind.	–	1.0	–	1.0	–	1.0	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., f = 0 $\overline{CE1} \geq V_{CC} - 0.2V$ , CE2 ≤ 0.2V, or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2V, V <sub>IN</sub> ≤ 0.2V	Com.	–	35	–	35	–	35	μA
			Ind.	–	50	–	50	–	50	

Note:

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

IC62LV2568LL POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		-55		-70		-100		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	–	40	–	30	–	20	mA
			Ind.	–	45	–	35	–	25	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , $\overline{CE1} \geq V_{IH}$ or CE2 ≤ V <sub>IL</sub> , f = 0	Com.	–	0.4	–	0.4	–	0.4	mA
			Ind.	–	1.0	–	1.0	–	1.0	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., f = 0 $\overline{CE} \geq V_{CC} - 0.2V$ , CE2 ≤ 0.2V, or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2V, V <sub>IN</sub> ≤ 0.2V	Com.	–	10	–	10	–	10	μA
			Ind.	–	15	–	15	–	15	

Note:

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	-55		-70		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	100	—	ns
t <sub>AA</sub>	Address Access Time	—	55	—	70	—	100	ns
t <sub>OH</sub>	Output Hold Time	10	—	10	—	15	—	ns
t <sub>ACE1</sub>	$\overline{CE1}$ Access Time	—	55	—	70	—	100	ns
t <sub>ACE2</sub>	CE2 Access Time	—	55	—	70	—	100	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	30	—	35	—	50	ns
t <sub>LZOE</sub> <sup>(2)</sup>	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t <sub>HZOE</sub> <sup>(2)</sup>	$\overline{OE}$ to High-Z Output	—	20	0	25	0	30	ns
t <sub>LZCE1</sub> <sup>(2)</sup>	$\overline{CE1}$ to Low-Z Output	10	—	10	—	10	—	ns
t <sub>LZCE2</sub> <sup>(2)</sup>	CE2 to Low-Z Output	10	—	10	—	10	—	ns
t <sub>HZCE</sub> <sup>(2)</sup>	$\overline{CE1}$ or CE2 to Low-Z Output	0	20	0	25	0	30	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

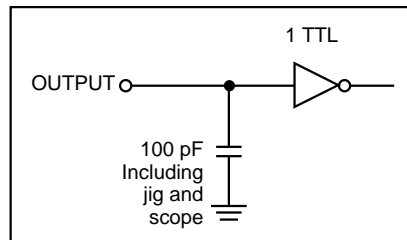


Figure 1

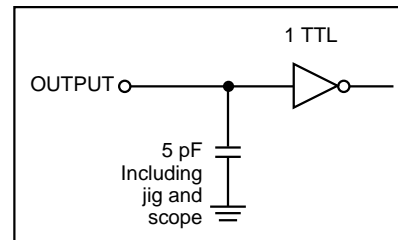
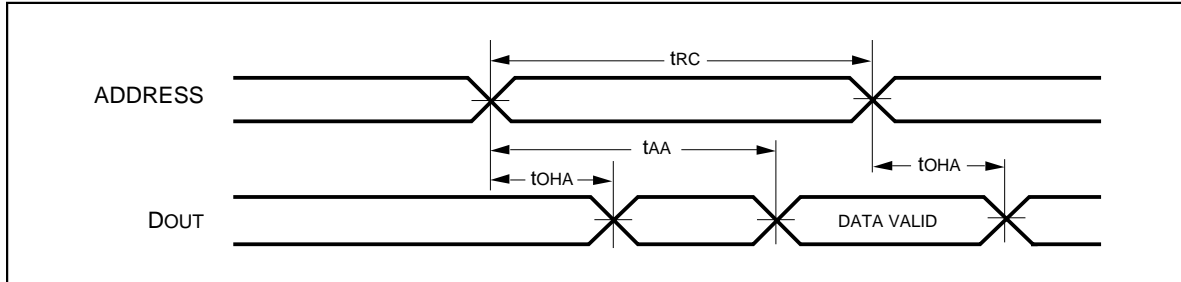
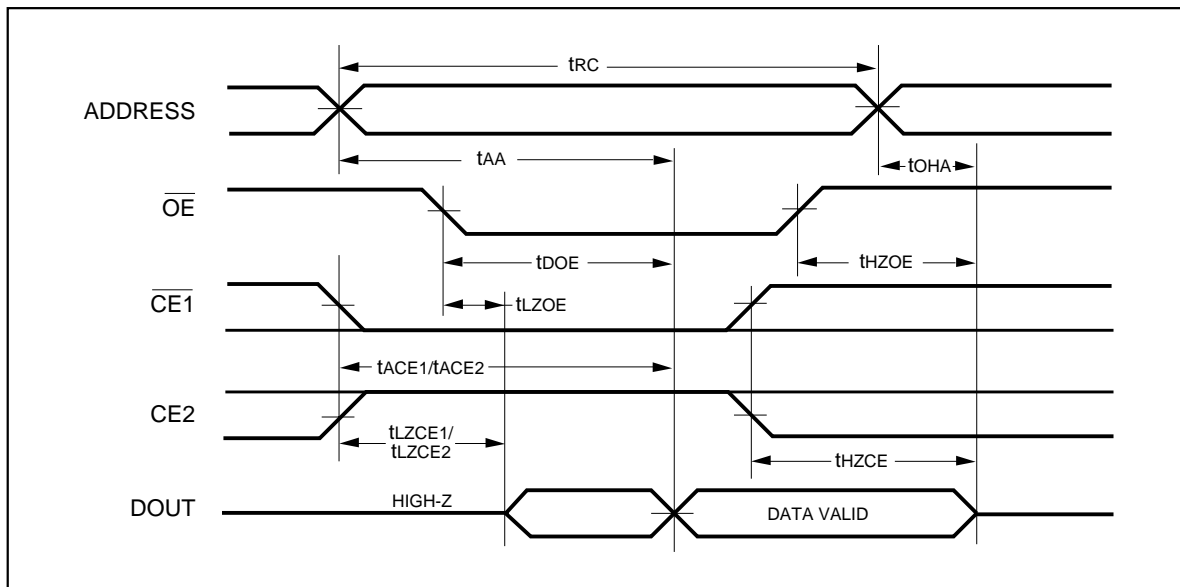


Figure 2

AC TEST LOADS  
READ CYCLE NO.1<sup>(1,2)</sup>



AC WAVEFORMS  
READ CYCLE NO. 2<sup>(1,3)</sup>



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE1} = V_{IL}$ ,  $CE2 = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE1}$  LOW and CE2 HIGH transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range, Standard and Low Power)

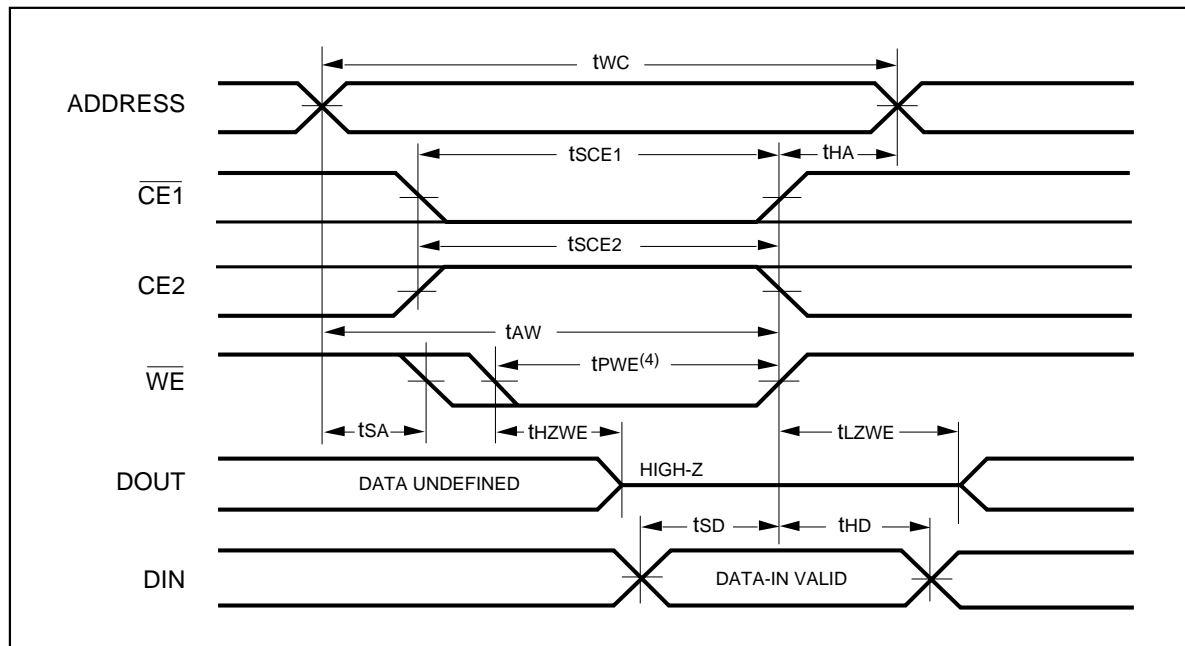
Symbol	Parameter	-55		-70		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>wc</sub>	Write Cycle Time	55	—	70	—	100	—	ns
t <sub>sce1</sub>	$\overline{CE1}$ to Write End	45	—	65	—	80	—	ns
t <sub>sce2</sub>	CE2 to Write End	45	—	65	—	80	—	ns
t <sub>aw</sub>	Address Setup Time to Write End	45	—	65	—	80	—	ns
t <sub>ha</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>sa</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>pwe</sub> <sup>(4)</sup>	$\overline{WE}$ Pulse Width	50	—	55	—	70	—	ns
t <sub>sd</sub>	Data Setup to Write End	25	—	30	—	40	—	ns
t <sub>hd</sub>	Data Hold from Write End	0	—	0	—	0	—	ns
t <sub>hzwe</sub> <sup>(3)</sup>	$\overline{WE}$ LOW to High-Z Output	—	25	—	25	—	30	ns
t <sub>lzwe</sub> <sup>(3)</sup>	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:

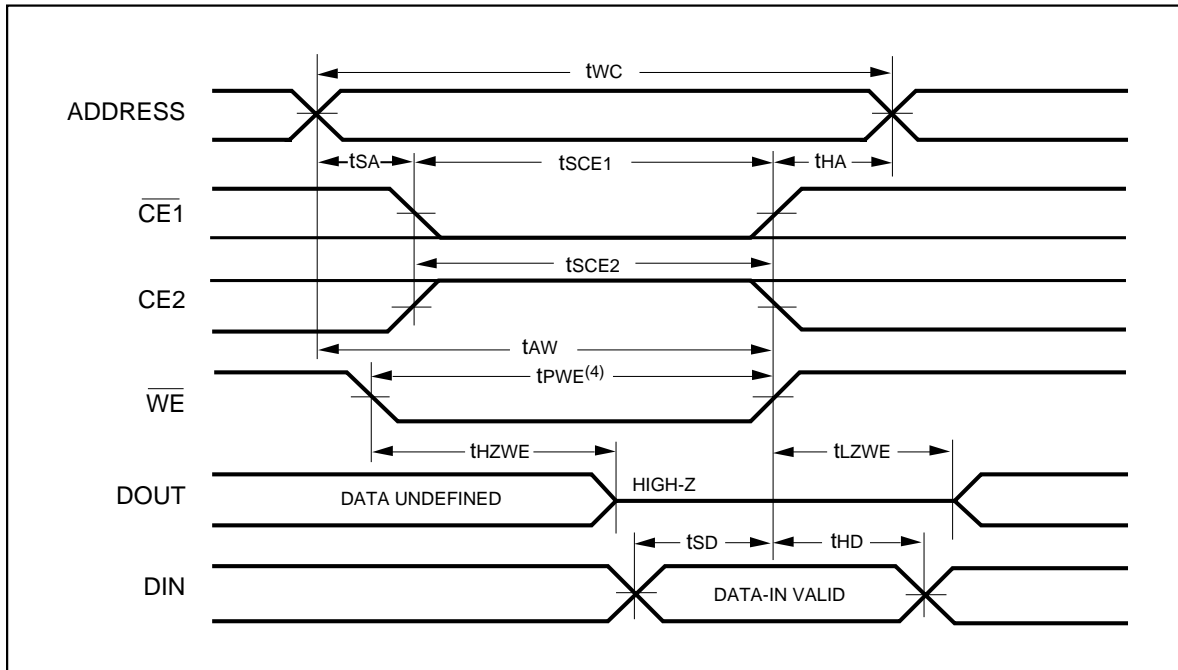
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE1}$  LOW, CE2 HIGH and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with  $\overline{OE}$  HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ( $\overline{WE}$  Controlled)<sup>(1,2)</sup>



WRITE CYCLE NO. 2 ( $\overline{CE1}$ , CE2 Controlled)<sup>(1,2)</sup>



Notes:

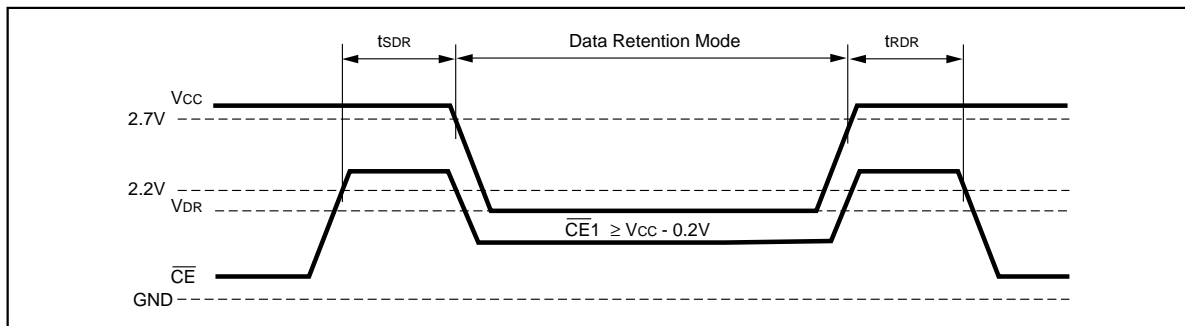
1. The internal write time is defined by the overlap of  $\overline{CE1}$  LOW, CE2 HIGH and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the HIGH-z state if  $\overline{OE} = V_{IH}$ .



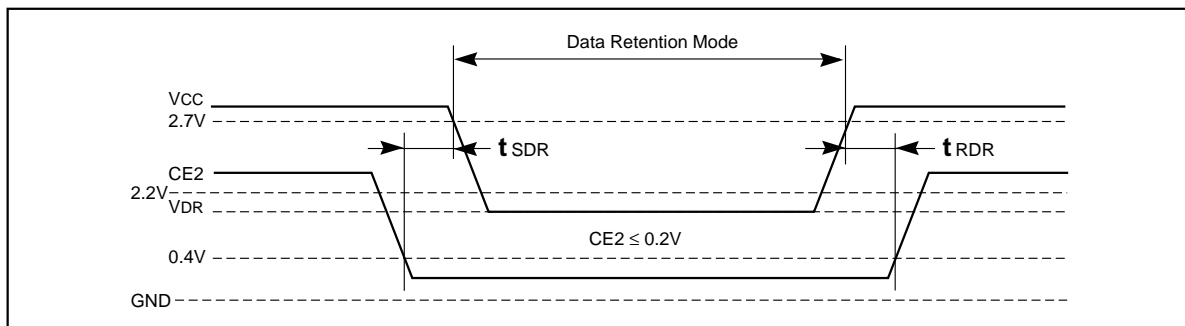
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit	
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	See Data Retention Waveform	1.5	3.6	V	
I <sub>DR</sub>	Data Retention Current	V <sub>CC</sub> = 2.0V, $\overline{CE1} \geq V_{CC} - 0.2V$	Com. (-L)	—	20	μA
			Com. (-LL)	—	5	μA
			Ind. (-L)	—	25	μA
			Ind. (-LL)	—	7	μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0	—	ns	
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	ns	

DATA RETENTION WAVEFORM ( $\overline{CE1}$  Controlled)



DATA RETENTION WAVEFORM (CE2 Controlled)





**ORDERING INFORMATION**

**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
55	IC62LV2568L-55T	8*20mm TSOP-1
	IC62LV2568L-55H	8*13.4mm TSOP-1
	IC62LV2568L-55B	6*8mm TF-BGA
70	IC62LV2568L-70T	8*20mm TSOP-1
	IC62LV2568L-70H	8*13.4mm TSOP-1
	IC62LV2568L-70B	6*8mm TF-BGA
100	IC62LV2568L-100T	8*20mm TSOP-1
	IC62LV2568L-100H	8*13.4mm TSOP-1
	IC62LV2568L-100B	6*8mm TF-BGA

**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
55	IC62LV2568L-55TI	8*20mm TSOP-1
	IC62LV2568L-55HI	8*13.4mm TSOP-1
	IC62LV2568L-55BI	6*8mm TF-BGA
70	IC62LV2568L-70TI	8*20mm TSOP-1
	IC62LV2568L-70HI	8*13.4mm TSOP-1
	IC62LV2568L-70BI	6*8mm TF-BGA
100	IC62LV2568L-100TI	8*20mm TSOP-1
	IC62LV2568L-100HI	8*13.4mm TSOP-1
	IC62LV2568L-100BI	6*8mm TF-BGA

**ORDERING INFORMATION**

**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
55	IC62LV2568LL-55T	8*20mm TSOP-1
	IC62LV2568LL-55H	8*13.4mm TSOP-1
	IC62LV2568LL-55B	6*8mm TF-BGA
70	IC62LV2568LL-70T	8*20mm TSOP-1
	IC62LV2568LL-70H	8*13.4mm TSOP-1
	IC62LV2568LL-70B	6*8mm TF-BGA
100	IC62LV2568LL-100T	8*20mm TSOP-1
	IC62LV2568LL-100H	8*13.4mm TSOP-1
	IC62LV2568LL-100B	6*8mm TF-BGA

**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
55	IC62LV2568LL-55TI	8*20mm TSOP-1
	IC62LV2568LL-55HI	8*13.4mm TSOP-1
	IC62LV2568LL-55BI	6*8mm TF-BGA
70	IC62LV2568LL-70TI	8*20mm TSOP-1
	IC62LV2568LL-70HI	8*13.4mm TSOP-1
	IC62LV2568LL-70BI	6*8mm TF-BGA
100	IC62LV2568LL-100TI	8*20mm TSOP-1
	IC62LV2568LL-100HI	8*13.4mm TSOP-1
	IC62LV2568LL-100BI	6*8mm TF-BGA



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