PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M416160CXX-5,-5S	50	13	25	13	90	540
M5M416160CXX-6,-6S	60	15	30	15	110	430
M5M416160CXX-7,-7S	70	20	35	20	130	385

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ---------------------------- CMOS Input level
- Low operating power dissipation
  M5M416160Cxx-5,-5S -------------------- 660.0mW (Max)
  M5M416160Cxx-6,-6S -------------------- 525.0mW (Max)
  M5M416160Cxx-7,-7S -------------------- 470.0mW (Max)
- Fast-page mode , Read-modify-write,$\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A0~A11)
 * : Applicable to self refresh version (M5M416160CJ,TP-5S,-6S,
    -7S : option) only

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A0~A11	Address inputs
DQ1~DQ16	Data inputs / outputs
$\overline{RAS}$	Row address strobe Input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5.0V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)
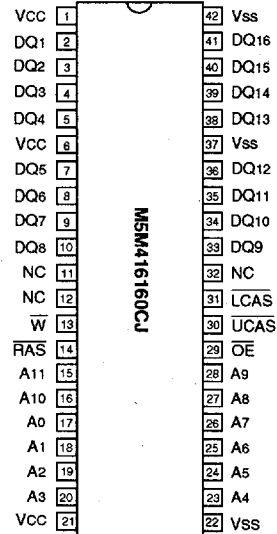
Outline 42P0N-A (400mil SOJ)
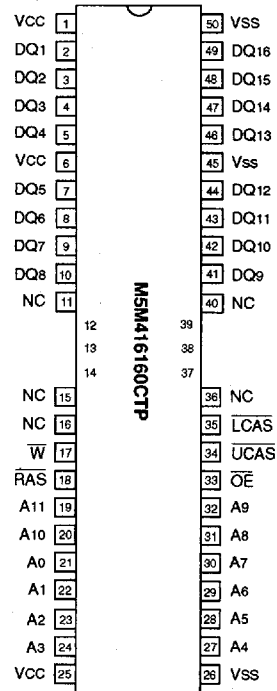
Outline 50P3G-F (400mil TSOP Normal Bend)

NC : NO CONNECTION

6249825 0028802 TTT

MITSUBISHI ELECTRIC

PRELIMINARY

Notice: This is not a final specification
Some parametric inputs are subject to change

FUNCTION

The M5M416160CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open
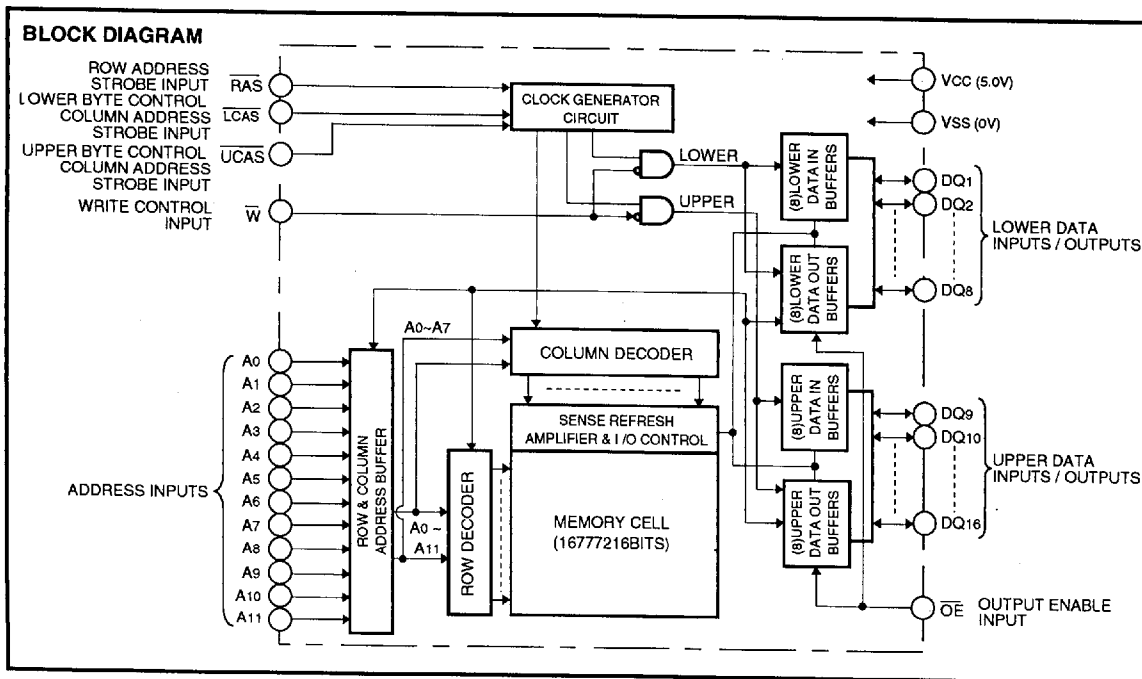
BLOCK DIAGRAM

MITSUBISHI ELECTRIC

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-1\sim7$	V
V_I	Input voltage	With respect to V_{SS}	$-1\sim7$	V
V_O	Output voltage		$-1\sim7$	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25 °C	1000	mW
T_{opr}	Operating temperature		$0\sim70$	°C
T_{stg}	Storage temperature		$-65\sim150$	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating $0V \leq V_{OUT} \leq 5.5V$	-10		10	μA
I_I	Input current		$0V \leq V_{IN} \leq 6V$, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3,4,5)	M5M416160C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling tRC=tWC=min. output open			120	mA
		M5M416160C-6,-6S				95	
		M5M416160C-7,-7S				85	
I_{CC2}	Supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ $\geq V_{CC}$ -0.2V			1	
			output open			0.3*	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3,5)	M5M416160C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} tRC=min. output open			120	mA
		M5M416160C-6,-6S				95	
		M5M416160C-7,-7S				85	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-page-mode (Note 3,4,5)	M5M416160C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling tPC=min. output open			80	mA
		M5M416160C-6,-6S				70	
		M5M416160C-7,-7S				65	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M416160C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tRC=min. output open			120	mA
		M5M416160C-6,-6S				95	
		M5M416160C-7,-7S				85	
$I_{CC8(AV)}$ *	Average supply current from V_{CC} Extended-refresh cycle (Note 6)	M5M416160C (S)	Stand-by: $\overline{RAS}\geq V_{CC}$-0.2V $\overline{CAS}\geq V_{CC}$-0.2V or $\overline{CAS}\leq$0.2V $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}\leq$0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{W}\leq$0.2V or $\geq V_{CC}$-0.2V $\overline{OE}\leq$0.2V or $\geq V_{CC}$-0.2V A0~A11$\leq$0.2V or $\geq V_{CC}$-0.2V DQ=open, tRC=125μs, tRAS=tRASmin~1 μs			600	μA
$I_{CC9(AV)}$ *	Average supply current from V_{CC} Self-refresh cycle	M5M416160C (S)	$\overline{RAS}$=$\overline{CAS}\leq$0.2V			400	μA

Note 2: Current flowing into an IC is positive, out is negative.
　　　3: ICC1 (AV), ICC3 (AV) and ICC4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
　　　4: ICC1 (AV) and ICC4 (AV) are dependent on output loading. Specified values are obtained with the output open.
　　　5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}/\overline{UCAS}$=$V_{IH}$.

6249825 0028804 872

MITSUBISHI ELECTRIC

M5M416160CJ,TP-5,-6,-7,-5S,-6S,-7S

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V$_I$=Vss f=1MHz V$_I$=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input			-	7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Columu address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12)	0	13	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	15	ns

Note 6: An initial pause of 500 µs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-5mA) / VOL=0.4V(IOL=4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.4V(VOH) and 0.4V(VOL).

8: Assumes that tRCD ≧ tRCD(max) and tASC ≧ tASC(max).

9: Assumes that tRCD ≦ tRCD(max) and tRAD ≦ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

10: Assumes that tRAD ≧ tRAD(max) and tASC ≦ tASC(max).

11: Assumes that tCP ≦ tCP(max) and tASC ≧ tASC(max).

12: tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (IOUT ≦ | ±10 µA |) and is not reference to VOH(min) or VOL(max).

6249825 0028805 709

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M416160CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter		Limits						Unit
			M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			64		64		64	ms
tREF∗	Refresh cycle time			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		15		ns
tT	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.

14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tT+tASC(min).

16: tRAD(max) is specified as a reference point only. If tRAD ≥ tRAD(max) and tASC ≤tASC(max), access time is controlled exclusively by tAA.

17: tASC(min) is specified as a reference point only. If tRCD ≥ tRCD(max) and tASC ≥tASC(max), access time is controlled exclusively by tCAC.

18: Either tDZC or tDZO must be satisfied.

19: Either tCDD or tODD must be satisfied.

20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 21)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

6249825 0028806 645

MITSUBISHI ELECTRIC

M5M416160CJ,TP-5,-6,-7,-5S,-6S,-7S

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	13	10000	15	10000	20	10000	ns
tCSH	CAS hold time after RAS low	50		60		70		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tWCS	Write setup time before CAS low (Note 23)	0		0		0		ns
tWCH	Write hold time after CAS low	8		10		15		ns
tCWL	CAS hold time after W low	13		15		20		ns
tRWL	RAS hold time after W low	13		15		20		ns
tWP	Write pulse width	8		10		15		ns
tDS	Data setup time before CAS low or W low	0		0		0		ns
tDH	Data hold time after CAS low or W low	10		15		15		ns
tOEH	OE hold time after W low	13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note 22)	131		155		180		ns
tRAS	RAS low pulse width	91	10000	105	10000	120	10000	ns
tCAS	CAS low pulse width	54	10000	60	10000	70	10000	ns
tCSH	CAS hold time after RAS low	91		105		120		ns
tRSH	RAS hold time after CAS low	54		60		70		ns
tRCS	Read setup time before CAS low	0		0		0		ns
tCWD	Delay time, CAS low to W low (Note 23)	36		40		45		ns
tRWD	Delay time, RAS low to W low (Note 23)	73		85		95		ns
tAWD	Delay time, address to W low (Note 23)	48		55		60		ns
tCWL	CAS hold time after W low	13		15		20		ns
tRWL	RAS hold time after W low	13		15		20		ns
tWP	Write pulse width	8		10		10		ns
tDS	Data setup time before W low	0		0		0		ns
tDH	Data hold time after W low	10		10		15		ns
tOEH	OE hold time after W low	13		15		15		ns

Note 22: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+5tT.

23: tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD(min), tAWD≧tAWD(min) and tCPWD≧tCPWD(min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time	76		85		95		ns
tRAS	RAS low pulse width for read write cycle (Note 25)	85	125000	100	125000	115	125000	ns
tCP	CAS high pulse width (Note 26)	8	12	10	15	10	15	ns
tCPRH	RAS hold time after CAS precharge	30		35		40		ns
tCPWD	Delay time, CAS precharge to W low (Note 23)	53		60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: tRAS(min) is specified as two cycles of CAS input are performed.

26: tCP(max) is specified as a reference point only.
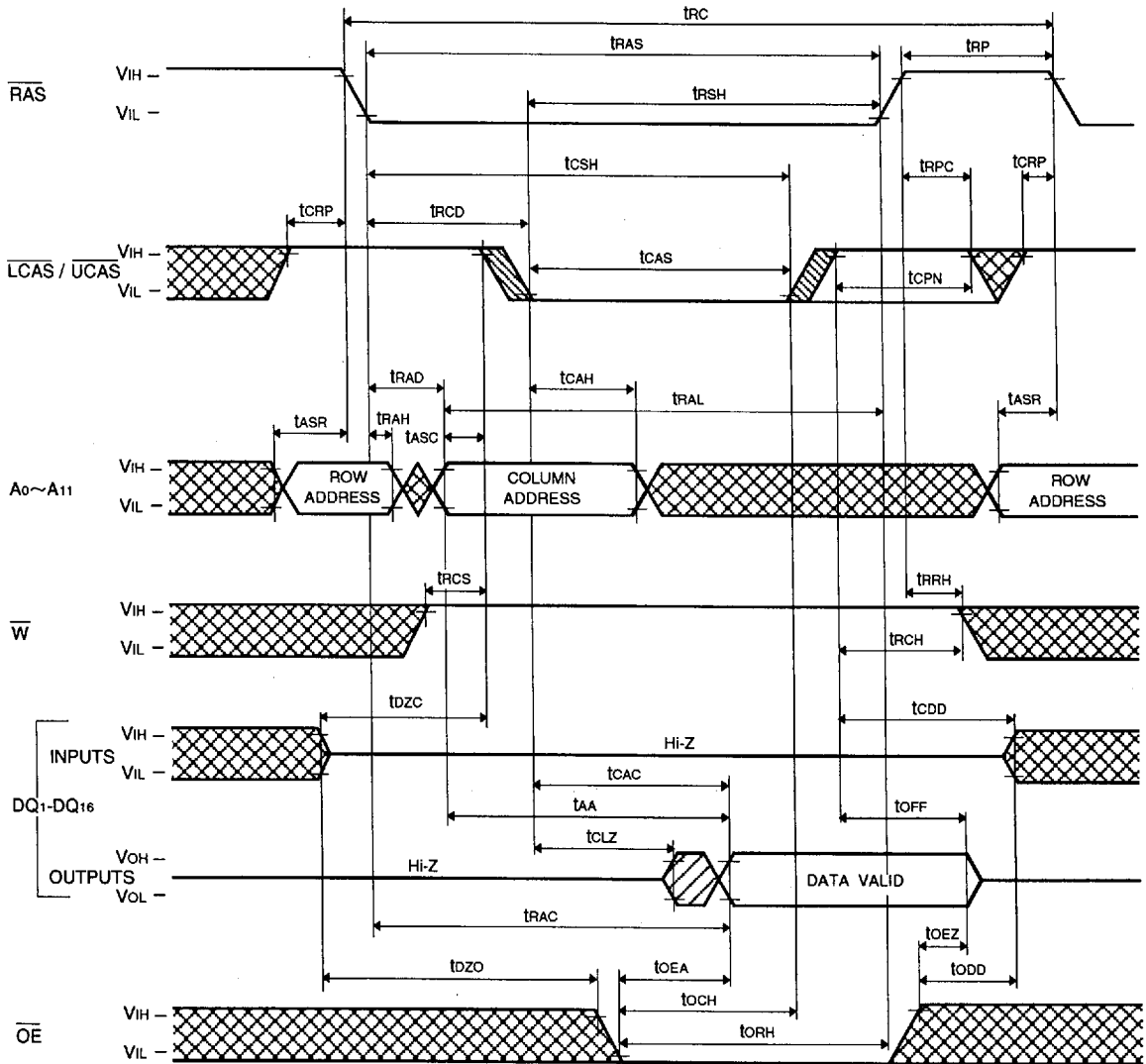
6249825 0028807 581

MITSUBISHI ELECTRIC

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

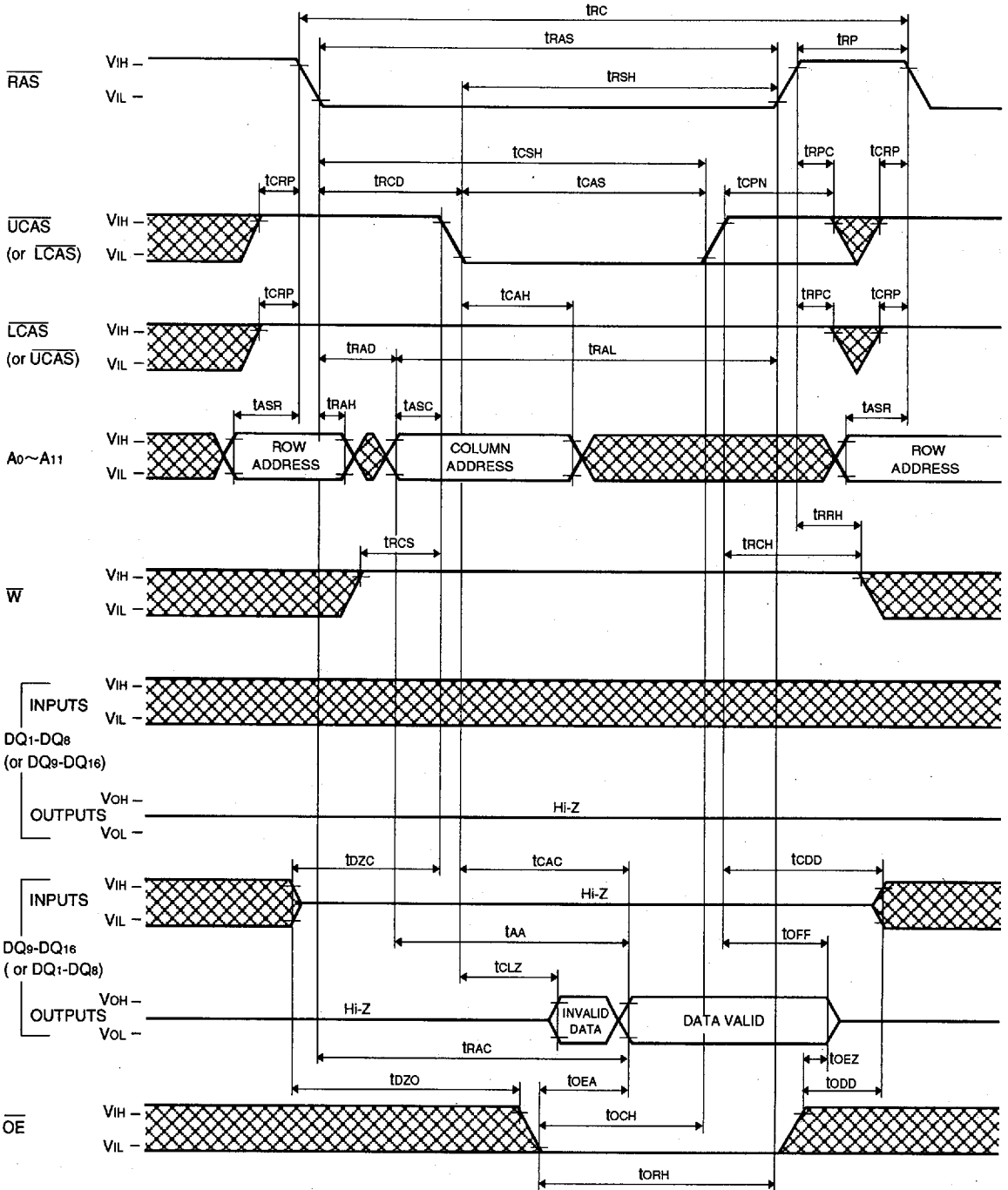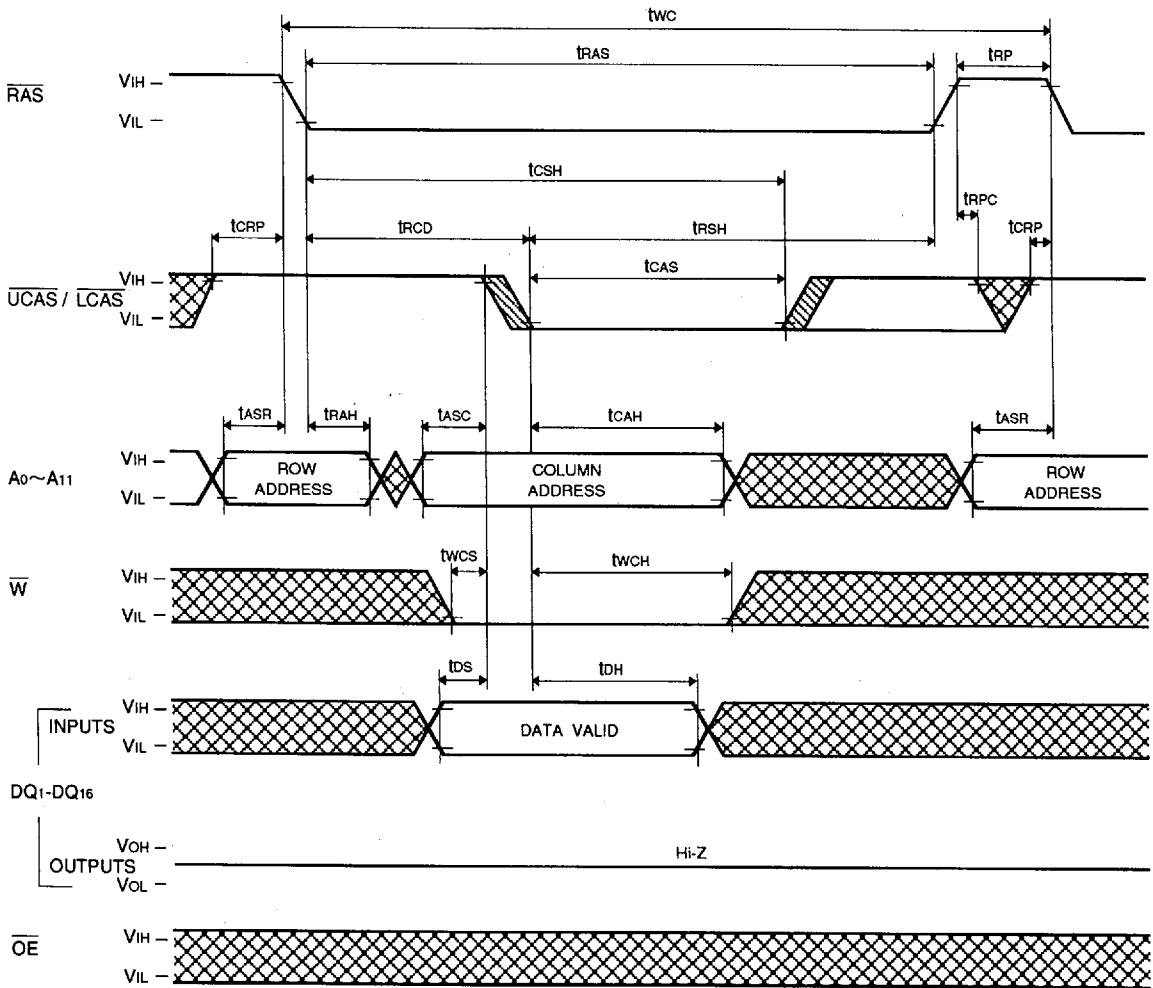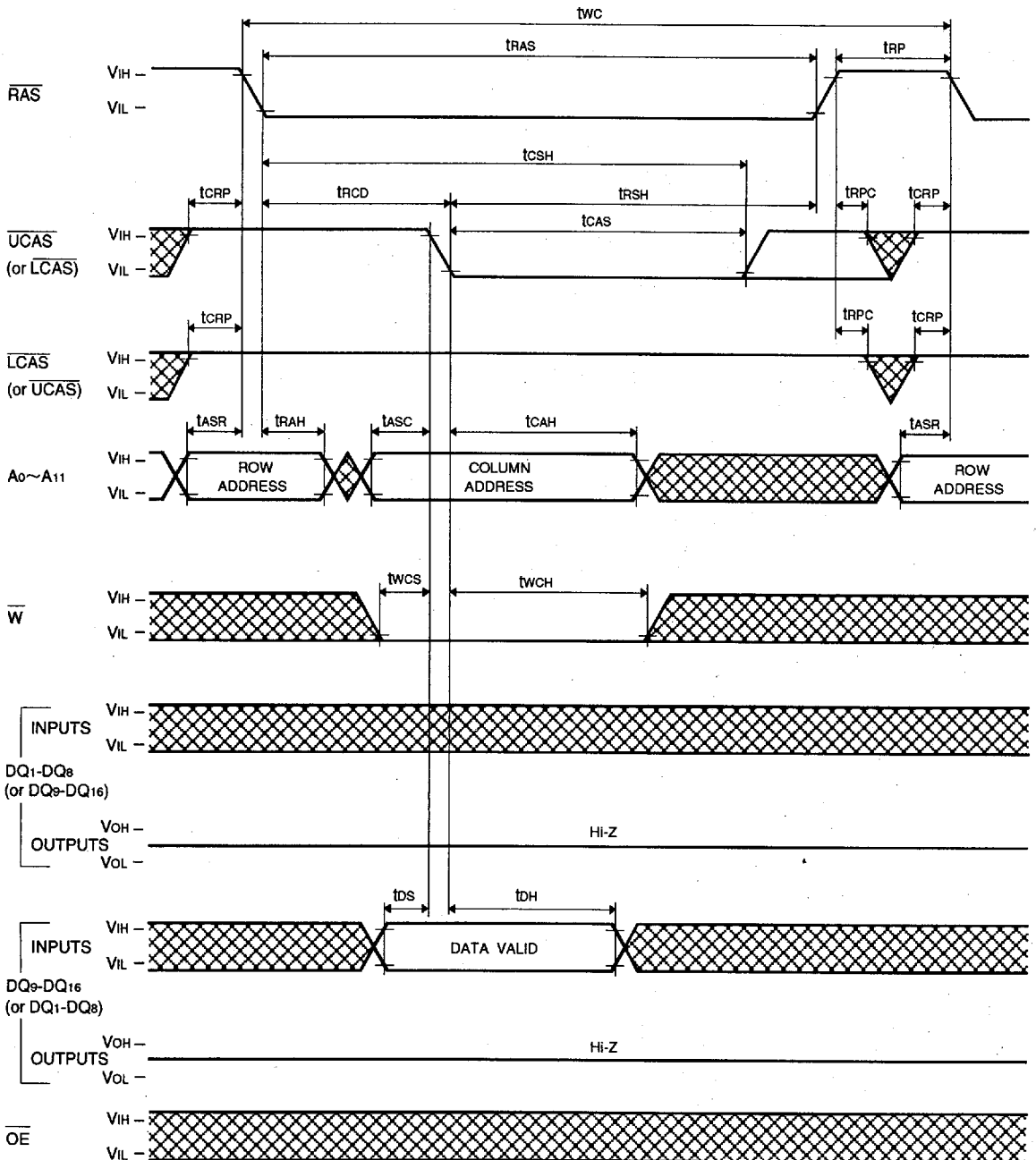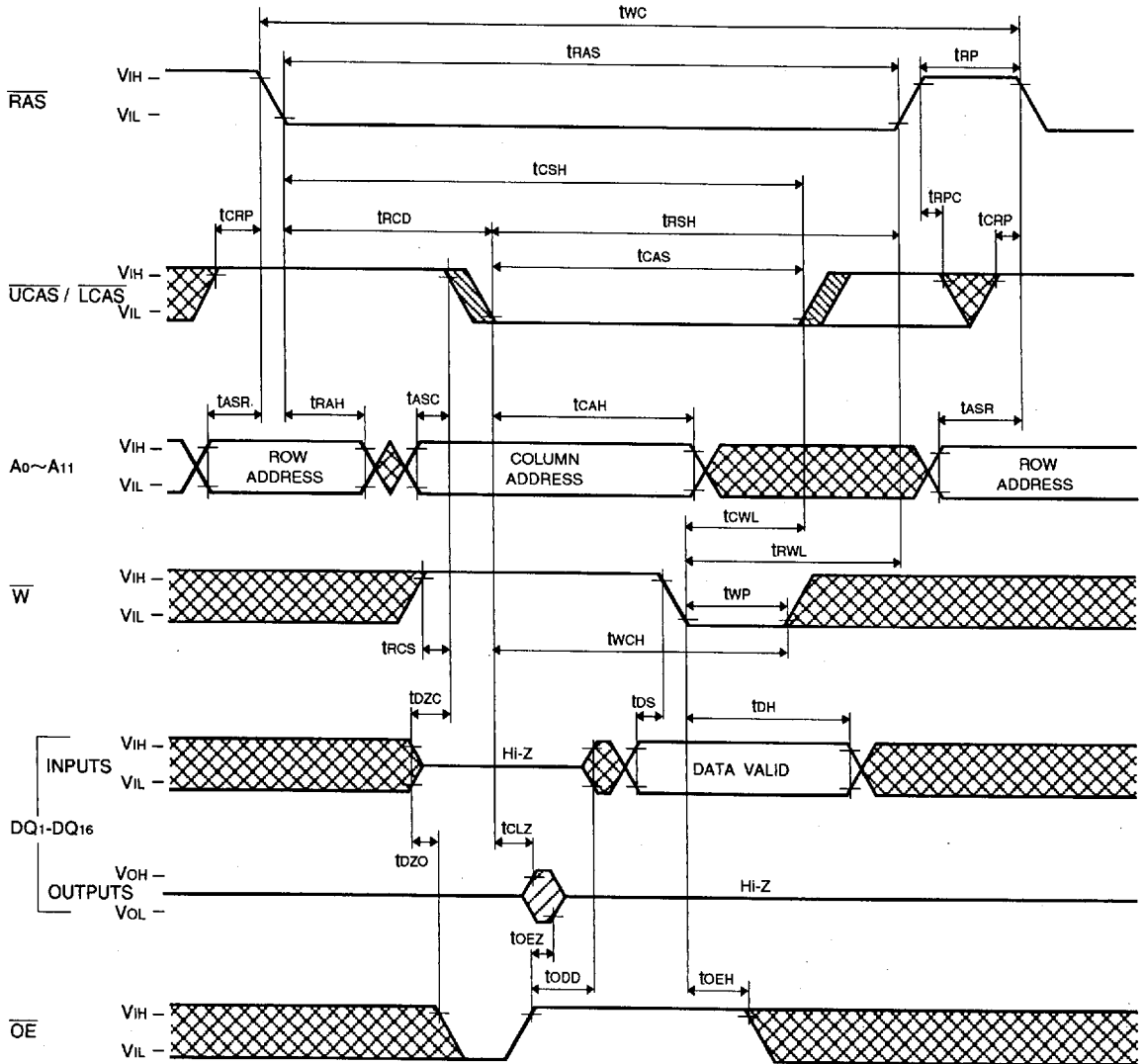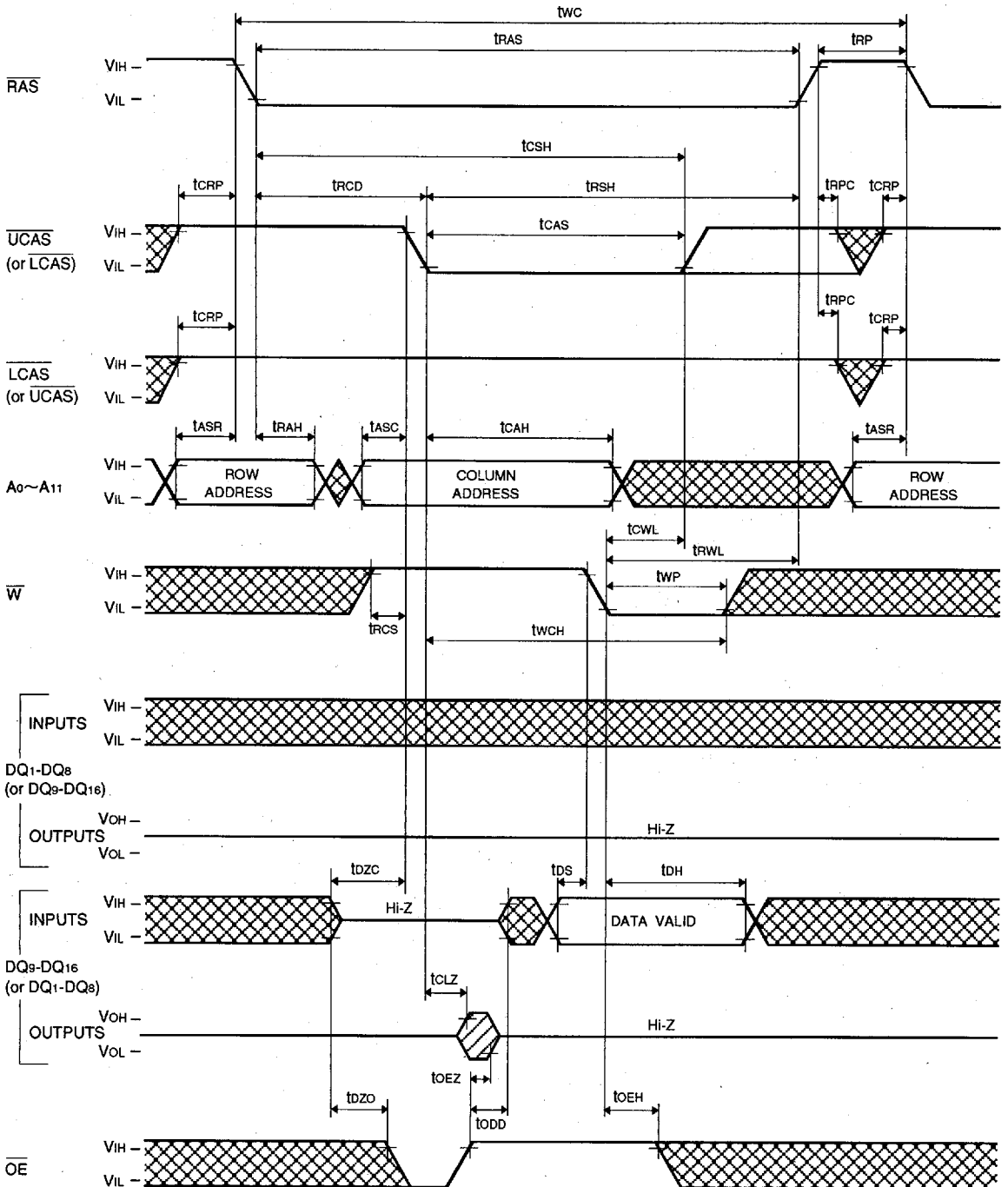### $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	M5M416160C-5,-5S		M5M416160C-6,-6S		M5M416160C-7,-7S		Unit
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/ -6S/ -7S. The other characteristics and requirements than the below are same as normal devices.

TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5.0V±10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	M5M416160C-5S		M5M416160C-6S		M5M416160C-7S		Unit
		Min	Max	Min	Max	Min	Max	
tRASS	Self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
tRPS	Self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
tCHS	Self refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within tNS / tSN before / after self refresh, on the condition of tNS≦64ms and tSN≦64ms.

tNS

tSN

DISTRIBUTED REFRESH
< 4K / 64ms >

DISTRIBUTED REFRESH
< 4K / 64ms >
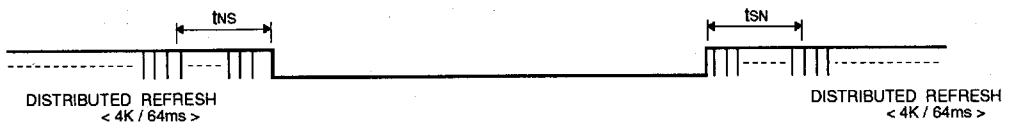
(2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within tNS / tSN before / after self refresh, on the condition of tNS +tSN≦64ms.

tNS

tSN

BURST REFRESH
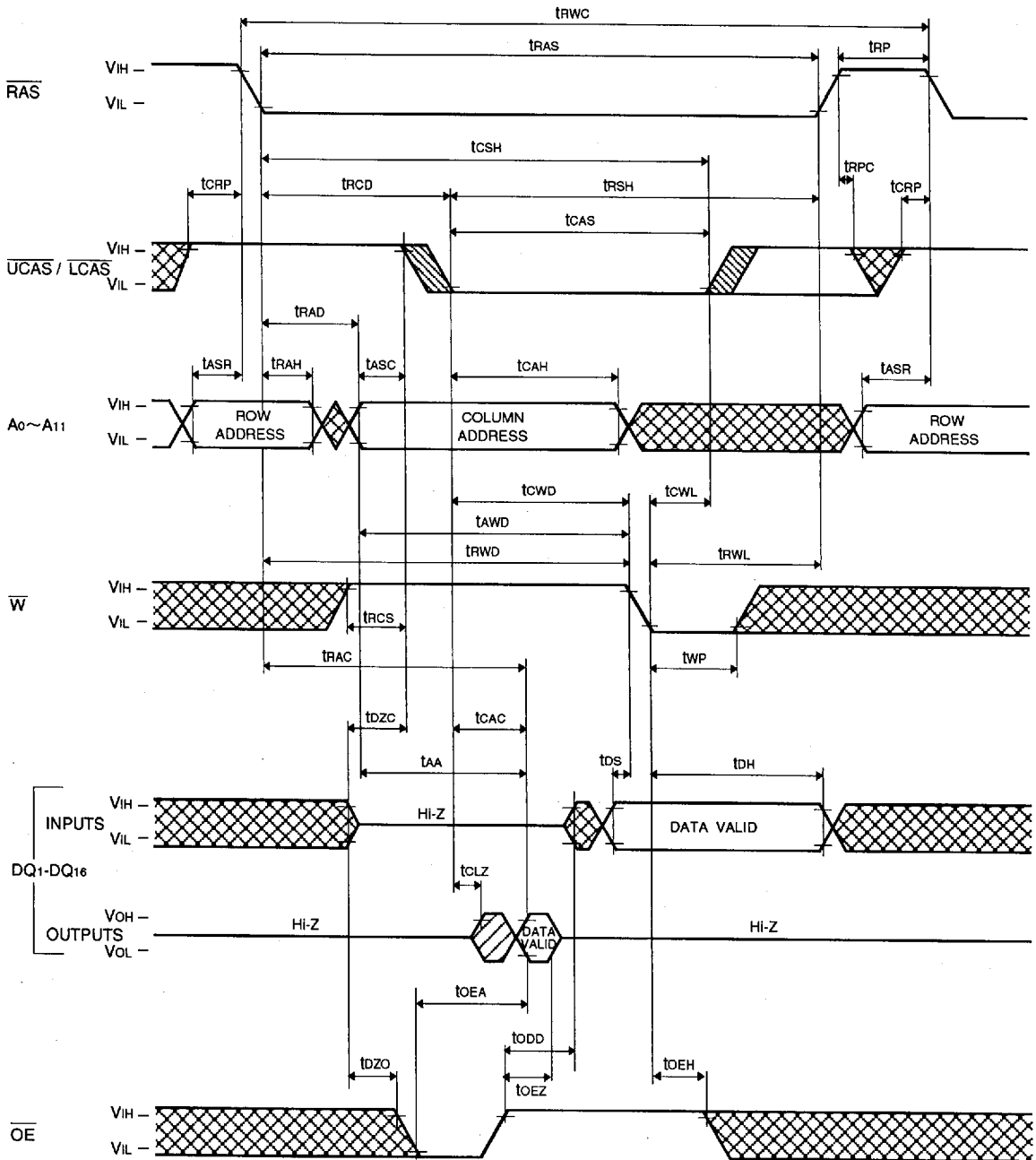< 4K / 64ms >

BURST REFRESH
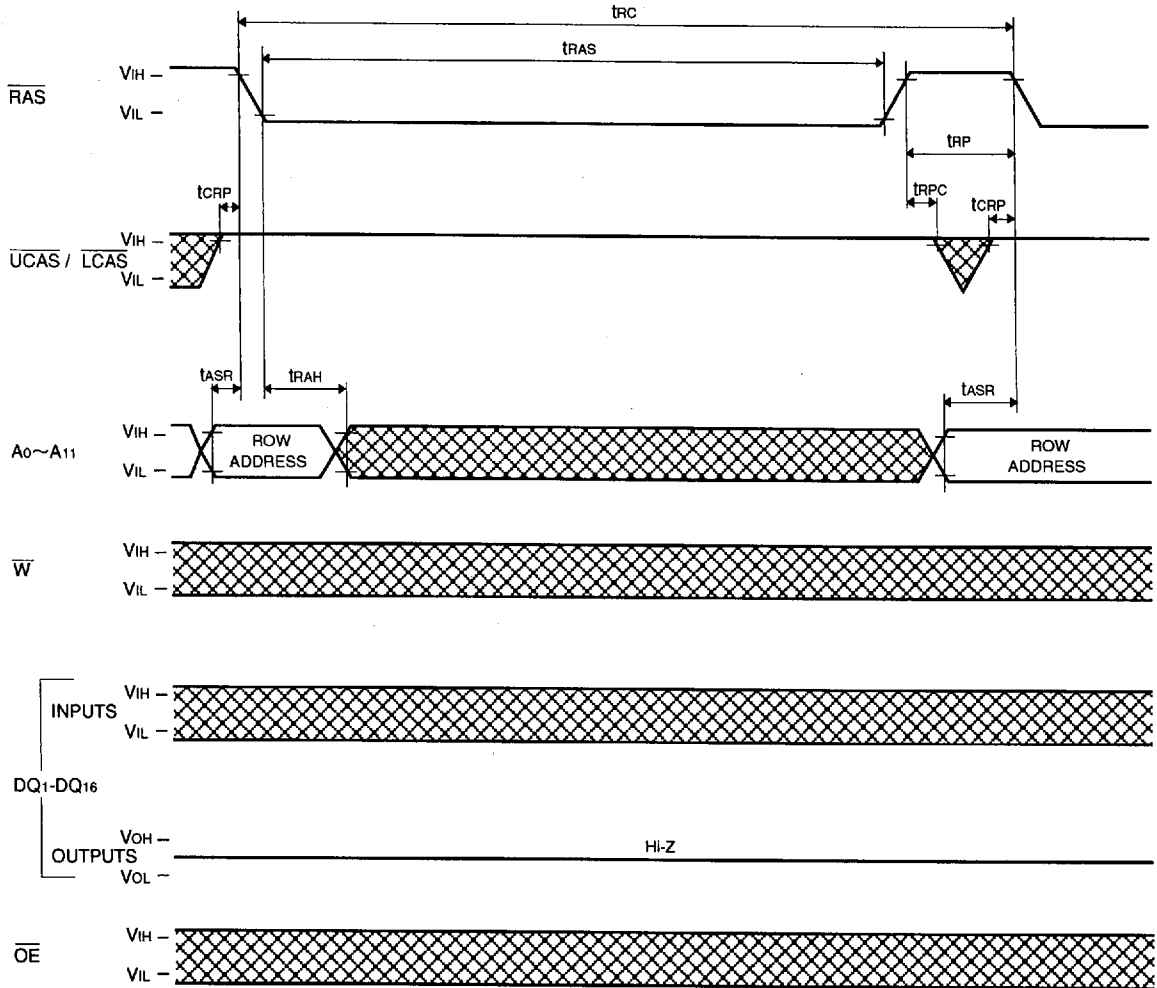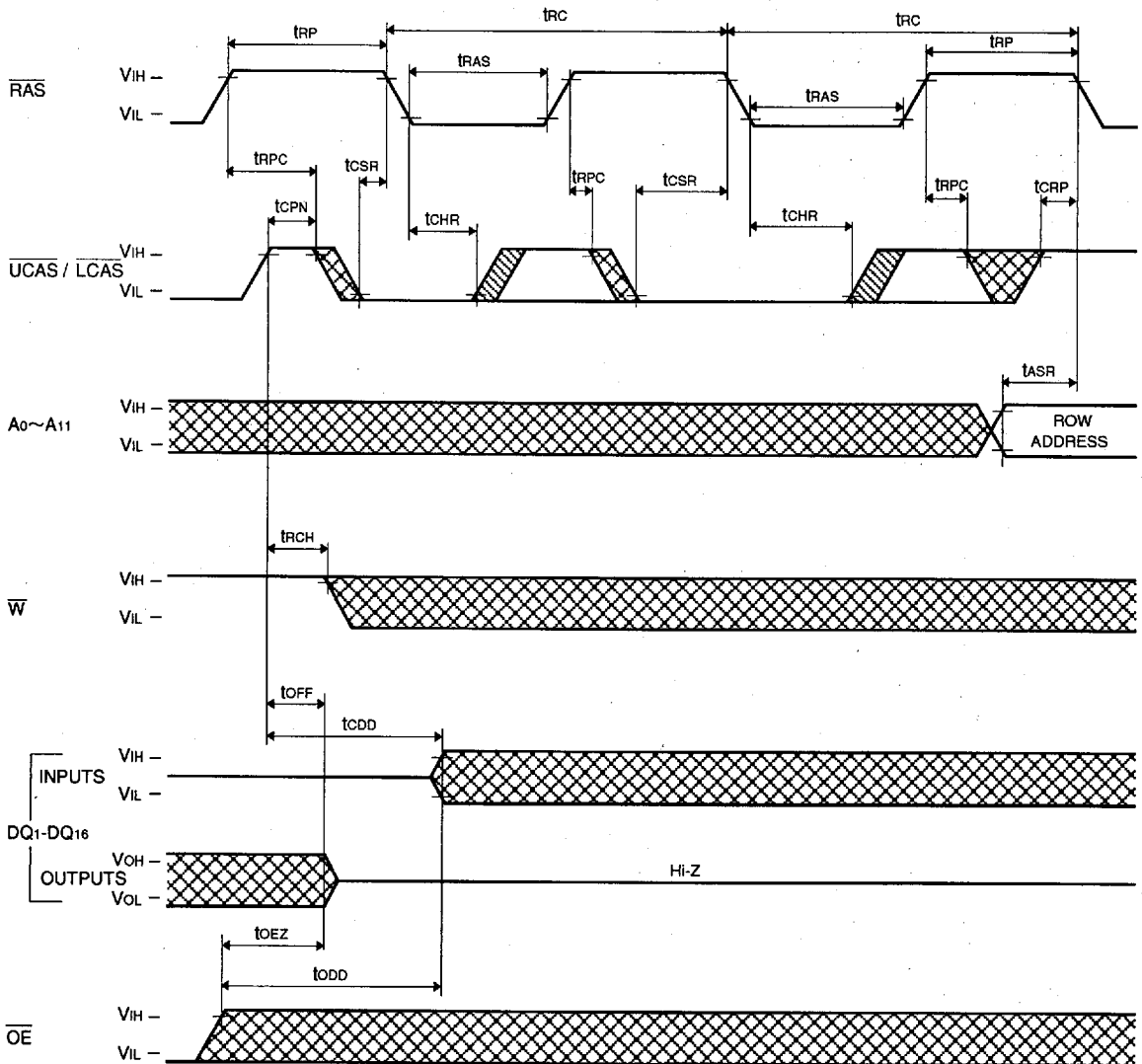< 4K / 64ms >
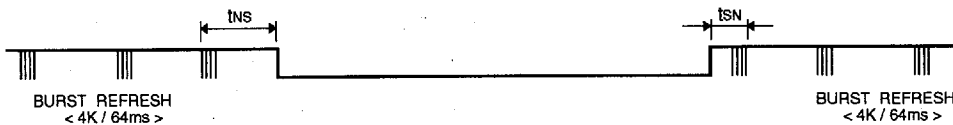
6249825 0028808 418

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Timing Diagrams (Note 28)
Read Cycle

Note 28

Indicates the don't care input.
V_{IH}(min.) $\leqq V_{IN} \leqq V_{IH}$(max) or V_{IL}(min.) $\leqq V_{IN} \leqq V_{IL}$(max)
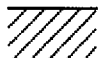
Indicates the
invalid output.

Indicates the skew of the two inputs.

PRELIMINARY

Notice: This is not a final specification
Some parametric limits are subject to change

Upper / (Lower) Byte Read Cycle

MITSUBISHI ELECTRIC

Write Cycle (Early write)

Upper / (Lower) Byte Write Cycle (Early write)

MITSUBISHI
ELECTRIC

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

Write Cycle (Delayed write)

6249825 0028813 885

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

Upper / (Lower) Byte Write Cycle (Delayed write)

■ 6249825 0028814 711 ■

MITSUBISHI ELECTRIC
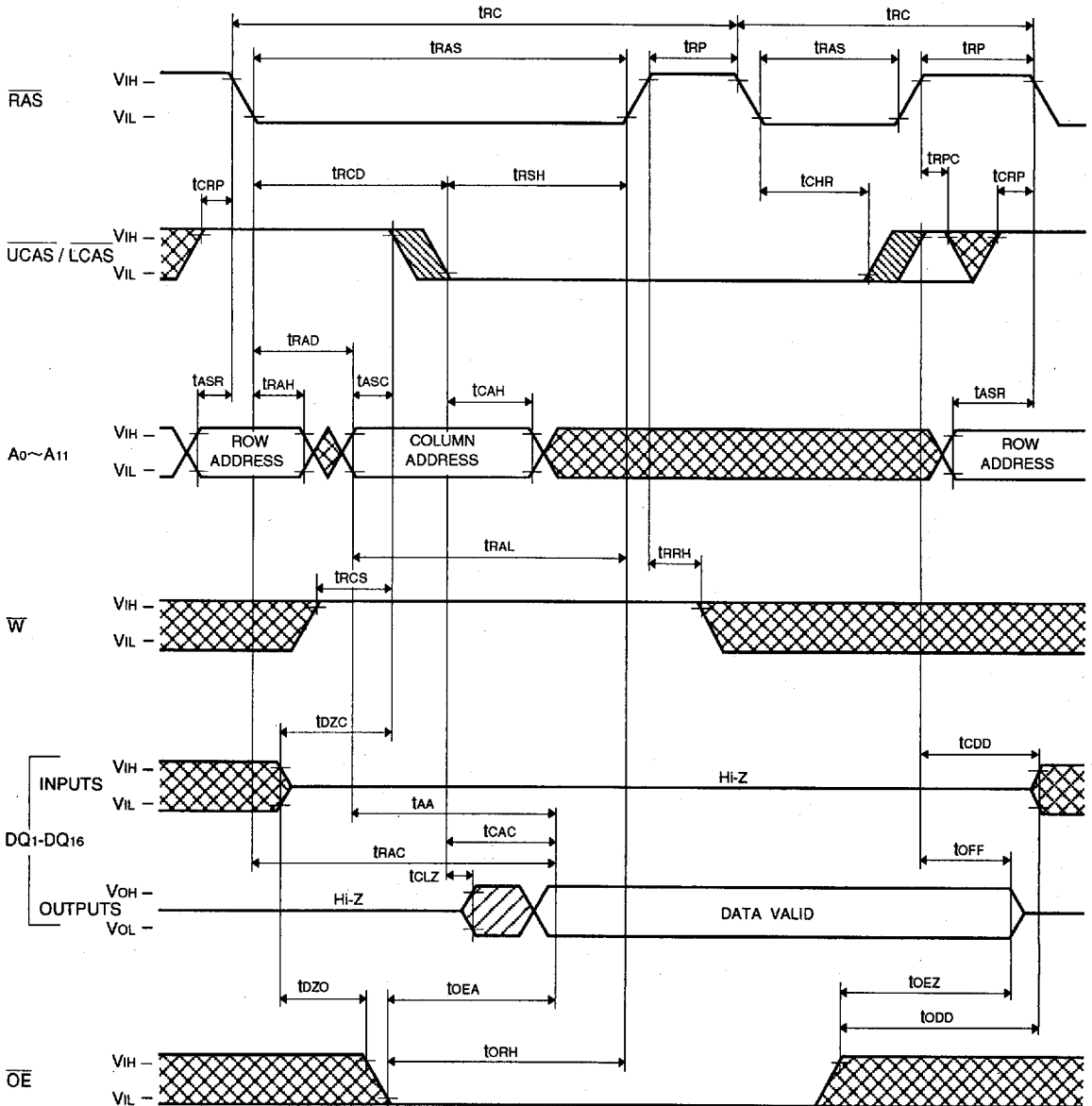
PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Read-Write, Read-Modify-Write Cycle

MITSUBISHI
ELECTRIC

Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle

MITSUBISHI
ELECTRIC

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

$\overline{\text{RAS}}$-only Refresh Cycle

MITSUBISHI LSIs

M5M416160CJ,TP-5,-6,-7,-5S,-6S,-7S

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle, Extended Refresh Cycle *

MITSUBISHI ELECTRIC

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper / (Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle ∗
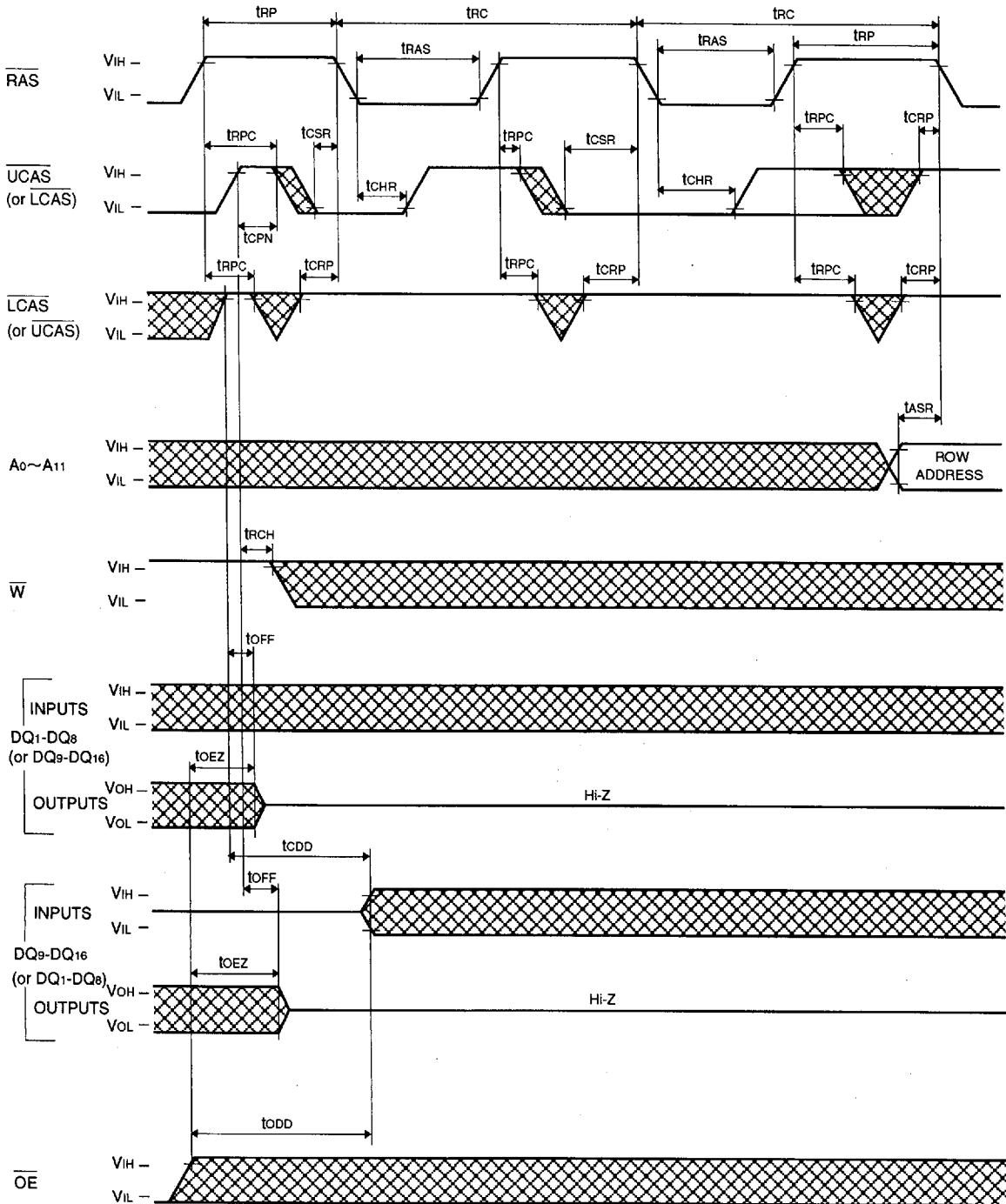
6249825 0028819 2T3

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

Hidden Refresh Cycle (Read) (Note 29)

Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

6249825 0028820 T15

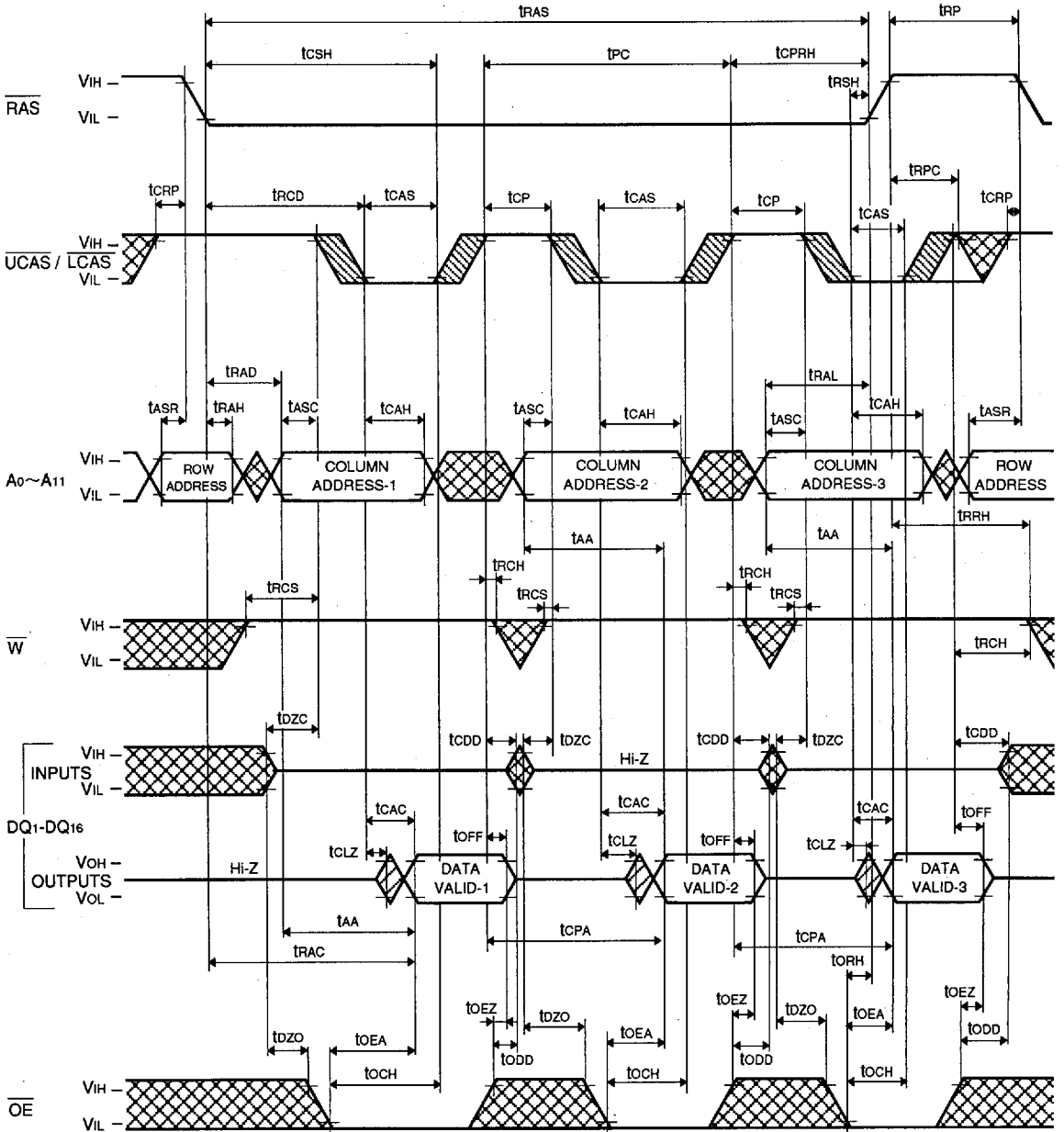MITSUBISHI ELECTRIC

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

Upper / (Lower) Hidden Refresh Cycle (Byte Read) (Note 29)
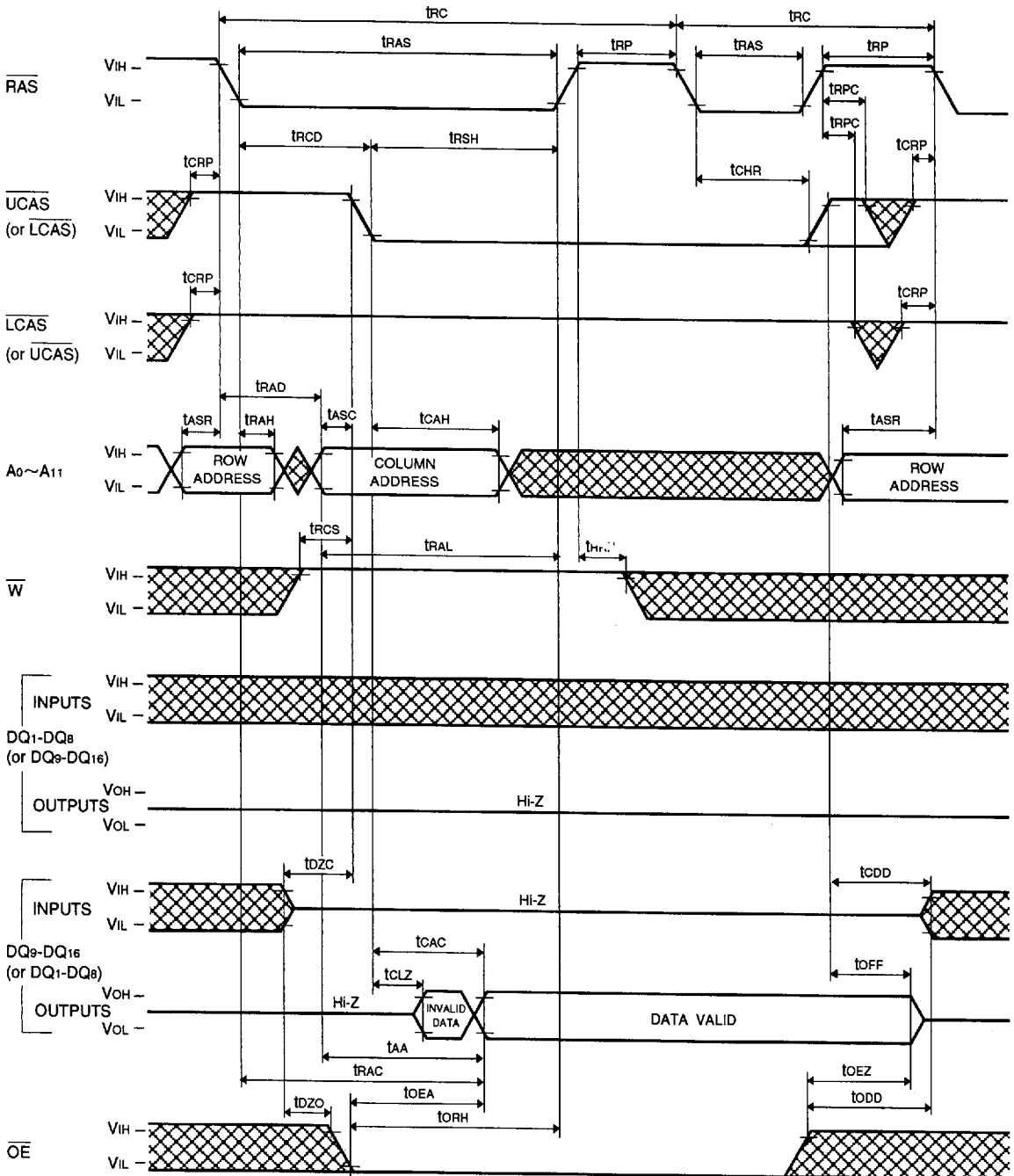
Signal	Labels
RAS	t_{RC}, t_{RAS}, t_{RP}, t_{RPC}
UCAS (or LCAS)	t_{CRP}, t_{RCD}, t_{RSH}, t_{CHR}
LCAS (or UCAS)	t_{CRP}
$A_0 \sim A_{11}$	t_{RAD}, t_{ASR}, t_{RAH}, t_{ASC}, t_{CAH}, ROW ADDRESS, COLUMN ADDRESS, ROW ADDRESS
W	t_{RCS}, t_{RAL}, t_{RWL}
INPUTS DQ1-DQ8 (or DQ9-DQ16) OUTPUTS	Hi-Z
INPUTS DQ9-DQ16 (or DQ1-DQ8) OUTPUTS	t_{DZC}, t_{CDD}, Hi-Z, t_{CAC}, t_{CLZ}, t_{OFF}, Hi-Z, INVALID DATA, DATA VALID, t_{AA}, t_{RAC}, t_{OEZ}, t_{ODD}, t_{OEA}, t_{DZO}, t_{ORH}
OE	

Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

6249825 0028821 951

PRELIMINARY

Notice This is not a final specification.
Some parametric limits are subject to change
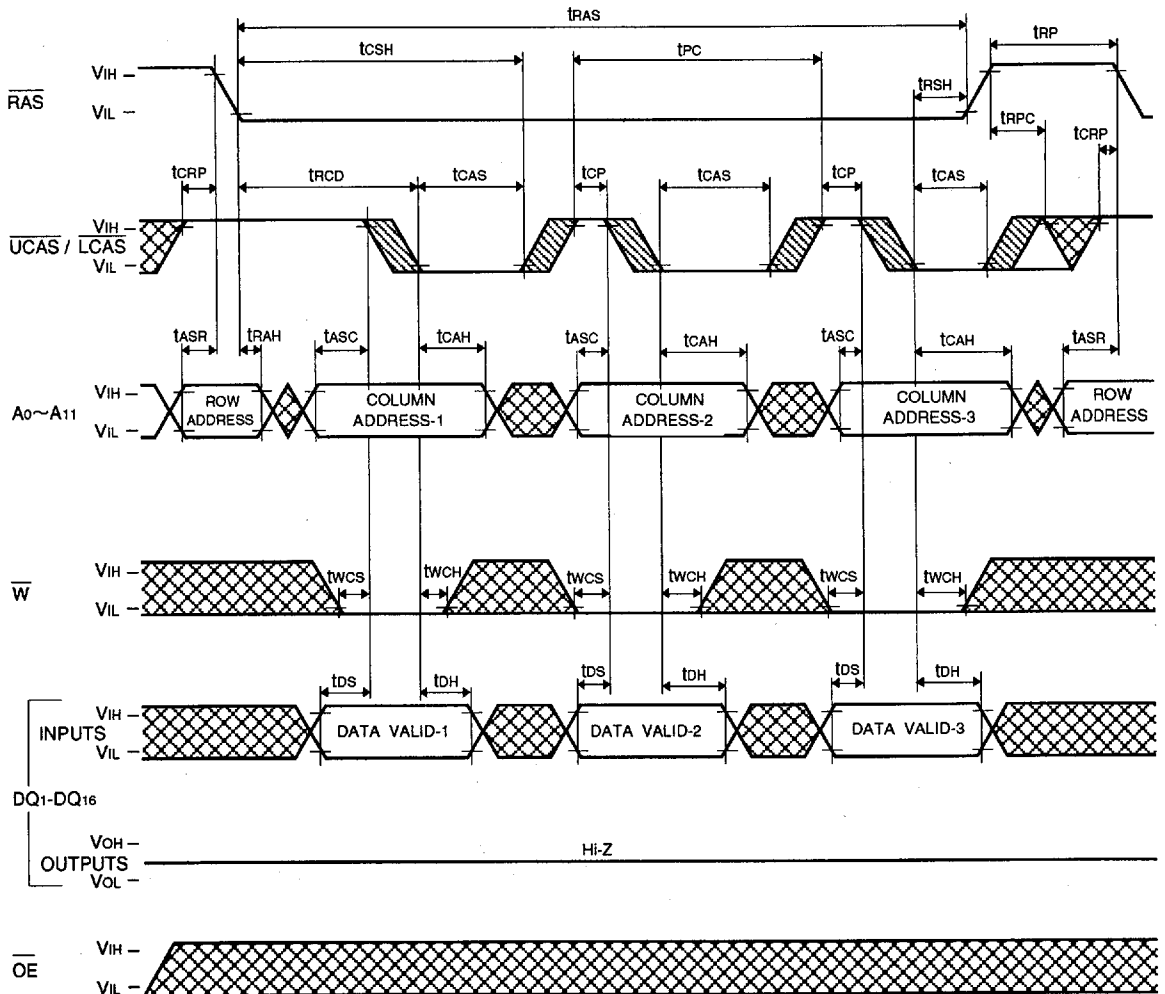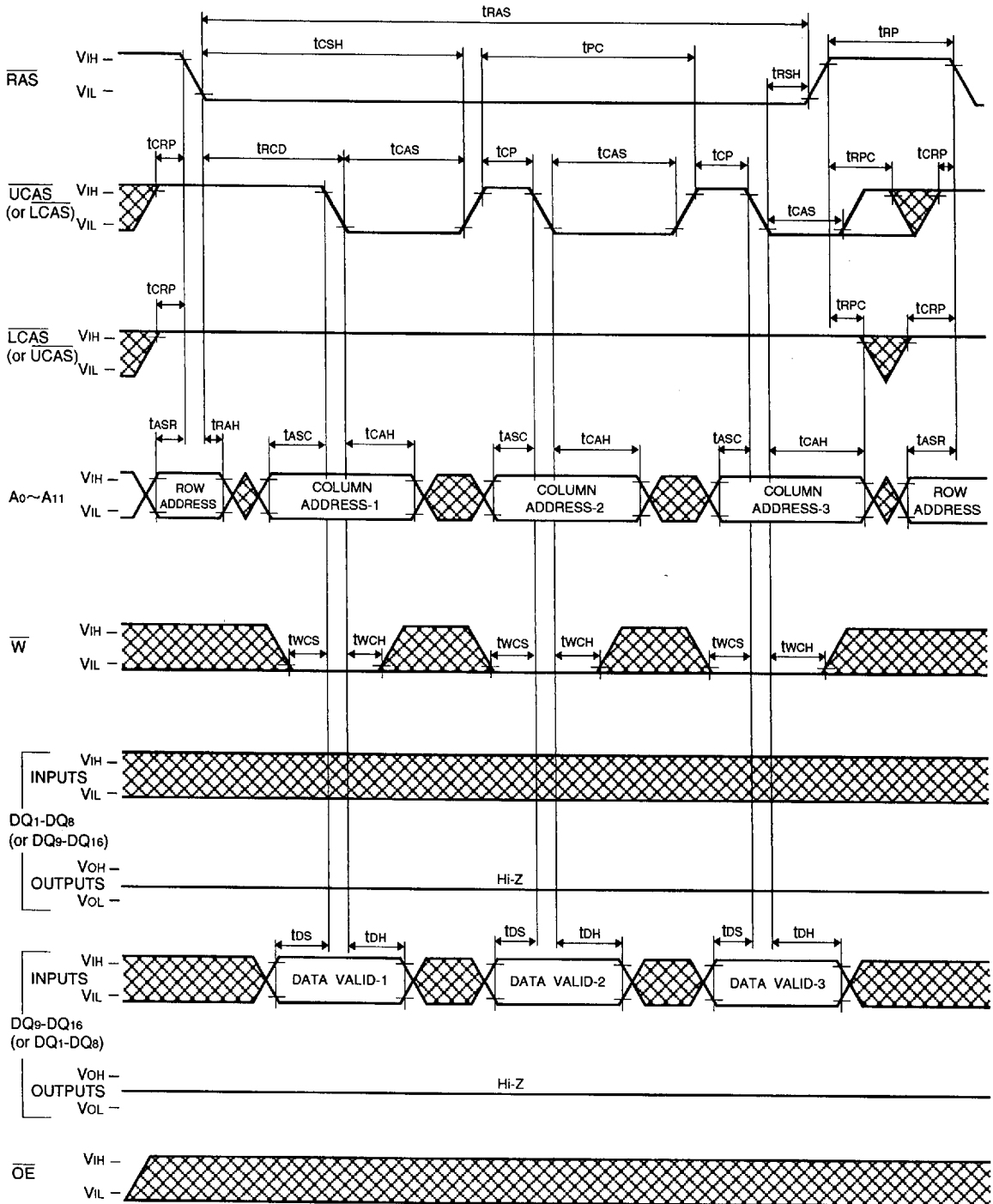
Fast Page Mode Read Cycle

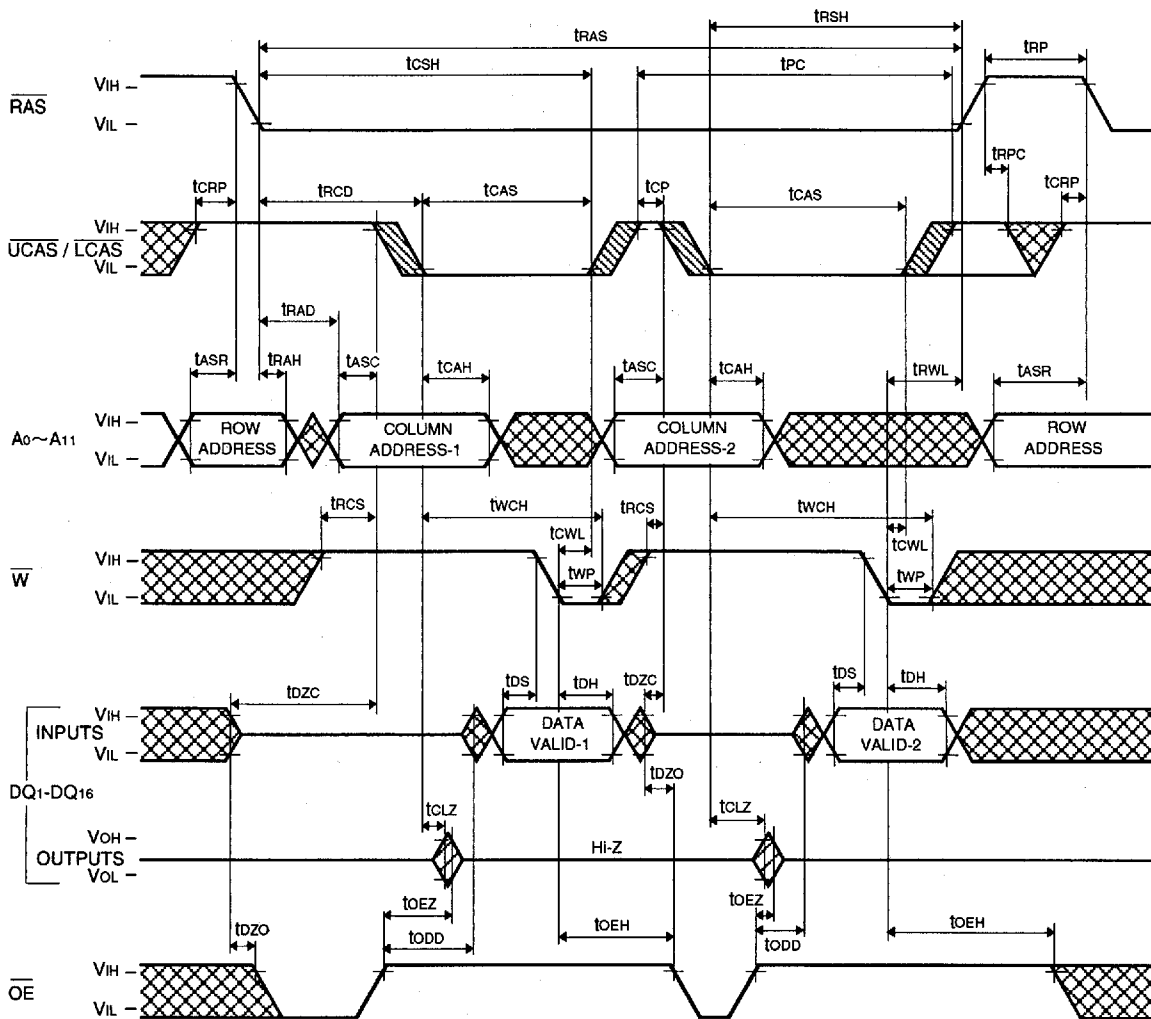6249825 0028822 898

MITSUBISHI
ELECTRIC

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper / (Lower) Fast Page Mode Read Cycle

6249825 0028823 724

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Write Cycle (Early Write)

■ 6249825 0028824 660 ■

**MITSUBISHI
ELECTRIC**

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Upper / (Lower) Byte Write Cycle (Early Write)

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

Fast Page Mode Write Cycle (Delayed Write)

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Upper / (Lower) Byte Write Cycle (Delayed Write)

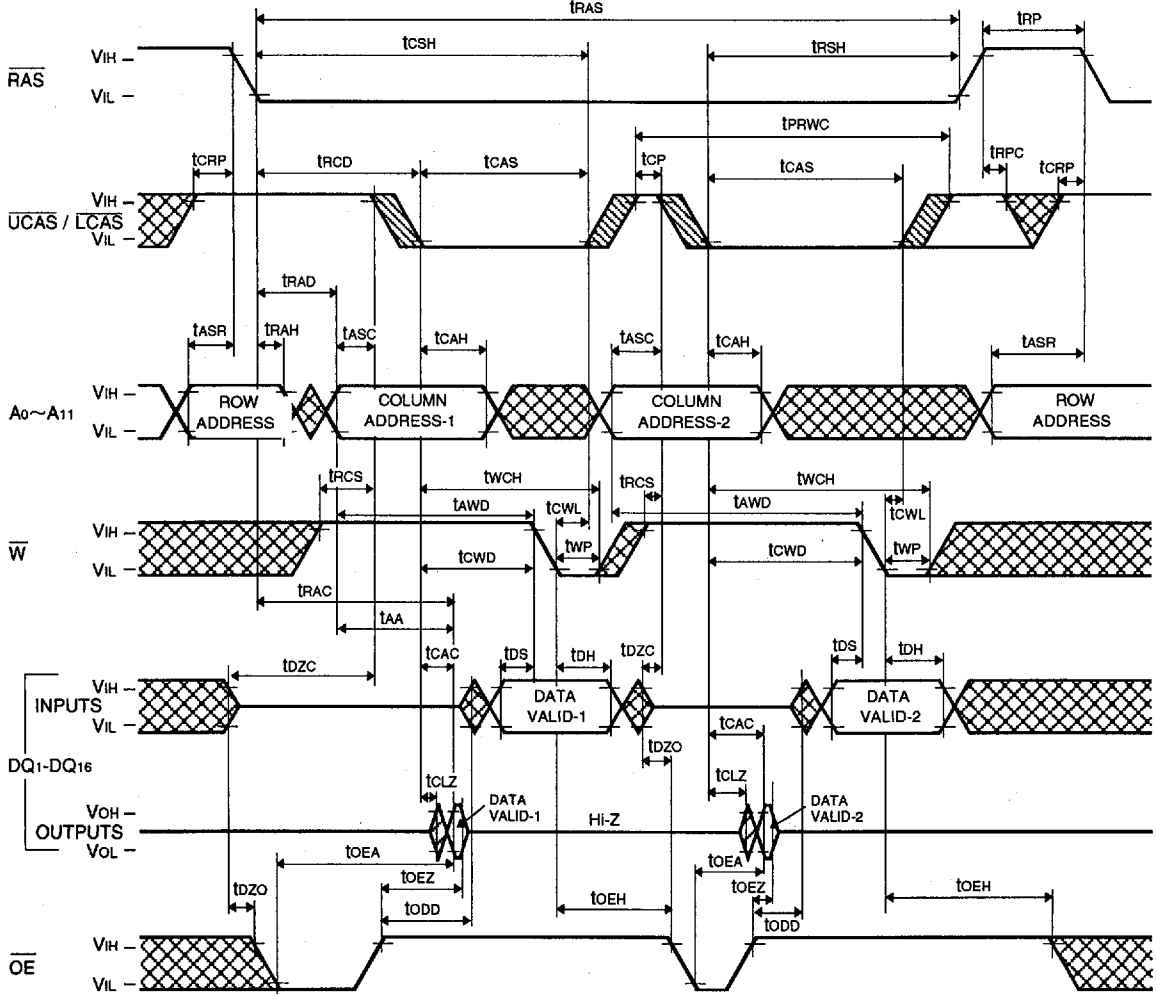$\overline{RAS}$ — V_{IH}, V_{IL}

$\overline{UCAS}$ (or $\overline{LCAS}$) — V_{IH}, V_{IL}

$\overline{LCAS}$ (or $\overline{UCAS}$) — V_{IH}, V_{IL}

$A_0 \sim A_{11}$ — V_{IH}, V_{IL} — ROW ADDRESS, COLUMN ADDRESS-1, COLUMN ADDRESS-2, ROW ADDRESS

$\overline{W}$ — V_{IH}, V_{IL}

INPUTS DQ_1-DQ_8 (or DQ_9-DQ_{16}) — V_{IH}, V_{IL}

OUTPUTS — V_{OH}, V_{OL} — Hi-Z

INPUTS DQ_9-DQ_{16} (or DQ_1-DQ_8) — V_{IH}, V_{IL} — DATA VALID-1, DATA VALID-2

OUTPUTS — V_{OH}, V_{OL} — Hi-Z

$\overline{OE}$ — V_{IH}, V_{IL}

Timing parameters shown: tRSH, tRAS, tCSH, tPC, tRP, tCRP, tRCD, tCAS, tCP, tCAS, tRPC, tCRP, tRAD, tASR, tRAH, tASC, tCAH, tASC, tCAH, tRWL, tASR, tRCS, tWCH, tCWL, tWP, tRCS, tWCH, tCWL, tWP, tDZC, tDS, tDH, tDZC, tDS, tDH, tDZO, tDZO, tCLZ, tCLZ, tOEZ, tODD, tOEH, tOEZ, tODD, tOEH

6249825 0028827 37T

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

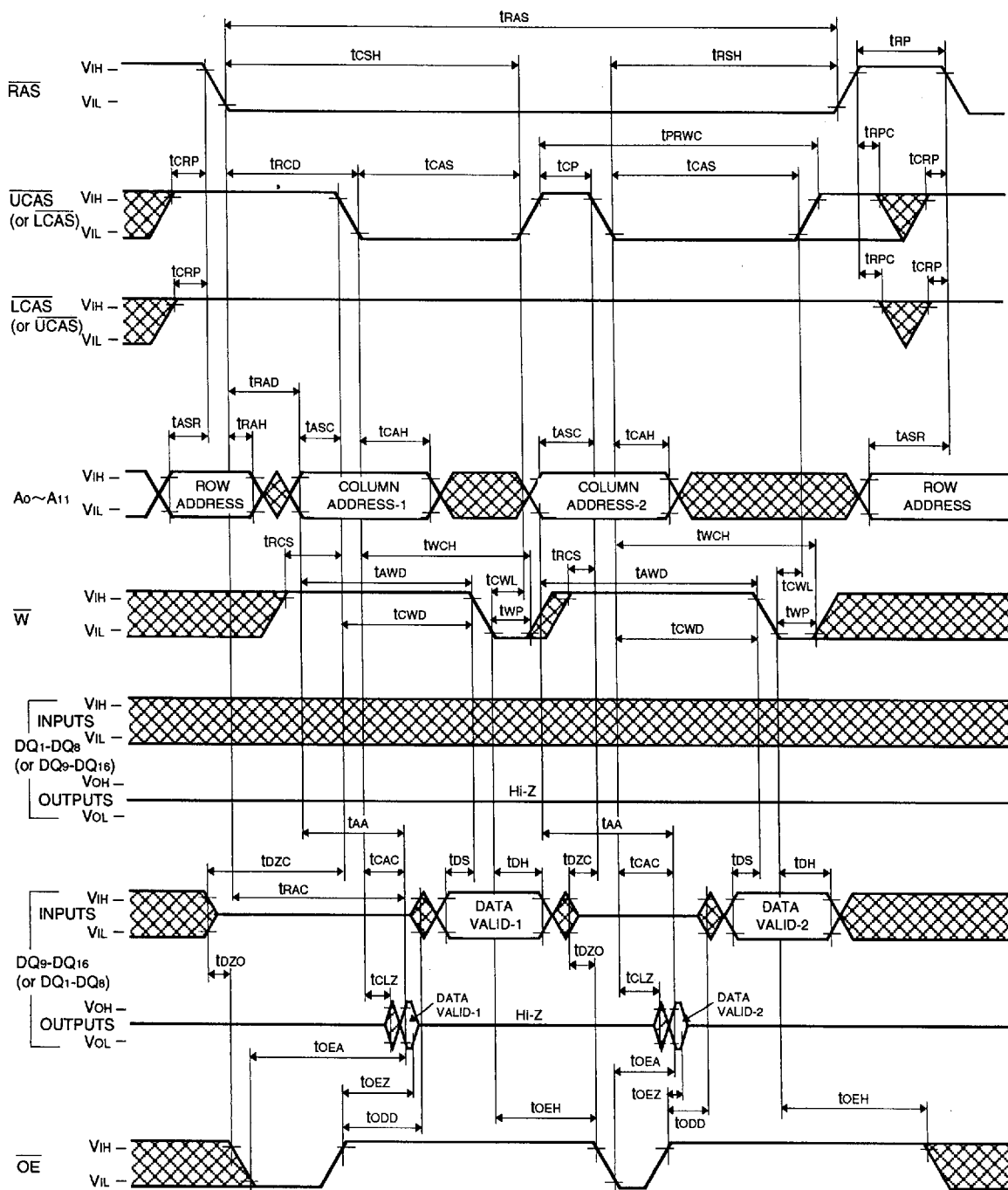## Fast Page Mode Read-Write, Read-Modify-Write Cycle

6249825 0028828 206

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Read-Upper / (Lower) Write, Read-Modify-Upper / (Lower) Write Cycle
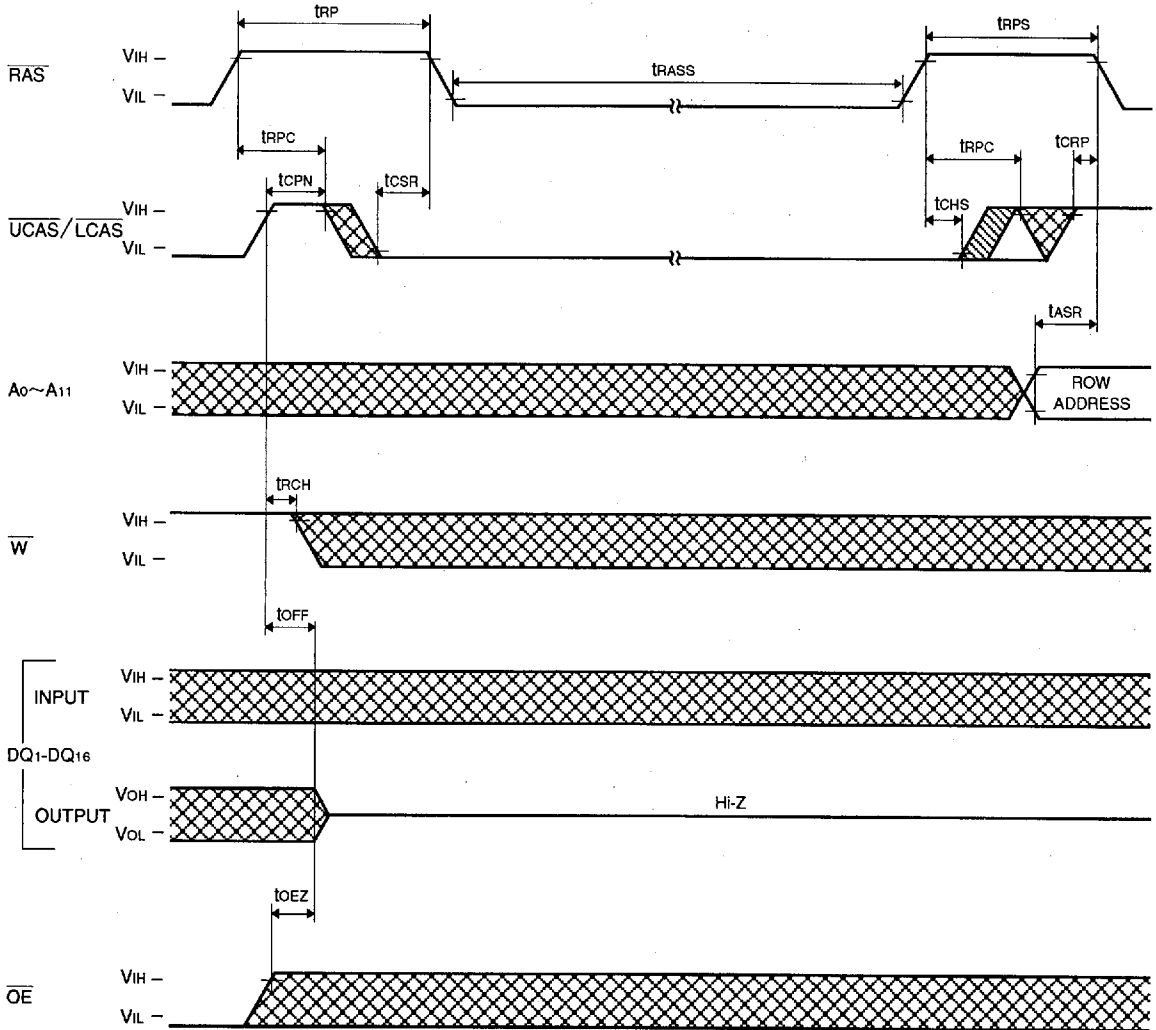

■ 6249825 0028829 142 ■

PRELIMINARY

Notice. This is not a final specification
Some parametric limits are subject to change

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM
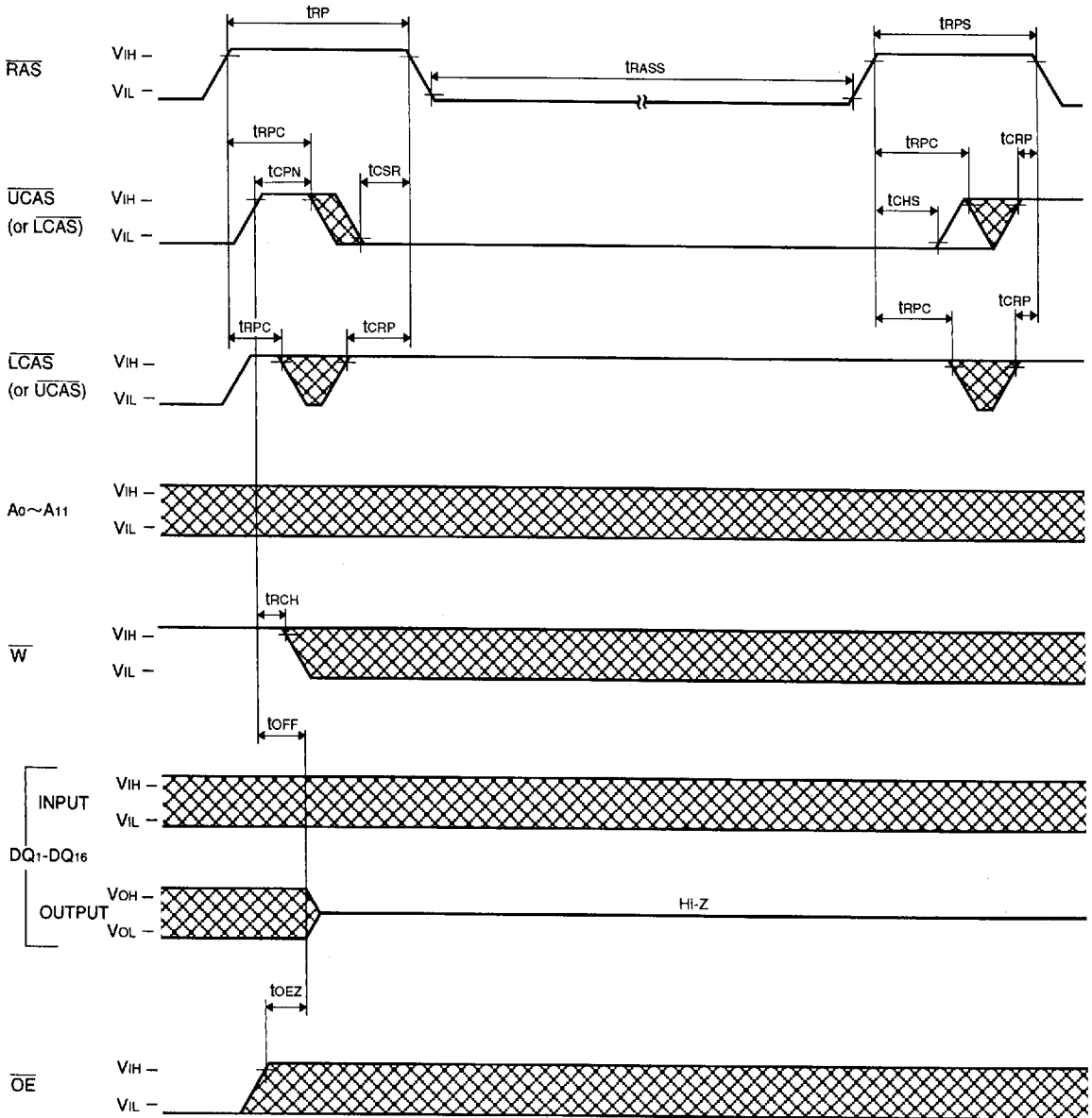
Self Refresh Cycle＊

MITSUBISHI
ELECTRIC

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change

Upper / (Lower) Self Refresh Cycle∗