REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate. Add devices 02 through 12. Add case outlines Z, U, T, and M. Add CAGE 52088 as source of supply for devices 02 through 04, CAGE 31468 as source of supply for devices 05 through 08, and CAGE 65342 as source of supply for devices 09 through 12. Editorial changes throughout.	93-09-16	M.A. Frye
B	Changes in accordance with NOR 5962-R044-94.	94-01-05	M.A. Frye
C	Changes in accordance with NOR 5962-R197-94.	94-05-20	M.A. Frye
D	Update boilerplate. Add devices 13 and 14. Add case outlines P and 9. Add CAGE 52088 as source of supply for devices 13 and 14. Editorial changes throughout.	94-06-24	M.A. Frye
E	Changes in accordance with NOR 5962-R259-94.	94-08-08	M.A. Frye
F	Update boilerplate. Make corrections to table IB. Add device types 15 through 18 and CAGE 65342 as source of supply. Add device type 19 and CAGE 34168 as source of supply. Editorial changes throughout.	95-11-17	M.A. Frye
G	Changes in accordance with NOR 5962-R097-96	96-04-11	M.A. Frye
H	Changes in accordance with NOR 5962-R122-96	96-05-06	M.A. Frye
J	Changes in accordance with NOR 5962-R239-97	97-03-31	Raymond Monnin
K	Updated boilerplate. Added case outline "4". Corrected terminal connection pinouts for case outlines "Z" and "U". glg	97-08-27	Raymond Monnin
L	Added pin 1 index indicator for case outlines "N". - ksr	00-10-17	Raymond Monnin
M	Boilerplate update and part of five year review. tcr	06-08-01	Raymond Monnin
N	Update drawing to current MIL-PRF-38535 requirements. Update radiation features in section 1.6 and SEP table IB. Remove class M references. – llb	15-06-11	Charles Saffle

REV																				
SHEET																				
REV	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			

REV STATUS	REV	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
92-09-30

REVISION LEVEL
N

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 32K X 8 STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

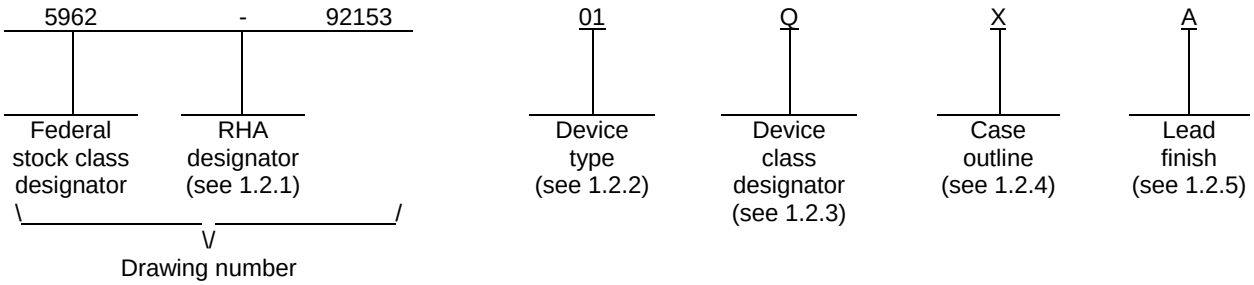
SIZE	CAGE CODE	
A	**67268**	**5962-92153**

SHEET 1 OF 31

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Input/output levels	Chip enable 2/	Access time
01	LOR2568C	32K X 8 CMOS SRAM	CMOS	Dual	60 ns
02	LOR2568T	32K X 8 CMOS SRAM	TTL	Dual	60 ns
03	LOR2568C	32K X 8 CMOS SRAM	CMOS	Dual	40 ns
04	LOR2568T	32K X 8 CMOS SRAM	TTL	Dual	40 ns
05	HC6856	32K X 8 CMOS SRAM	CMOS	Dual	60 ns
06	HC6856	32K X 8 CMOS SRAM	TTL	Dual	60 ns
07	HC6856	32K X 8 CMOS SRAM	CMOS	Dual	40 ns
08	HC6856	32K X 8 CMOS SRAM	TTL	Dual	40 ns
09	UT7156C55PB	32K X 8 CMOS SRAM	CMOS	Single	55 ns
10	UT7156T55PB	32K X 8 CMOS SRAM	TTL	Single	55 ns
11	UT7156C55WB	32K X 8 CMOS SRAM	CMOS	Dual	55 ns
12	UT7156T55WB	32K X 8 CMOS SRAM	TTL	Dual	55 ns
13	LOR2568C	32K X 8 CMOS SRAM	CMOS	Dual	30 ns
14	LOR2568T	32K X 8 CMOS SRAM	TTL	Dual	30 ns
15	UT7156C70PB	32K X 8 CMOS SRAM	CMOS	Single	70 ns
16	UT7156T70PB	32K X 8 CMOS SRAM	TTL	Single	70 ns
17	UT7156C70WB	32K X 8 CMOS SRAM	CMOS	Dual	70 ns
18	UT7156T70WB	32K X 8 CMOS SRAM	TTL	Dual	70 ns
19	HC6856	32K X 8 CMOS SRAM	CMOS	Dual	35 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 and QML-38535.
2/ Any device type, when ordered in case outline "M" or "9", is single chip enable.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	36	Flat pack
Y	See figure 1	40	Flat pack
Z	See figure 1	36	Flat pack
U	See figure 1	36	Flat pack
T	See figure 1	36	Flat pack
M	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
N	See figure 1	36	Flat pack
9	See figure 1	28	Flat pack
4	See figure 1	36	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 3/ 4/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.3 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+250°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X and Y	3.3°C/watt
Cases Z, U, and 4	2.2°C/watt.
Case T	10°C/watt
Case M	See MIL-STD-1835
Case N	2.1°C/watt
Case 9	1.8°C/watt
Output voltage applied to high Z state	-0.3 V dc to V_{CC} + 0.3 V dc
Maximum power dissipation (P_D)	2 watts
Maximum junction temperature (T_J)	+150°C 5/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc (min) to 5.5 V dc (max)
Supply voltage (V_{SS})	0.0 V dc
High level input voltage range (V_{IH}):	
Device types 01,03,09,11,13,15,17 (CMOS levels)	3.5 V dc to V_{CC} + 0.3 V dc
Device types 05,07,19 (CMOS levels)	0.7 x V_{CC} to V_{CC} + 0.3 V dc
Device types 02,04,06,08,10,12,14,16,18 (TTL levels)	2.2 V dc to V_{CC} + 0.3 V dc
Low level input voltage range (V_{IL}):	
Device types 01,03,09,11,13,15,17 (CMOS levels)	-0.3 V dc to 1.5 V dc
Device types 05,07,19 (CMOS levels)	-0.3 V dc to 0.3 x V_{CC}
Device types 02,04,06,08,10,12,14,16,18 (TTL levels)	-0.3 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, method 5012)	100 percent

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ All voltages referenced to V_{SS} (V_{SS} = ground), unless otherwise specified.
5/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

1.6 Radiation features 6/

Maximum total ionizing dose available (dose rate = 50 - 300 rad(Si)/s)……...1 x 10^6 rad(Si)
Single event phenomenon (SEP):
No single event latch-up (SEL) occurs at effective LET (see 4.4.4.2) …… ≤ 120 MeV-cm^2/mg
Heavy ion single event upset error rate (SER) … …… 1 x 10^{-10} upsets/bit-day 7/
Proton Single event upset error rate (SER) ..... 1 x10^{-11} upsets/bit-day 7/
Neutron irradiation (1MeV equivalent) ..... 1 x10^{14} neutrons/cm^2 8/
Dose rate data induced upset (dose rate duration ≤ 20 ns) .....……1 x10^9 rad(Si)/s
Dose rate survivability (dose rate duration ≤ 20 ns) .....1 x10^{12} rad(Si)/s
Dose rate induced latch-up……..... Immune by SOI technology

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

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6/ For details on RHA parameters and test results, contact the vendor.
7/ Projected performance based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100 mil Aluminum shield using Weibull parameters based on an analysis of test data and simulation results. Weibull parameters and other relevant attributes are available from the vendor upon request to calculate projected SER performance for other orbits and environments.
8/ Guaranteed but not tested for 1MeV equivalent neutrons.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation test circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4 mA, V_{IL} = 1.5 V, V_{IH} = 3.5 V		1,2,3	01,13	2.4		V
					03	4.2		
		V_{CC} = 4.5 V, I_{OH} = -5 mA, V_{IL} = 1.35 V, V_{IH} = 3.15 V			05,07,19	4.2		
		V_{CC} = 4.5 V, I_{OH} = -200 µA, V_{IL} = 1.5 V, V_{IH} = 3.5 V			09,11,15,17	4.45		
		V_{CC} = 4.5 V, I_{OH} = -4 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V			06,08	4.2		
					02,04,10,12,14,16,18	2.4		
			M,D,P,L,R,F,G,H	1 2/		3/		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA, V_{IL} = 1.5 V, V_{IH} = 3.5 V		1,2,3	01-03,13		0.4	V
		V_{CC} = 4.5 V, I_{OL} = 10 mA, V_{IL} = 1.35 V, V_{IH} = 3.15 V			05,07,19		0.4	
		V_{CC} = 4.5 V, I_{OL} = 200 µA, V_{IL} = 1.5 V, V_{IH} = 3.5 V			09,11,15,17		0.05	
		V_{CC} = 4.5 V, I_{OL} = 8 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V			04,06,08,10,12,14,16,18		0.4	
			M,D,P,L,R,F,G,H	1 2/			3/	V
Input leakage current	I_{ILK}	V_{CC} = 5.5 V, V_{IN} = 0.0 V to 5.5 V, all other pins at 0.0 V		1,2,3	01-08,13,14 19	-5	5	µA
					09-12,15-18	-10	10	
			M,D,P,L,R,F,G,H	1 2/		3/	3/	µA
Output leakage current	I_{OLK}	V_{CC} = 5.5 V, V_{OUT} = 0.0 V to 5.5 V, all other pins at 0.0 V		1,2,3	All	-10	10	µA
			M,D,P,L,R,F,G H	1 2/		3/	3/	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Data retention voltage	V_{DR}	V_{CC} = 2.5 V		1,2,3	All	2.5		V
			M,D,P, L,R, F,G, H	1 2/		 3/		 V
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, f = f_{MAX} 4/, S = GND, E = V_{CC}, no output loading		1,2,3	07,08, 13,14		180	mA
					01-06		130	
					09-12, 15-18		120	
					19		202	
			M,D,P, L,R, F,G, H	1 2/			 3/	 mA
Supply current (deselected)	I_{CC2}	V_{CC} = 5.5 V, f = f_{MAX} 4/, S = V_{CC}, E = GND		1,2,3	01,02, 13,14		2	mA
					03-12, 15-19		1.2	
			M,D,P, L,R, F,G, H	1 2/			 3/	 mA
Supply current (standby)	I_{CC3}	V_{CC} = 5.5 V, f = 0.0 MHz, S = V_{CC}, E = GND		1,2,3	01,02, 13,14		2	mA
					03-12, 15-19		1.2	
			M,D,P, L,R, F,G, H	1 2/			 3/	 mA
Data retention current	I_{CC4}	V_{CC} = 2.5 V		1,2,3	01,02, 13,14		1	mA
					03-12, 15-19		0.4	
			M,D,P, L,R, F,G, H	1 2/			 3/	 mA
Input capacitance 5/	C_{IN}	V_I = 5.0 V or 0.0 V, T_A = +25°C, (see 4.4.1e) f = 1.0 MHz		4	01-04, 13,14		4	pF
					05-08, 19		6	
					09-12, 15-18		20	
Output capacitance 5/	C_{OUT}	V_O = 5.0 V or 0.0 V, T_A = +25°C, (see 4.4.1e) f = 1.0 MHz		4	01-04, 13,14		7	pF
					05-08, 19		8	
					09-12, 15-18		20	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Functional tests		See 4.4.1c		7,8A,8B	All			
			M,D,P, L,R, F,G, H	7 2/		3/		
Read cycle								
Read cycle time	t_{AVAV}			9,10,11	01,02	60		ns
					03-08	40		
					09-12, 15-18	55		
					13,14	30		
					19	35		
			M,D,P, L,R, F,G, H	9 2/		3/		ns
Address access time	t_{AVQV}			9,10,11	01,02		60	ns
					03-08		40	
					09-12, 15-18		55	
					13,14		30	
					19		35	
			M,D,P, L,R, F,G, H	9 2/			3/	ns
Chip enable/select access time	t_{EHQV} t_{SLQV}			9,10,11	01,02		60	ns
					03-08		40	
					09-12, 15-18		55	
					13,14		30	
					19		35	
			M,D,P, L,R, F,G, H	9 2/			3/	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output hold after address change	t_{AVQX}			9,10,11	01-18	5		ns
					19	5.5		
			M,D,P, L,R, F,G, H	9 2/		3/		ns
Output enable access time	t_{GLQV}			9,10,11	01,03, 09-12, 14-18		15	ns
					02,04		18	
					05-08, 19		10	
					13		12	
			M,D,P, L,R, F,G, R	9 2/			3/	ns
Chip select/enable to output active	t_{SLQX} t_{EHQX} 6/			9,10,11	01-08, 13,14, 19	3		ns
					09-12, 15-18	0		
			M,D,P, L,R, F,G, H	9 2/		3/		ns
Output enable to output active	t_{GLQX}			9,10,11	01-04, 13,14	3		ns
					05-12, 15-19	0		
			M,D,P, L,R, F,G, H	9 2/		3/		ns
Chip select/disable to output disable	t_{SHQZ} t_{ELQZ}	6/		9,10,11	01-04		15	ns
					13,14		12	
		7/			05-08, 19		15	
					09-12, 15-18		20	
			M,D,P, L,R, F,G, H	9 2/			3/	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output enable to output disable	t_{GHQZ}	6/		9,10,11	01-04		15	ns
					13,14		12	
		7/			05-08, 19		10	
					09-12, 15-18		15	
			M,D,P, L,R, F,G, H	9 2/			3/	ns
Write cycle								
Write enable to output disable	t_{WLQZ}	6/		9,10,11	01-04		15	ns
					13,14		12	
		7/			05-08, 19		10	
					09-12		20	
					15-18		25	
			M,D,P, L,R, F,G, H	9 2/			3/	ns
Data setup to end of write	t_{DVWH}			9,10,11	01,02, 09-12	40		ns
					05,06, 15-18	50		
					03,04, 07,08	30		
					13,14	25		
					19	27		
			M,D,P, L,R, F,G, H	9 2/		3/		ns
Data hold after end of write	t_{WHDX}			9,10,11	01,02, 04, 09-12	5		ns
					03,13, 14	3		
					05-08, 15-19	0		
			M,D,P, L,R, F,G, H	9 2/		3/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output active after end of write	t_{WHQX}			9,10,11	01,02	3		ns
					03,04, 13,14	1		
					05-08, 19	5		
					09-12, 15-18	0		
			M,D,P, L,R, F,G, H	9 2/		3/		ns
Write cycle time	t_{AVAV} 8/			9,10,11	01,02, 05,06	60		ns
					09-12	55		
					03,04, 07,08	40		
					13,14, 19	35		
					15-18	70		
			M,D,P, L,R, F,G, H	9 2/		3/		ns
Chip enable/select to end of write	t_{SLWH} t_{EHWH}			9,10,11	01,02, 05,06	55		ns
					09-12	50		
					03,04, 07,08	35		
					13,14	30		
					15-18	65		
					19	32		
			M,D,P, L,R, F,G, H	9 2/		3/		ns
Address setup to end of write	t_{AVWH}			9,10,11	01,02, 05,06	55		ns
					09-12	40		
					03,04, 07,08	35		
					13,14, 19	30		
					15-18	50		
			M,D,P, L,R, F,G, H	9 2/		3/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Address setup to start of write	t_{AVWL}			9,10,11	All	0		ns
			M,D,P,L,R,F,G,H	9 2/		3/		ns
Write pulse width	t_{WLWH}			9,10,11	01,02,05,06	55		ns
					03,04,07,08	35		
					09-12	40		
					13,14,19	30		
					15-18	50		
			M,D,P,L,R,F,G,H	9 2/		3/		ns
Address hold after end of Write	t_{WHAX}			9,10,11	All	0		ns
			M,D,P,L,R,F,G,H	9 2/		3/		ns
Write disable pulse width	t_{WHWL}			9,10,11	All	5		ns
			M,D,P,L,R,F,G,H	9 2/		3/		ns

1/ AC measurements assume transition times ≤ 2 ns/volt for device type 01 and ≤ 5 ns for all other device types. For output load circuit, see figure 4 and for timing waveforms, see figure 5.
2/ When performing postirradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C \pm 5°C$. The M, D, P, L, R, F, G, and H in the test condition column are the postirradiation limits for the device types specified in the device types column.
3/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
4/ $f_{MAX} = 1/t_{AVAV}$ (minimum). For devices 05-08 and 19 only, $f_{MAX} = 1/t_{AVAV}$ (minimum write cycle time).
5/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table IA.
6/ Transition is measured ±500 mV from steady-state voltage.
7/ Transition is measured ±400 mV from steady-state voltage.
8/ Outputs disabled for device types 05-12 and 15-19.

TABLE IB. SEP Test Limits 1/ 2/

Device Type	Memory pattern	$V_{CC} = 4.5\ V$ SEU rate 4/ Adam 90% environment	Bias $V_{CC} = 5.5\ V$ for latch-up (SEL)test No SEL occurs at effective LET = 5/
All	3/	1×10^{-10} upsets/bit-day	LET ≤ 120 MeV-cm^2/mg

See footnotes at end of table.

TABLE IB. SEP Test Limits – Continued. 1/ 2/

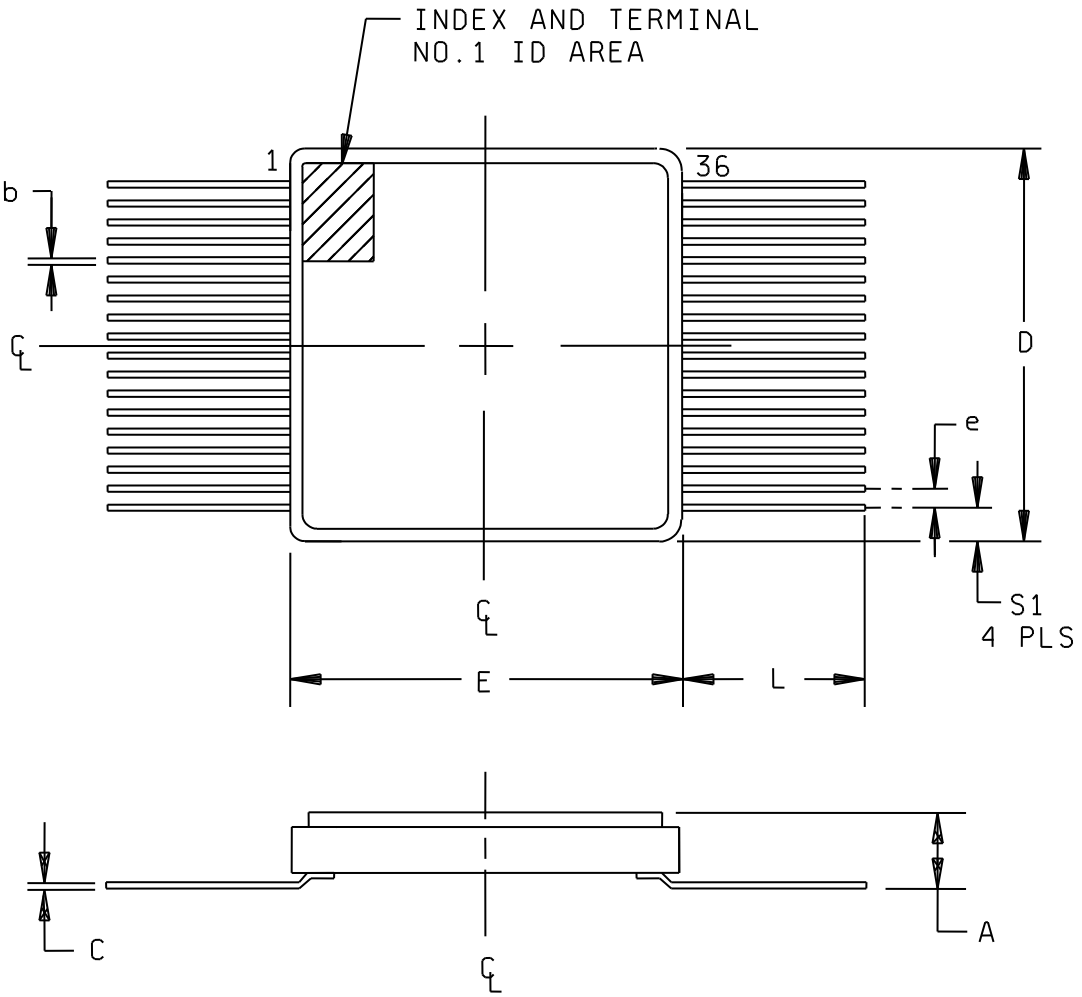
1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Testing shall be performed using checkerboard and checkerboard bar test patterns.
4/ Based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield using Weibull parameters derived from actual test data (see 4.4.4.4). Weibull parameters are available from the vendor to calculate projected upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).
5/ Worst case temperature T_A = +125°C + 10°C for SEL test.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1		1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1		1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ See 4.4.1d.
7/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1). For device class V performance of delta limits shall be as specified in the manufacturer's QM plan.

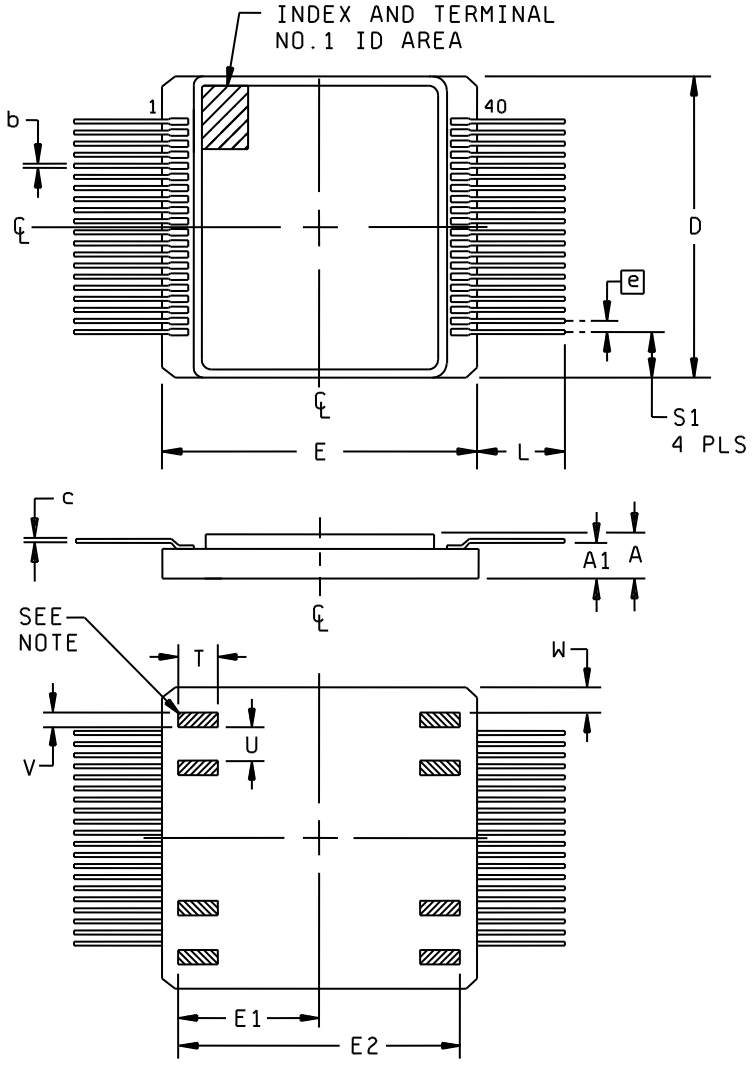
Case X



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.075	.125	1.91	2.41
b	.007	.010	.18	.25
S1	.103	.123	2.62	3.12
c	.004	.006	.11	.15
D	.640	.660	16.26	16.76
E	.623	.637	15.82	16.18
e	0.025 BSC		0.64 BSC	
L	.235	.300	5.96	7.24

FIGURE 1. Case outlines.

Case Y



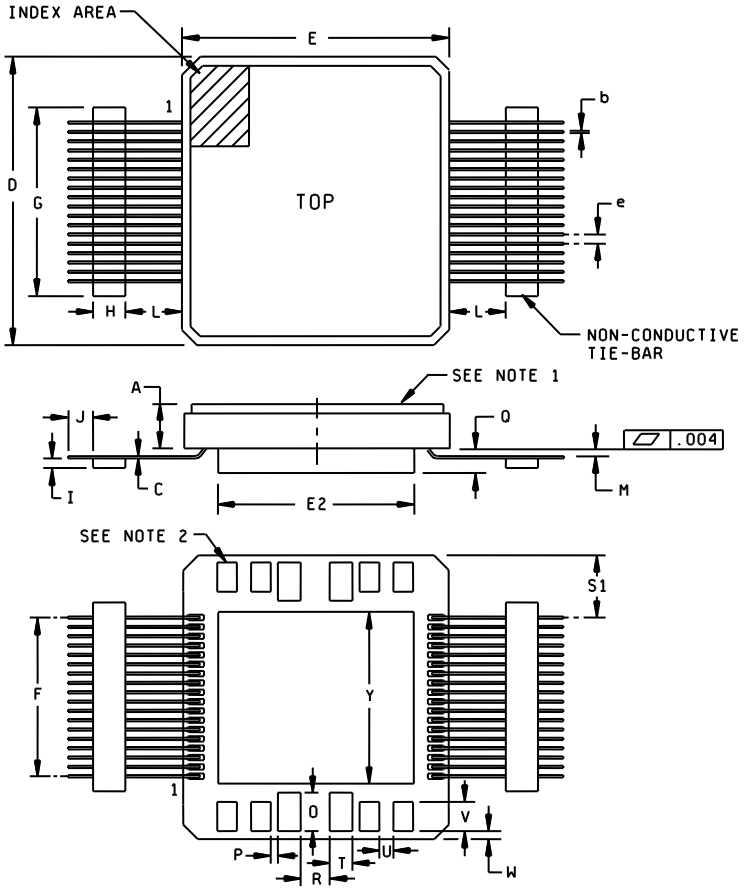
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.066	.078	1.68	1.98
A1	.060	.076	1.53	1.93
b	.007	.010	.18	.25
S1	.078	.098	1.98	2.48
c	.004	.006	.11	.15
D	.640	.660	16.26	16.76
E	.768	.783	19.48	19.88
E1	.350 REF		8.89 REF	

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
E2	.700 REF		17.78 REF	
e	0.025 BSC		0.64 BSC	
L	.238	.288	6.04	7.32
T	.100 REF		2.54 REF	
U	.080 REF		2.03 REF	
V	.040 REF		1.02 REF	
W	.045 REF		1.14 REF	

NOTE: The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P8.

FIGURE 1. Case outlines - Continued.

Case Z, 4



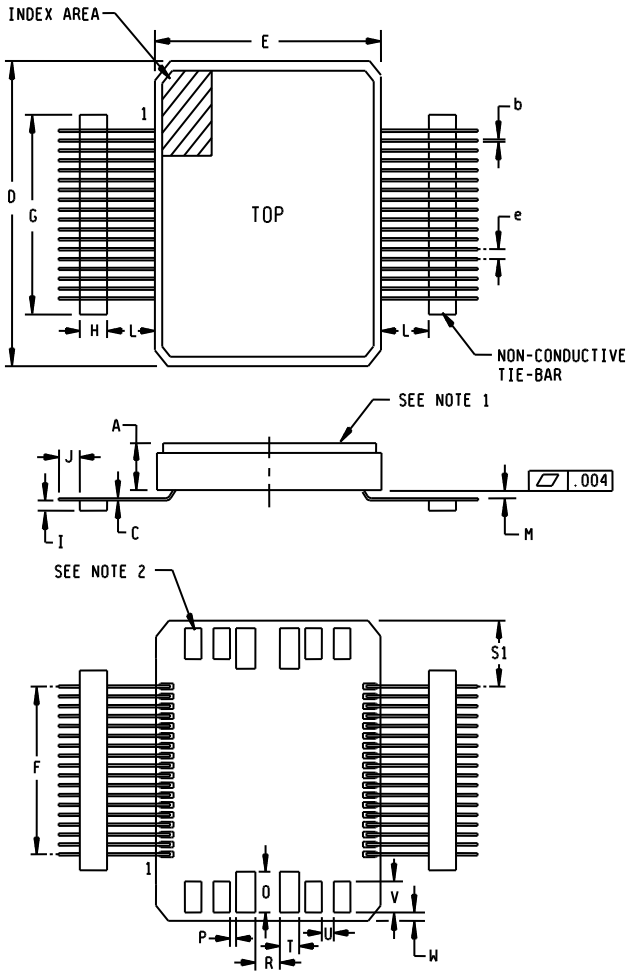
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.085	.105	2.16	2.67
b	.006	.010	.15	.25
C	.0050	.0075	.127	.191
D	.640	.660	16.26	16.76
E	.623	.637	15.82	16.18
E2	0.450 REF		11.43 REF	
e	0.025 BSC		0.64 BSC	
F	.420	.430	10.67	10.92
G	0.525 REF		13.34 REF	
H	0.135 REF		3.43 REF	
I	.025	.035	.64	.89
J	0.080 REF		2.03 REF	

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
L	.270	.300	6.86	7.62
M	.05	.011	.13	.28
O	0.090 REF		2.29 REF	
P	0.015 REF		0.38 REF	
Q	.040	.060	1.02	1.52
R	0.075 REF		1.91 REF	
S1	.103	.123	2.62	3.12
T	0.050 REF		1.27 REF	
U	0.030 REF		0.76 REF	
V	0.080 REF		2.03 REF	
W	0.005 REF		0.13 REF	
Y	0.400 REF		10.16 REF	

NOTES: 1. Lid tied to V_{SS}.
2. The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P12.

FIGURE 1. Case outlines - Continued.

Case U



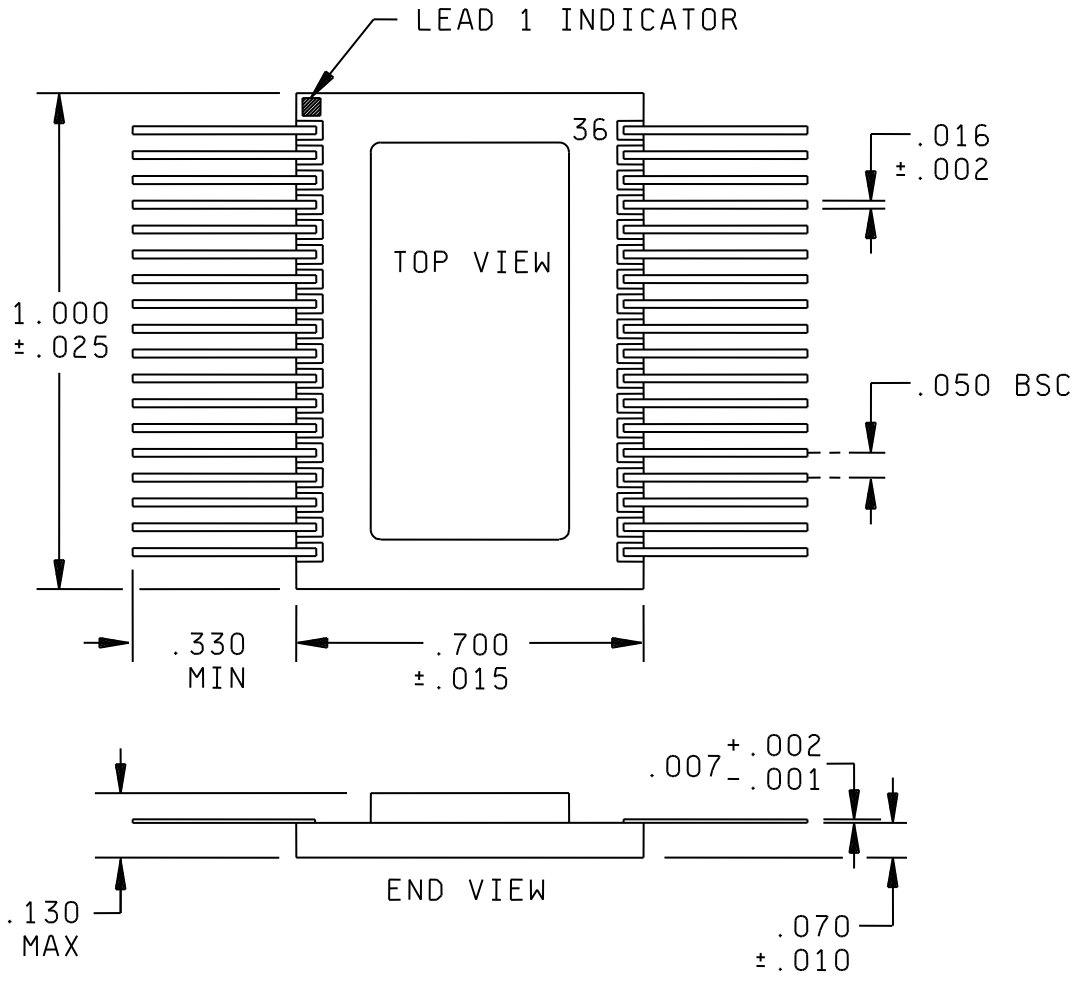
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.085	.105	2.16	2.67
b	.006	.010	.15	.25
C	.0050	.005	.127	.191
D	.640	.660	16.26	16.76
E	.623	.637	15.82	16.18
e	0.025 BSC		0.64 BSC	
F	.420	.430	10.67	10.92
G	0.525 REF		13.34 REF	
H	0.135 REF		3.43 REF	
I	.025	.035	.64	.89
J	0.080 REF		2.03 REF	

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
L	.270	.300	6.86	7.62
M	.005	.011	.13	.28
O	0.090 REF		2.29 REF	
P	0.015 REF		0.38 REF	
R	0.075 REF		1.91 REF	
S1	.103	.123	2.62	3.12
T	0.050 REF		1.27 REF	
U	0.030 REF		0.76 REF	
V	0.080 REF		2.03 REF	
W	0.005 REF		0.13 REF	

NOTES: 1. Lid tied to V_{SS}.
2. The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P12.

FIGURE 1. Case outlines - Continued.

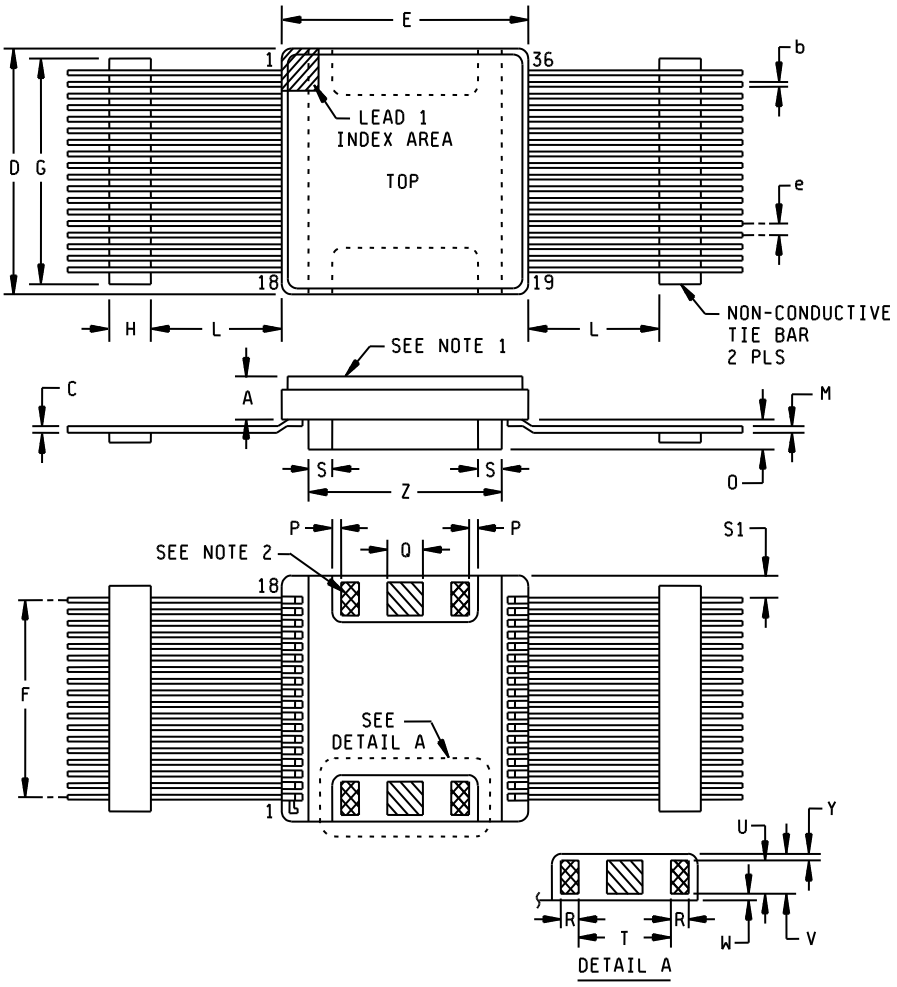
Case T



Inches	Millimeters
.001	.03
.002	.05
.007	.18
.010	.25
.015	.38
.016	.41
.025	.64
.050	1.27
.070	1.78
.130	3.30
.330	8.38
.700	17.78
1.000	25.40

FIGURE 1. Case outlines - Continued.

Case N



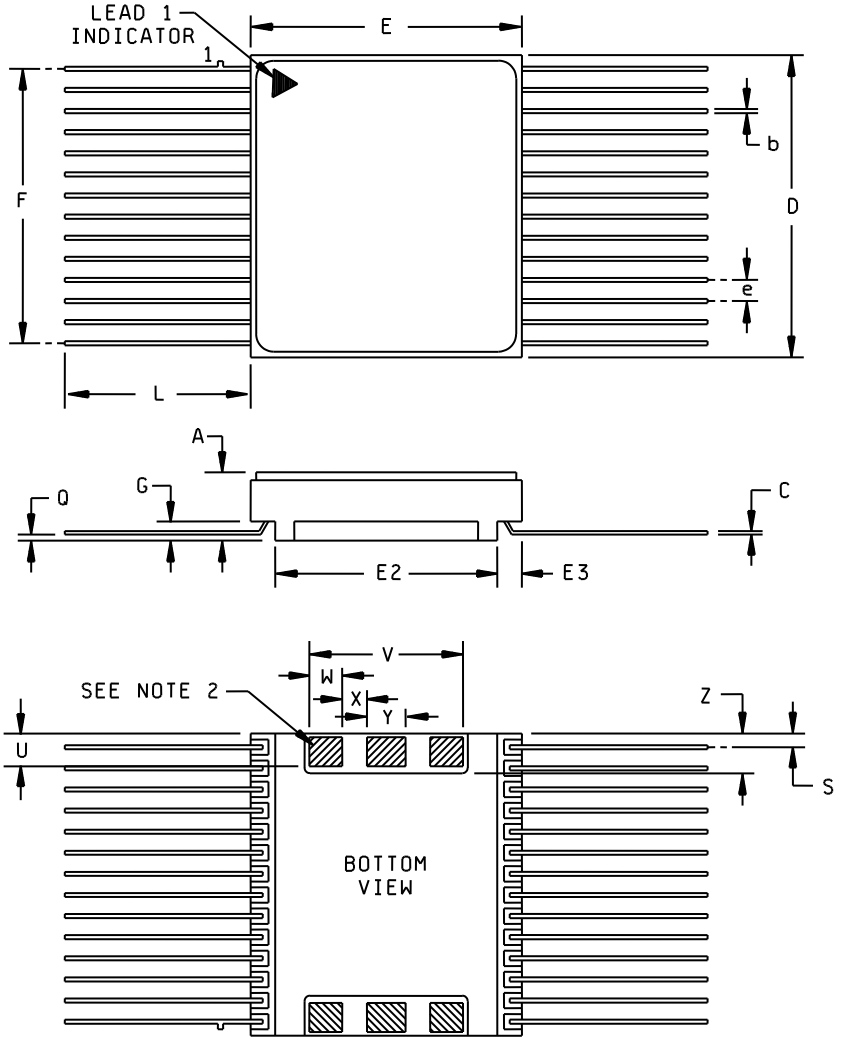
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.062	.082	1.57	2.09
b	.007	.010	.178	.254
C	.0050	.0075	.127	.191
D	.640	.660	16.26	16.76
E	.623	.637	15.82	16.18
e	0.025 BSC		0.64 BSC	
F	.421	.429	10.69	10.90
G	0.525 REF		13.34 REF	
H	0.135 REF		3.43 REF	
L	.270	.300	6.86	7.62

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
O	.045	.055	1.14	1.40
P	.010 REF		0.254 REF	
Q	.075	.085	1.91	2.15
R	0.040 REF		1.02 REF	
S	.070	.080	1.77	2.03
S1	.103	.123	2.62	3.12
T	0.240 REF		6.10 REF	
U	0.100 REF		2.54 REF	
V	0.115 REF		2.92 REF	
W	0.005 REF		0.13 REF	
Y	0.010 REF		0.25 REF	
Z	0.490 REF		12.45 REF	

NOTES: 1. Lid tied to V_{SS}.
2. The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P6.

FIGURE 1. Case outlines - continued.

Case 9



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.120	.150	3.05	3.81
b	.013	.017	0.33	0.43
C	.004	.009	0.10	0.23
D	.712	.728	18.08	18.49
e	0.050 BSC		1.27 BSC	
E	.522	.538	13.26	13.67
E2	.412	.428	10.46	10.87
E3	0.055 REF		13.97 REF	
F	.645	.655	16.38	16.64

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
G	.045	.055	1.14	1.40
L	.295	---	7.49	---
Q	.026	.045	0.66	1.14
S	.025	.045	0.64	1.14
V	0.300 REF		7.62 REF	
W	0.050 REF		1.27 REF	
X	0.030 REF		0.76 REF	
Y	0.100 REF		2.54 REF	
Z	0.080 REF		2.03 REF	

NOTES: 1. Lid tied to GND.
2. The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P6.

FIGURE 1. Case outlines - continued.

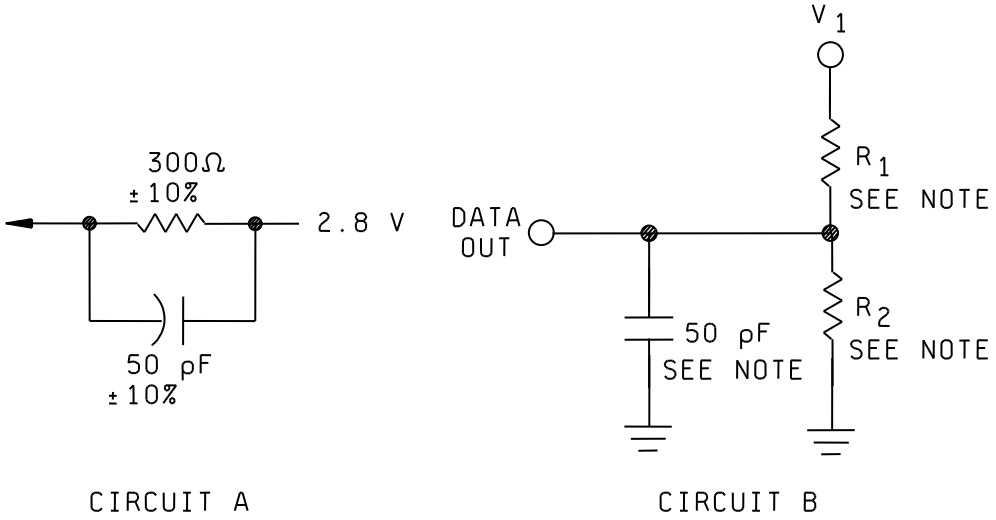
Device Type	All						
Case outline	Z, U	4	X, T	Y	M	N	9
Terminal no.	Terminal symbol						
1	GND	GND	GND	NC	A_{14}	GND	A_{14}
2	V_{CC}	V_{CC}	V_{CC}	GND	A_{12}	V_{CC}	A_{12}
3	A_{14}	A_{14}	A_1	V_{CC}	A_7	A_1	A_7
4	A_{12}	A_{12}	A_0	A_1	A_6	A_0	A_6
5	A_7	A_7	A_{10}	A_0	A_5	A_{10}	A_5
6	A_6	A_6	A_9	A_{10}	A_4	A_9	A_4
7	A_5	A_5	A_7	A_9	A_3	A_7	A_3
8	A_4	A_4	A_8	A_7	A_2	A_8	A_2
9	A_3	A_3	A_{11}	A_8	A_1	A_{11}	A_1
10	A_2	A_2	A_{12}	A_{11}	A_0	A_{12}	A_0
11	A_1	A_1	A_{13}	A_{12}	I/O_0	A_{13}	I/O_0
12	A_0	A_0	A_{14}	A_{13}	I/O_1	A_{14}	I/O_1
13	I/O_0	I/O_0	I/O_1	A_{14}	I/O_2	I/O_1	I/O_2
14	I/O_1	I/O_1	I/O_2	I/O_1	V_{SS}	I/O_2	GND
15	I/O_2	I/O_2	I/O_3	I/O_2	I/O_3	I/O_3	I/O_3
16	NC	NC	NC	I/O_3	I/O_4	NC	I/O_4
17	V_{CC}	V_{CC}	V_{CC}	NC	I/O_5	V_{CC}	I/O_5
18	GND	GND	GND	V_{CC}	I/O_6	GND	I/O_6
19	GND	GND	GND	GND	I/O_7	GND	I/O_7
20	V_{CC}	V_{CC}	V_{CC}	NC	$\overline{S}$	V_{CC}	$\overline{S}$
21	I/O_3	I/O_3	I/O_4	NC	A_{10}	I/O_4	A_{10}
22	I/O_4	I/O_4	I/O_5	GND	$\overline{G}$	I/O_5	$\overline{G}$
23	I/O_5	I/O_5	I/O_6	V_{CC}	A_{11}	I/O_6	A_{11}
24	I/O_6	I/O_6	I/O_7	I/O_4	A_9	I/O_7	A_9
25	I/O_7	I/O_7	I/O_8	I/O_5	A_8	I/O_8	A_8
26	$\overline{S}$	$\overline{S}$	$\overline{S}$	I/O_6	A_{13}	$\overline{S}$	A_{13}
27	A_{10}	A_{10}	A_2	I/O_7	$\overline{W}$	A_2	$\overline{W}$
28	$\overline{G}$	$\overline{G}$	$\overline{G}$	I/O_8	V_{CC}	$\overline{G}$	V_{CC}
29	A_{11}	A_{11}	A_6	$\overline{S}$	----	A_6	----
30	A_9	A_9	A_5	A_2	----	A_5	----
31	A_8	A_8	A_4	$\overline{G}$	----	A_4	----
32	A_{13}	E	A_3	A_6	----	A_3	----
33	E	$\overline{W}$	E	A_5	----	E	----
34	$\overline{W}$	A_{13}	$\overline{W}$	A_4	----	$\overline{W}$	----
35	V_{CC}	V_{CC}	V_{CC}	A_3	----	V_{CC}	----
36	GND	GND	GND	E	----	GND	----
37	----	----	----	$\overline{W}$	----	----	----
38	----	----	----	V_{CC}	----	----	----
39	----	----	----	GND	----	----	----
40	----	----	----	NC	----	----	----
P1	V_{CC}	V_{CC}	----	V_{CC}	----	V_{CC}	V_{CC}
P2	GND	GND	----	V_{CC}	----	GND	GND
P3	GND	GND	----	GND	----	V_{CC}	V_{CC}
P4	V_{CC}	V_{CC}	----	GND	----	V_{CC}	V_{CC}
P5	V_{CC}	V_{CC}	----	V_{CC}	----	GND	GND
P6	GND	GND	----	V_{CC}	----	V_{CC}	V_{CC}
P7	GND	GND	----	GND	----	----	----
P8	V_{CC}	V_{CC}	----	GND	----	----	----
P9	V_{CC}	V_{CC}	----	----	----	----	----
P10	GND	GND	----	----	----	----	----
P11	GND	GND	----	----	----	----	----
P12	V_{CC}	V_{CC}	----	----	----	----	----

FIGURE 2. Terminal connections.

Mode	Inputs (see notes 1 and 2)					Power
	E (see note 3)	$\overline{S}$	$\overline{W}$	$\overline{G}$	I/O	
WRITE	HIGH	LOW	LOW	DON'T CARE	DATA-IN	ACTIVE
READ	HIGH	LOW	HIGH	LOW	DATA-OUT	ACTIVE
STANDBY	DON'T CARE	HIGH	DON'T CARE	DON'T CARE	HIGH-Z	STANDBY
STANDBY (see note 4)	LOW	DON'T CARE	DON'T CARE	DON'T CARE	HIGH-Z	STANDBY

NOTES:
1. V_{IN} for Don't Care inputs = V_{IL} OR V_{IH}.
2. When $\overline{G}$ = high, I/O is High-Z.
3. E does not apply to devices in case outlines "M" or "9".
4. When in standby mode, $\overline{S}$ = V_{CC} and E = GND input levels to dissipate minimum standby power. All other input levels may float.

FIGURE 3. Truth table.



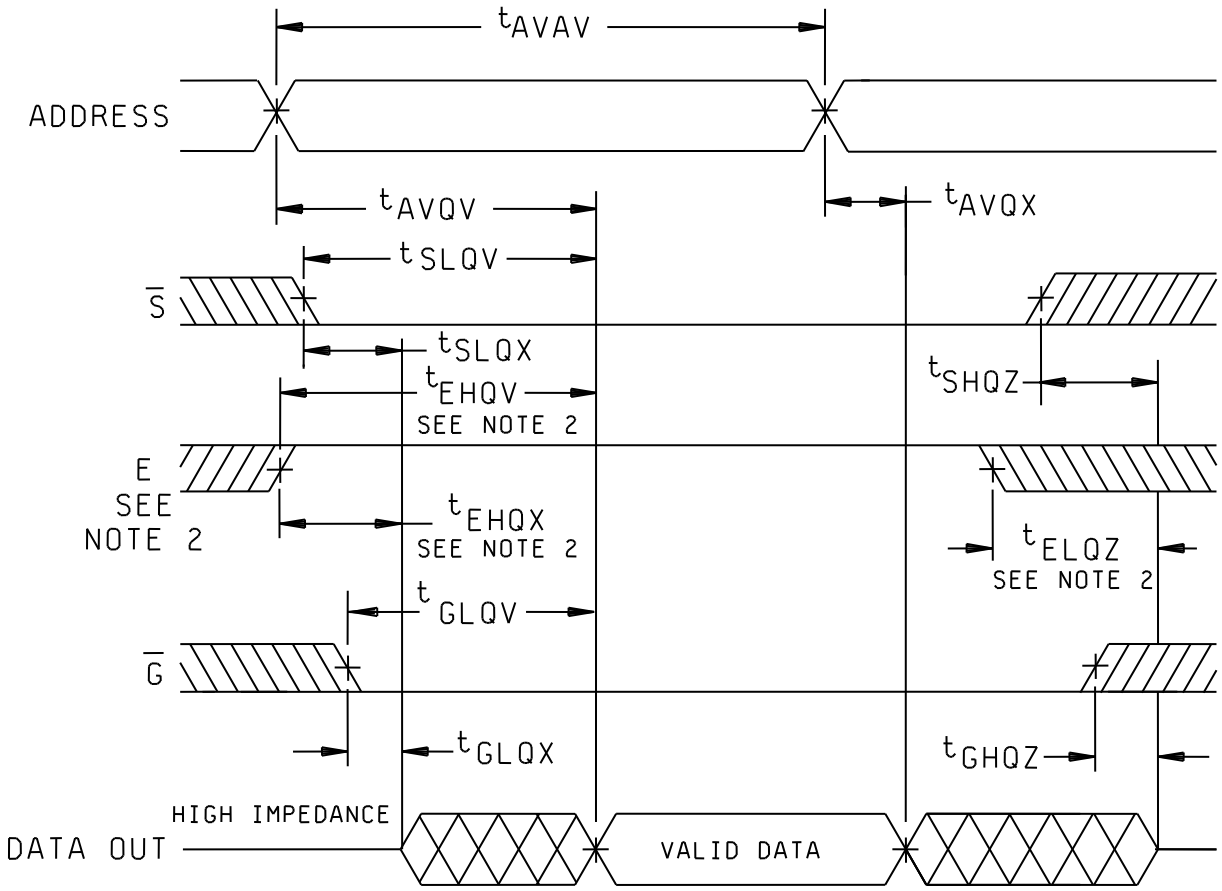
AC test conditions

	Device types		
	01,13	02,03,05,07,09,11,15,17,19	04,06,08,10,12,14,16,18
Input pulse levels	0.0 V to V_{CC}	0.5 V to V_{CC} - 0.5 V	0 V to 3 V
Input rise/fall times	≤ 2.0 ns/volt	≤ 5 ns	≤ 5 ns
Input timing reference	2.5 volts	V_{CC} / 2	1.5 V
Output timing reference	2.5 volts	V_{CC} / 2	1.5 V

NOTES: Capacitance includes scope and jig (minimum values). Circuit A applies to device types 01, 03, and 13. Circuit B applies to device types 02, 04, 09-12, and 14-18, with V_1 = 5.0 V, R_1 = 480 Ω, R_2 = 255 Ω. For device types 05-08 and 19, V_1 = 2.9 V, R_1 = 249 Ω, R_2 is open (no resistor).

FIGURE 4. Output load circuit (see note).

Read cycle (see note1)

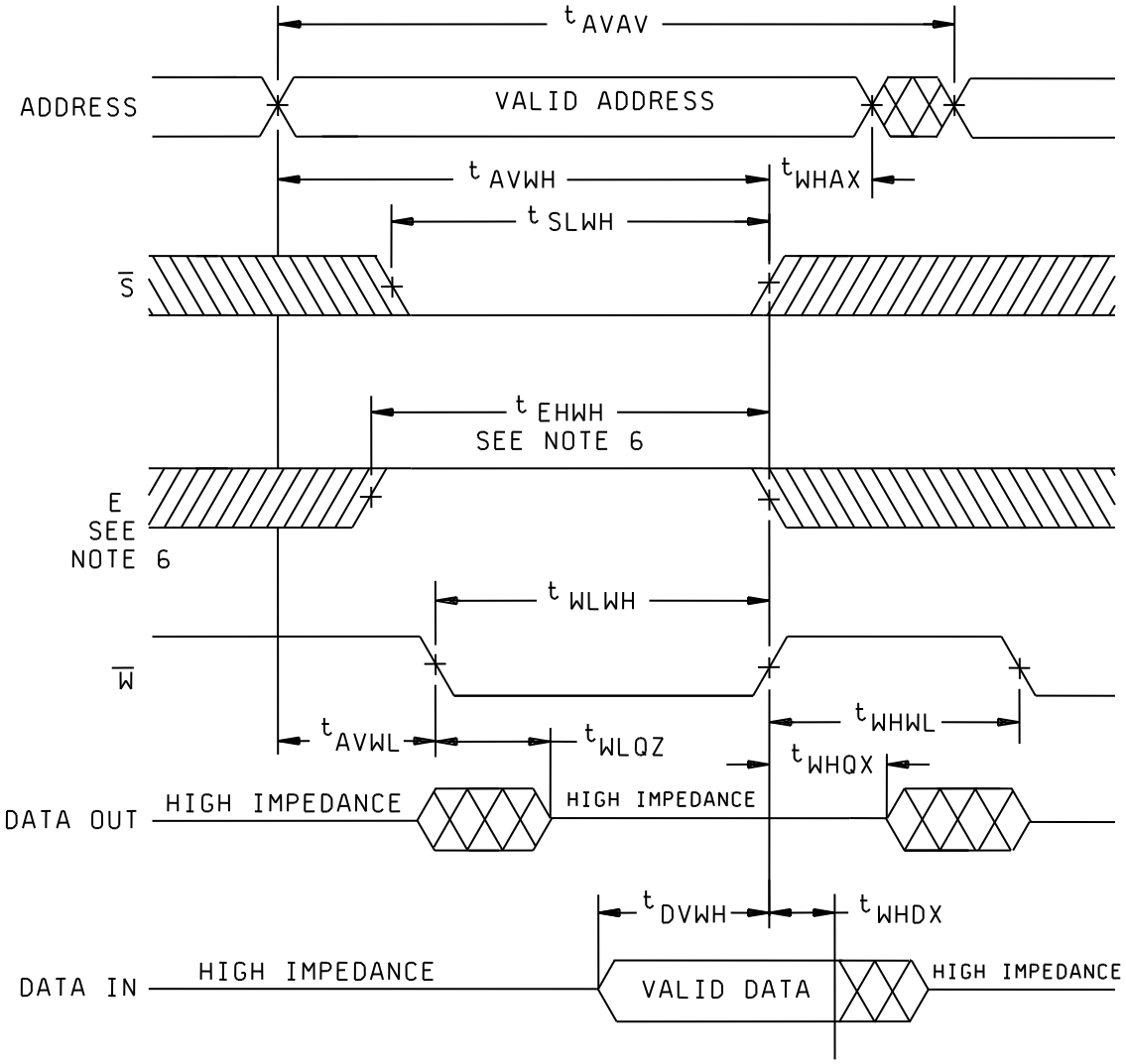


NOTE:

1. $\overline{W}$ is high for read cycle.
2. E and timing parameters t_{EHQV}, t_{EHQX}, t_{ELQZ} do not apply to devices in case outlines "M" or "9".

FIGURE 5. Timing waveforms.

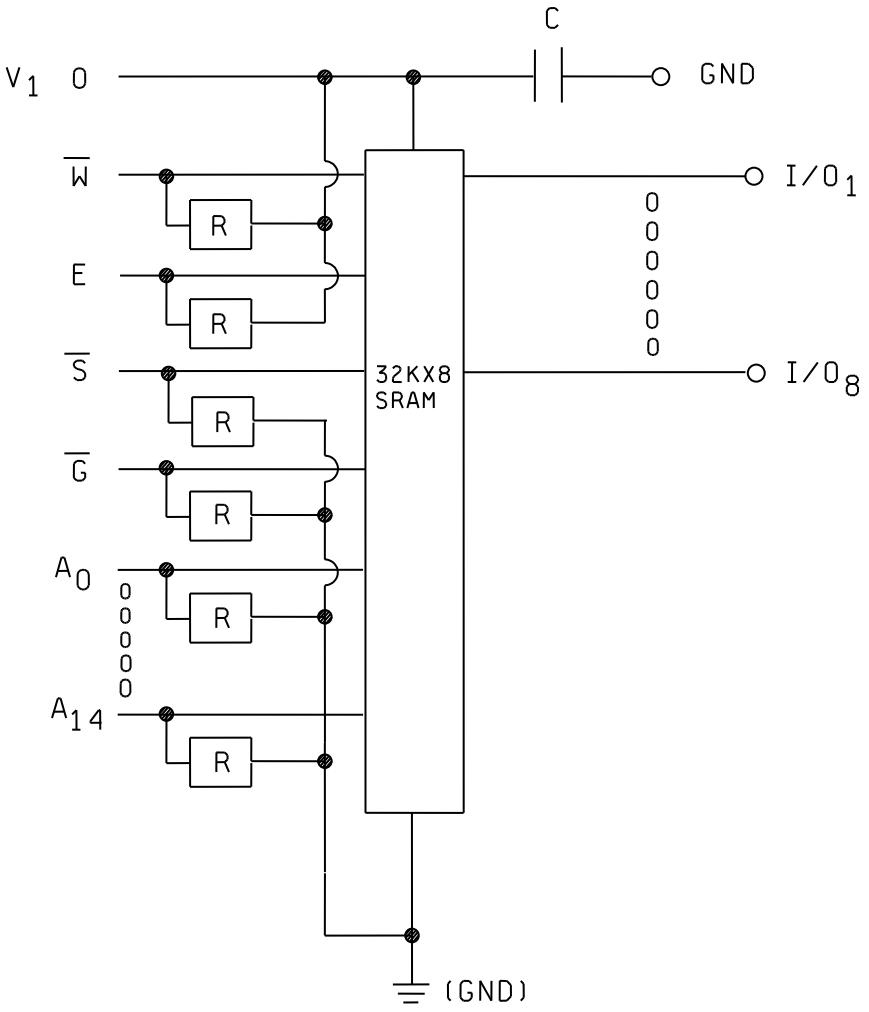
Write cycle (see notes 1, 2, 3, 4, and 5)



NOTES:

1. Write cycle data is latched by the first occurrence of $\overline{S}$ high, E low or $\overline{W}$ high.
2. $\overline{S}$ high, E low, or $\overline{W}$ high must occur while address transitions.
3. Write cycle time is guaranteed for toggling $\overline{S}$ and E or holding $\overline{S}$ or E, or both, in active state.
4. The worst case timing sequence of $t_{WLQZ} + t_{DVWH} + t_{WHWL}$ = the write cycle time (t_{AVAV}).
5. $\overline{G}$ high will eliminate the I/O output from becoming active (t_{WLQZ}).
6. E and timing parameter t_{EHWH} do not apply to devices in case outlines "M" or "9".

FIGURE 5. Timing waveforms - continued.



NOTES:

1. Power pins connected to V_1.
2. The absolute voltage ratings of 1.3 shall not be exceeded.
3. ESD precautions shall be followed.
4. The pattern in the memory array will be checkerboard for irradiation and accelerated anneaing tests.
5. Pin conditions (E does not apply to devices in case outlines "M" or "9") :

$\overline{S}$ = GND	$\overline{W}$ = V_{CC}	$\overline{G}$ = GND
E = V_{CC}	A_0 - A_{14} = GND	I/O_1 - I/O_8 = FLOATING
V_1 = V_{CC}	R = 10 kΩ ± 10%	C = 0.1 μF ± 10%
V_{CC} = 5.0 V		

FIGURE 6. Radiation exposure circuit. (see notes)

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing shall be performed on all devices requiring a RHA level greater than 5K rads(Si). The post-anneal end point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may effect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the SEC or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 102 and 105 ion/cm2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latchup measurements.

g. For SEP test limits see table IB herein.

4.4.4.3 Dose rate induced latch-up testing. When specified by the procuring activity, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. When specified by the procuring activity, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein (see 1.6). All device classes must meet the post irradiation end-point electrical parameter limits as defined in Table IA, for the subgroups specified in Table IIA herein at T_A = +25°C ± 5°C after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and herein:

C_{IN}, C_{OUT} ..... Input and bidirectional output capacitance, terminal-to-GND.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{IL} ..... Input current low.
I_{IH} ..... Input current high.
T_C ..... Case temperature.
T_A ..... Ambient temperature.
V_{CC} ..... Positive supply voltage.
O/V ..... Latch-up over-voltage.
O/I ..... Latch-up over-current.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEU).

d. Number of transients (SET).

e. Occurrence of latchup (SEL).

APPENDIX A

Appendix A forms a part of SMD 5962-92153

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for, each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.2.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.

A.3.2.1 XY March – Continued.

Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-06-11

Approved sources of supply for SMD 5962-92153 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9215301QNC	3/	LOR2568C-Q60I
5962H9215301QXC	3/	LOR2568C-Q60X
5962H9215301QYC	3/	LOR2568C-Q60Y
5962H9215301VNC	3/	LOR2568C-V60I
5962H9215301VXC	3/	LOR2568C-V60X
5962H9215301VYC	3/	LOR2568C-V60Y
5962H9215302QNC	3/	LOR2568T-Q60I
5962H9215302QXC	3/	LOR2568T-Q60X
5962H9215302QYC	3/	LOR2568T-Q60Y
5962H9215302QZA	3/	2568T60
5962H9215302VNC	3/	LOR2568T-V60I
5962H9215302VXC	3/	LOR2568T-V60X
5962H9215302VYC	3/	LOR2568T-V60Y
5962H9215302VZA	3/	2568T60
5962H9215303QMA	3/	UT7156C40PCAH
5962H9215303QMC	3/	UT7156C40PCCH
5962H9215303QNC	3/	LOR2568C-Q40I
5962H9215303QTA	3/	UT7156C40WCAH
5962H9215303QTC	3/	UT7156C40WCCH
5962H9215303QXC	3/	LOR2568C-Q40X
5962H9215303QYC	3/	LOR2568C-Q40Y
5962H9215303QZA	3/	2568C40
5962H9215303VMA	3/	UT7156C40PCAH
5962H9215303VMC	3/	UT7156C40PCCH
5962H9215303VNC	3/	LOR2568C-V40I
5962H9215303VTA	3/	UT7156C40WCAH
5962H9215303VTC	3/	UT7156C40WCCH
5962H9215303VXC	3/	LOR2568C-V40X
5962H9215303VYC	3/	LOR2568C-V40Y
5962H9215303VZA	3/	2568C40
5962H9215304QNC	3/	LOR2568T-Q40I
5962H9215304QXC	3/	LOR2568T-Q40X
5962H9215304QYC	3/	LOR2568T-Q40Y
5962H9215304QZA	3/	2568T40

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9215304VNC	3/	LOR2568T-V40I
5962H9215304VXC	3/	LOR2568T-V40X
5962H9215304VYC	3/	LOR2568T-V40Y
5962H9215305Q4C	3/	HC6856/2XQHZC
5962H9215305Q9C	3/	HC6856/1NQHZC
5962H9215305QMC	3/	HC6856/1RQHZC
5962H9215305QUC	3/	HC6856/1WQHZC
5962H9215305QZC	3/	HC6856/1XQHZC
5962H9215305V4C	3/	HC6856/2XVHZC
5962H9215305V9C	3/	HC6856/1NVHZC
5962H9215305VMC	3/	HC6856/1RVHZC
5962H9215305VUC	3/	HC6856/1WVHZC
5962H9215305VZC	3/	HC6856/1XVHZC
5962H9215306Q9C	3/	HC6856/1NQHZT
5962H9215306QMC	3/	HC6856/1RQHZT
5962H9215306QUC	3/	HC6856/1WQHZT
5962H9215306QZC	3/	HC6856/1XQHZT
5962H9215306VMC	3/	HC6856/1RVHZT
5962H9215306VUC	3/	HC6856/1WVHZT
5962H9215306VZC	3/	HC6856/1XVHZT
5962H9215307Q4C	3/	HC6856/2XQHAC
5962H9215307Q9C	3/	HC6856/1NQHAC
5962H9215307QMC	3/	HC6856/1RQHAC
5962H9215307QUC	3/	HC6856/1WQHAC
5962H9215307V4C	3/	HC6856/2XVHAC
5962H9215307V9C	3/	HC6856/1NVHAC
5962H9215307VMC	3/	HC6856/1RVHAC
5962H9215307VUC	3/	HC6856/1WVHAC
5962H9215307VZC	3/	HC6856/1XVHAC
5962H9215308Q9C	3/	HC6856/1NQHAT
5962H9215308QMC	3/	HC6856/1RQHAT
5962H9215308QUC	3/	HC6856/1WQHAT
5962H9215308QZC	3/	HC6856/1XQHAT
5962H9215308V9C	3/	HC6856/1NVHAT
5962H9215308VMC	3/	HC6856/1RVHAT
5962H9215308VUC	3/	HC6856/1WVHAT
5962H9215308VZC	3/	HC6856/1XVHAT
5962H9215309QMA	3/	UT7156C55PBAH

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9215309QMC	3/	UT7156C55PBCH
5962H9215310QMA	3/	UT7156T55PBAH
5962H9215310QMC	3/	UT7156T55PBCH
5962H9215311QTA	3/	UT7156C55WBAH
5962H9215311QTC	3/	UT7156C55WBCH
5962H9215312QTA	3/	UT7156T55WBAH
5962H9215312QTC	3/	UT7156T55WBCH
5962H9215313QNC	3/	LOR2568C-Q30I
5962H9215313QXC	3/	LOR2568C-Q30X
5962H9215313QYC	3/	LOR2568C-Q30Y
5962H9215313VNC	3/	LOR2568C-V30I
5962H9215313VXC	3/	LOR2568C-V30X
5962H9215313VYC	3/	LOR2568C-V30Y
5962H9215314QNC	3/	LOR2568T-Q30I
5962H9215314QXC	3/	LOR2568T-Q30X
5962H9215314QYC	3/	LOR2568T-Q30Y
5962H9215314VNC	3/	LOR2568T-V30I
5962H9215314VXC	3/	LOR2568T-V30X
5962H9215314VYC	3/	LOR2568T-V30Y
5962H9215319QZC	34168	HC6856/1XQHCC
5962H9215319VZC	34168	HC6856/1XVHCC
5962R9215305Q4C	3/	HC6856/2XQRZC
5962R9215305QUC	3/	HC6856/1WQRZC
5962R9215305QZC	3/	HC6856/1XQRZC
5962R9215305V4C	3/	HC6856/2XVRZC
5962R9215305VUC	3/	HC6856/1WVRZC
5962R9215305VZC	3/	HC6856/1XVRZC
5962R9215306QUC	3/	HC6856/1WQRZT
5962R9215306QZC	3/	HC6856/1XQRZT
5962R9215306VUC	3/	HC6856/1WVRZT
5962R9215306VZC	3/	HC6856/1XVRZT
5962R9215307Q4C	3/	HC6856/2XQRAC
5962R9215307QUC	3/	HC6856/1WQRAC
5962R9215307QZC	3/	HC6856/1XQRAC
5962R9215307V4C	3/	HC6856/2XVRAC
5962R9215307VUC	3/	HC6856/1WVRAC
5962R9215307VZC	3/	HC6856/1XVRAC
5962R9215308QUC	3/	HC6856/1WQRAT

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9215308QZC	3/	HC6856/1XQRAT
5962R9215308VUC	3/	HC6856/1WVRAT
5962R9215308VZC	3/	HC6856/1XVRAT
5962R9215309QMA	3/	UT7156C55PBAR
5962R9215309QMC	3/	UT7156C55PBCR
5962R9215310QMA	3/	UT7156T55PBAR
5962R9215310QMC	3/	UT7156T55PBCR
5962R9215311QTA	3/	UT7156C55WBAR
5962R9215311QTC	3/	UT7156C55WBCR
5962R9215312QTA	3/	UT7156T55WBAR
5962R9215312QTC	3/	UT7156T55WBCR
5962R9215315QMA	3/	UT7156C70PBAR
5962R9215315QMC	3/	UT7156C70PBCR
5962R9215316QMA	3/	UT7156T70PBAR
5962R9215316QMC	3/	UT7156T70PBCR
5962R9215317QTA	3/	UT7156C70WBAR
5962R9215317QTC	3/	UT7156C70WBCR
5962R9215318QTA	3/	UT7156T70WBAR
5962R9215318QTC	3/	UT7156T70WBCR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34168	Honeywell SSEC MN14-3C12 12001 Hwy 55 West Plymouth, MN 55441