ERROR FLAG OUTPUT TRUTH TABLE

Inputs		Internal To Device	Outputs Pre-State	Output	Function
$\overline{CLR}$	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
H	⌐	H	H	H	Sample
H	⌐	–	L	L	(1's
H	⌐	L	–	L	Capture)
L	–	–	–	H	Clear

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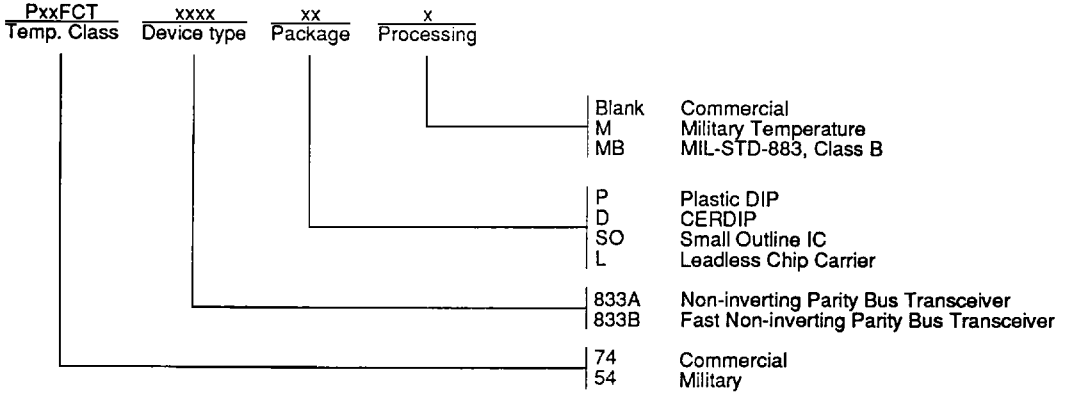
Notes:
1. $\overline{OE}_T$ is HIGH and $\overline{OE}_R$ is LOW.
2. H = High
   L = Low
   – = Don't care or irrelevant
   ⌐ = Low to High transition of clock

ORDERING INFORMATION



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PIN DESCRIPTION

Pin No.	Name	I/O	Description
1	$\overline{OE}_R$	I	RECEIVE enable input.
2–9	R_i	I/O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O Open Drain	Output from fault registers. Registers detection of odd parity fault on using clock edge (CLK). A registered $\overline{ERR}$ output remains low until cleared. Open drain output, requires pull up resistor.
11	$\overline{CLR}$	O	Clears the fault register output.
16–23	T_i	I/O	8-bit TRANSMIT data output.
15	PARITY	I/O	1-bit PARITY output.
14	$\overline{OE}_T$	I	TRANSMIT enable input.
13	CLK	I	External clock pulse input for fault register flag.

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FUNCTION TABLE

Inputs						Outputs				Function
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_i (Σ of H'S)	T_i Incl PARITY (Σ of H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	H	⌐	H (Odd)	NA	NA	H	L	H	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	H	⌐	H (Even)	NA	NA	H	H	L	
L	H	H	⌐	L (Odd)	NA	NA	L	L	H	
L	H	H	⌐	L (Even)	NA	NA	L	H	L	
H	L	H	⌐	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	⌐	NA	H (Even)	H	NA	NA	L	
H	L	H	⌐	NA	L (Odd)	L	NA	NA	H	
H	L	H	⌐	NA	L (Even)	L	NA	NA	L	
–	–	L	–	–	–	NA	NA	NA	H	Clear the state of error flag register.
H	H	H	H or L	–	–	Z	Z	Z	•	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	–	–	–	Z	Z	Z	H	
H	H	H	⌐	H or L (Odd)	–	Z	Z	Z	H	
H	H	H	⌐	Hor L (Even)	–	Z	Z	Z	L	
L	L	H	⌐	H (Odd)	NA	NA	H	H	L	Forced-error checking.
L	L	H	⌐	H (Even)	NA	NA	H	L	H	
L	L	H	⌐	L (Odd)	NA	NA	L	H	L	
L	L	H	⌐	L (Even)	NA	NA	L	L	H	

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H = High
L = Low
NC = No Change
Z = High Impedance
NA = Not Applicable
$\overline{ERR}_{n-1}$ = Pre-state of $\overline{ERR}$
– = Don't care or irrelevant
Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7
⌐ = Low to High transition of clock
• = No change to stored Error State

Note:
1. Output state assumes HIGH output pre-state.

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DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.001	0.5	mA	V_{CC} = MAX, f_1 = 0, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 2.7V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 2.7V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

Inputs			Outputs 'FCT11374
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

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H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH clock transition
Z = HIGH Impedance

AC CHARACTERISTICS

Symbol	Parameter	'FCT11374				Units	Fig. No.
		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	1.5	5.3	1.5	4.5	ns	1 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	5.4	1.5	5.0	ns	1 7 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.1	1.5	4.5	ns	

Note:
1. AC Characteristics guaranteed with C_L = 50 pF as shown in Figure 1.

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AC OPERATING REQUIREMENTS

Symbol	Parameter	'FCT11374				Units	Fig. No.
		MIL		COM'L			
		Min.[1]	Max.	Min.	Max.		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n TO CP	2.0	—	1.5	—	ns	9
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	1.5	—	1.0	—		
$t_w(H)$ $t_w(L)$	Clock Pulse Width[2], HIGH or LOW	5.0	—	4.0	—	ns	5

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. With one data channel toggling, $t_w(L) = t_w(H) = 2.0$ns and $t_r = t_f = 1.0$ns.

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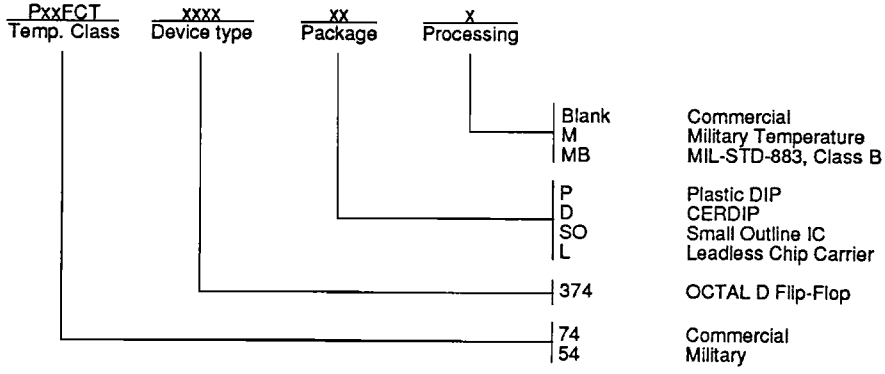
ORDERING INFORMATION



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