TOSHIBA MOS MEMORY PRODUCTS

TC55258PL-10/PL-12/PL-15
TC55258FL-10/FL-12/FL-15

DESCRIPTION

TC55258PL/FL is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a operating current of 5mA/MHz (Typ.) and minimum cycle time of 100ns. The TC55258PL/FL has two control inputs. Two chip enable inputs ($\overline{CE1}$, CE2) allow for device selection and data retention control. When device is placed in standby mode with chip off state, standby current is typically 0.01μA. Thus the TC55258PL/FL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. Ultra low standby power allow not only battery but capacitance back up. The TC55258PL/FL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out line plastic flat package.

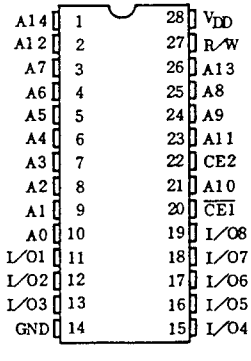
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Typ.) Operating
- Standby Current
  0.2μA(MAX.) at Ta=25°C
  1.0μA(MAX.) at Ta=60°C
  10.0μA(MAX.) at Ta=85°C
- 5V Single Power Supply
- Fully Static Operation
- Data Retention Supply Voltage
  : 2.0 ∿ 5.5V
- Access Time

	TC55258PL -10/FL-10	TC55258PL -12/FL-12	TC55258PL -15/FL-15
Access Time	100ns	120ns	150ns
$\overline{CE1}$ Access Time	100ns	120ns	150ns
CE2 Access Time	100ns	120ns	150ns

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP and Plastic Flat Package
- Wide Temperature Operation: -40 ∿ 85°C

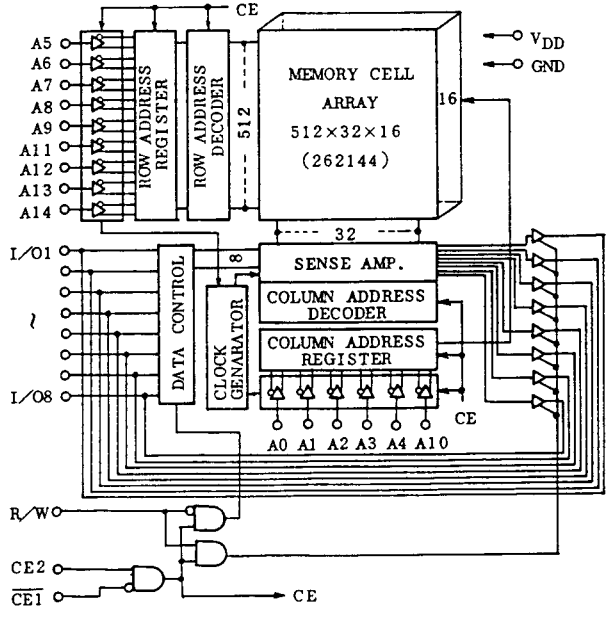
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ∿ I/O8	Data Inputs/Outputs
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	R/W	I/O1 ~ I/O8	POWER
Read	L	H	H	D_{OUT}	I_{DDO}
Write	L	H	L	D_{IN}	I_{DDO}
Standby	*	L	*	High-Z	I_{DDS}
	H	*	*	High-Z	I_{DDS}

*) H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~ V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{solder}	Soldering Temperature	260 · 10	°C·sec
T_{strg}	Storage Temperature	-55 ~ 150	°C
T_{opr}	Operating Temperature	-40 ~ 85	°C

*) -3.0V at pulse width 50ns
**) Flat package

D.C. and RECOMMENDED OPERATING CONDITIONS (Ta=-40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3 *	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

*) -3.0V at pulse width 50ns

D.C. and OPERATING CHARACTERISTICS (Ta=-40 ∿ 85°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IN}	Input Leakage Current	V_{IN}=0 ∿ V_{DD}		-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V		-1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		4.0	-	-	mA
V_{OH}	Output High Voltage	I_{OH}=-20μA		V_{DD}-0.1	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=20μA		-	-	0.1	V
I_{LO}	Output Leakage Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or R/W=V_{IL} V_{OUT}=0 ∿ V_{DD}		-	-	±1.0	μA
I_{DDO1}	Operating Current (Read Cycle)*	V_{DD}=5.5V, $\overline{CE1}$=V_{IL}	t_{cycle}=1μs	-	10	-	mA
		CE2=V_{IH}, R/W=V_{IH} I_{OUT}=0mA Other Input= V_{IL}/V_{IH}	t_{cycle}= Min. cycle	-	-	70	
I_{DDO2}		V_{DD}=5.5V, $\overline{CE1}$=0.2V	t_{cycle}=1μs	-	5	-	mA
		CE2=V_{DD}-0.2V R/W=V_{DD}-0.2V Other Input= V_{DD}-0.2V/0.2V I_{OUT}=0mA	t_{cycle}= Min. cycle	-	-	60	
I_{DDS1}	Standby Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		-	-	3	mA
I_{DDS2}	Standby Current	$\overline{CE1}$=V_{DD}-0.2V or CE2=0.2V V_{DD}=2.0 ∿ 5.5V	Ta=25°C	-	0.01	0.2	μA
			Ta=60°C	-	-	1.0	
			Ta=85°C	-	-	10.0	

* Assuming that R/W is Low for Write Cycle, the current consumption is twice as much as that when R/W is high for Write Cycle.

CAPACITANCE (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=-40 ~ 85°C, V_{DD}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TC55258PL -10/FL-10		TC55258PL -12/FL-12		TC55258PL -15/FL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	120	-	150	-	ns
t_{ACC}	Address Access Time	-	100	-	120	-	150	
t_{CO1}	$\overline{CE1}$ Access Time	-	100	-	120	-	150	
t_{CO2}	CE2 Access Time	-	100	-	120	-	150	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	5	-	5	-	5	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	-	50	-	60	-	70	
t_{OH}	Output Data Hold Time	10	-	10	-	10	-	

WRITE CYCLE

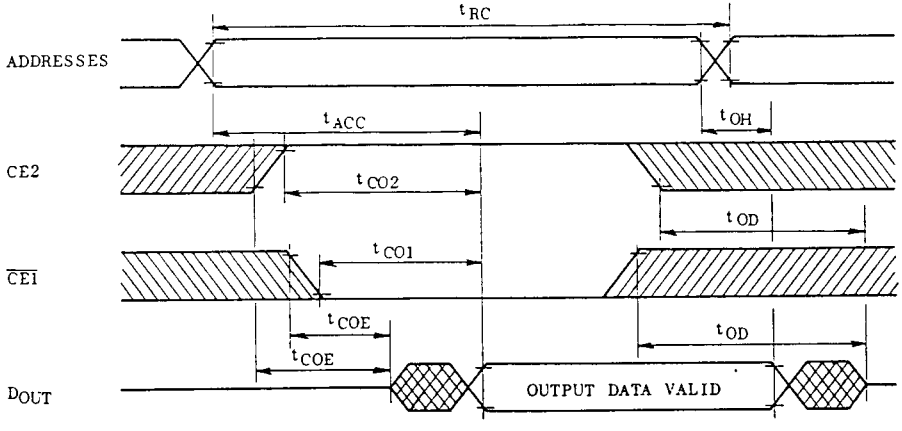
SYMBOL	PARAMETER	TC55258PL -10/FL-10		TC55258PL -12/FL-12		TC55258PL -15/FL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	120	-	150	-	ns
t_{WP}	Write Pulse Width	70	-	80	-	100	-	
t_{CW}	Chip Selection to End of Write	90	-	100	-	120	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{ODW}	R/W to Output in High-Z	-	50	-	60	-	70	
t_{OEW}	R/W to Output in Low-Z	5	-	5	-	5	-	
t_{DS}	Data Set Up Time	40	-	50	-	60	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITION

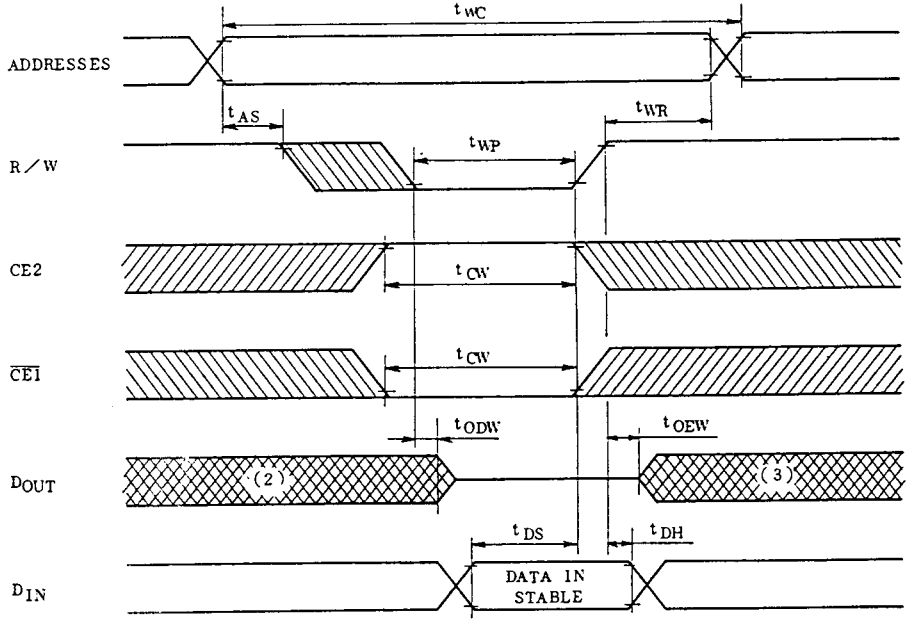
- Input Pulse Levels : 2.4V/0.6V
- Timing Measurement Reference Levels: 2.2V/0.8V
- Output Reference Levels : 2.2V/0.8V
- Input Pulse Rise and Fall Time : 5ns
- Output Load : 100pF + 1 TTL Gate

TIMING WAVEFORMS

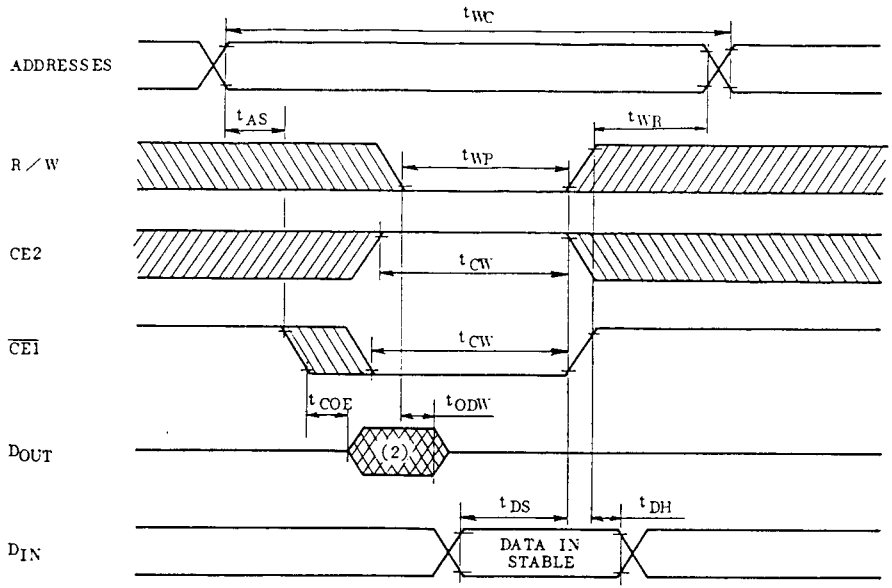
READ CYCLE (1)



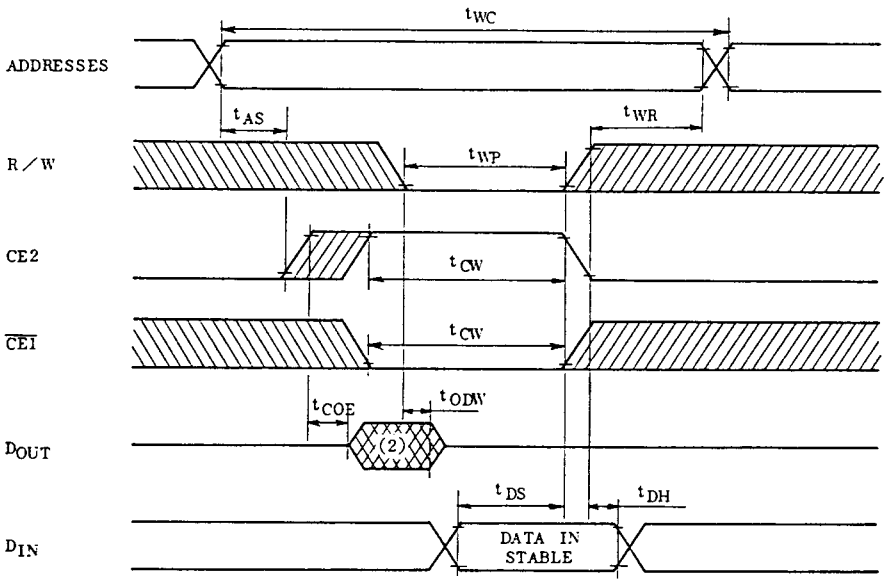
WRITE CYCLE 1 (R/W Controlled Write)



WRITE CYCLE 2 ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (CE2 Controlled Write)



NOTE:

(1) R/W is High for Read Cycle.

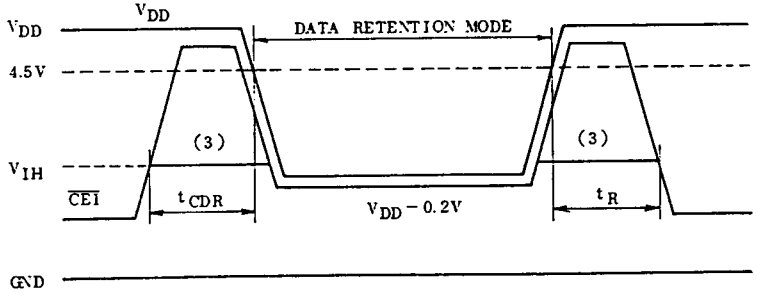
(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

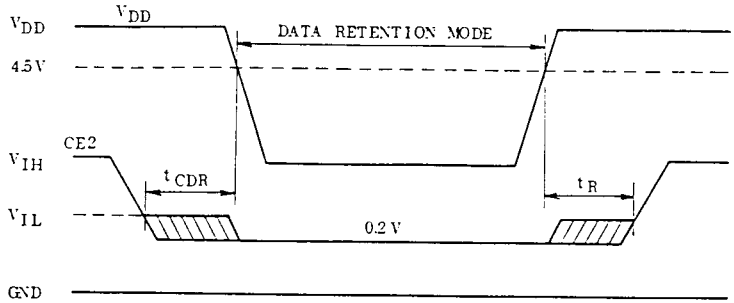
DATA RETENTION CHARACTERISTICS (Ta=-40 ~ 85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	Ta=25°C	-	0.01	0.2	μA
		Ta=60°C	-	-	1.0	
		Ta=85°C	-	-	10.0	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μs
t_R	Recovery Time		t_{RC}(1)	-	-	

$\overline{CE1}$ Controlled Data Retention Mode (2)



CE2 Controlled Data Retention Mode (4)



NOTE: (1) t_{RC}: Read Cycle Time

(2) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $\overline{CE1} \geqq V_{DD}-0.2V$.

(3) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

(4) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V.

3V OPERATION SPECIFICATION

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=-10 ~ 60°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	2.7	-	5.5	V
V_{IH}	Input High Voltage	V_{DD}-0.2	-	V_{DD}	
V_{IL}	Input Low Voltage	0	-	0.2	

D.C. and OPERATING CHARACTERISTICS (Ta=-10 ~ 60°C, V_{DD}=2.7V ~ 5.5V)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.*	MAX.	UNIT
I_{IN}	Input Leakage Current	V_{IN}=0 ~ V_{DD}		-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=V_{DD}-0.2V		-100	-	-	μA
I_{OL}	Output Low Current	V_{OL}=0.2V		100	-	-	μA
V_{OH}	Output High Current	I_{OH}=-20μA		V_{DD}-0.1	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=20μA		-	-	0.1	V
I_{LO}	Output Leakage Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or R/W=V_{IL} V_{OUT}=0 ~ V_{DD}		-	-	±1.0	μA
I_{DDO}**	Operation Current	$\overline{CE1}$=V_{IL}, CE2=V_{IH} R/W=V_{IH} Other Input= V_{DD}-0.2V/0.2V I_{OUT}=0mA	t_{cycle}=1μs	-	3.0	5.0	mA
I_{DDS}	Standby Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL}	Ta=25°C	-	0.01	0.2	μA
			Ta=60°C	-	-	1.0	

All voltage is measured from GND.

* V_{DD}=3V, Ta=25°C. This value shows with typical lot and reference only.

** I_{DDO} is slightly depending on input pulse t_r, t_f. If long t_r, t_f pulse is applied, there are some transient current at input stage. These specification is guaranteed with t_r, t_f < 20ns.

3V OPERATION SPECIFICATION

A.C. CHARACTERISTICS ($Ta=-10 \sim 60°C$, $V_{DD}=2.7V \sim 5.5V$)

READ CYCLE

SYMBOL	PARAMETER	MIN.	TYP.*	MAX.	UNIT
t_{RC}	Read Cycle Time	1000	-	-	ns
t_{ACC}	Address Access Time	-	300	1000	
t_{CO1}	$\overline{CE1}$ Access Time	-	300	1000	
t_{CO2}	CE2 Access Time	-	300	1000	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	5	-	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	-	-	200	
t_{OH}	Output Data Hold Time	10	-	-	

* $V_{DD}=3V$, $Ta=25°C$. This value shows with typical lot, and reference only.

WRITE

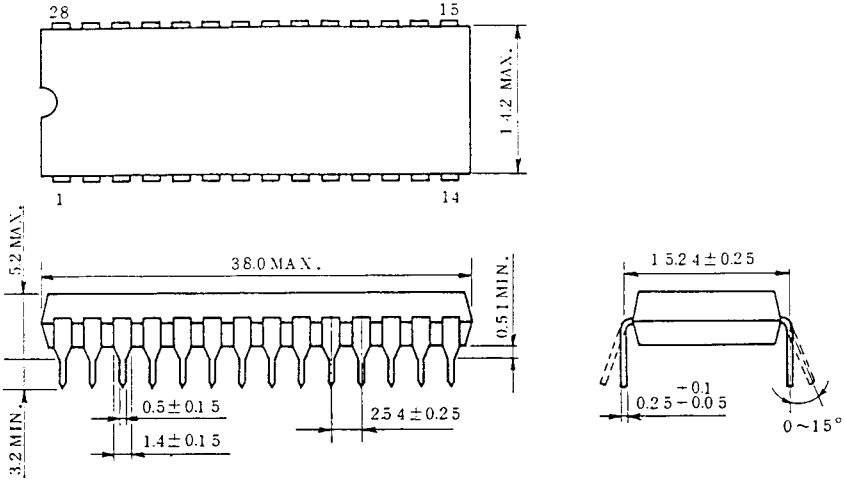
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{WC}	Write Cycle Time	1000	-	-	ns
t_{WP}	Write Pulse Width	500	-	-	
t_{CW}	Chip Selection to End of Write	800	-	-	
t_{AS}	Address Set Up Time	100	-	-	
t_{WR}	Write Recovery Time	100	-	-	
t_{ODW}	R/W to Output in High-Z	-	-	200	
t_{OEW}	R/W to Output in Low-Z	5	-	-	
t_{DS}	Data Set Up Time	400	-	-	
t_{DH}	Data Hold Time	50	-	-	

A.C. TEST CONDITIONS

- Input Pulse Levels : $V_{DD}-0.2V/0.2V$
- Timing Measurement Reference Levels: $V_{DD}/2$ / $V_{DD}/2$
- Output Reference Levels : $V_{DD}/2$ / $V_{DD}/2$
- Input Pulse Rise and Fall Time : $\leqq$ 20ns
- Output Load : 100pF + 1 TTL Gate

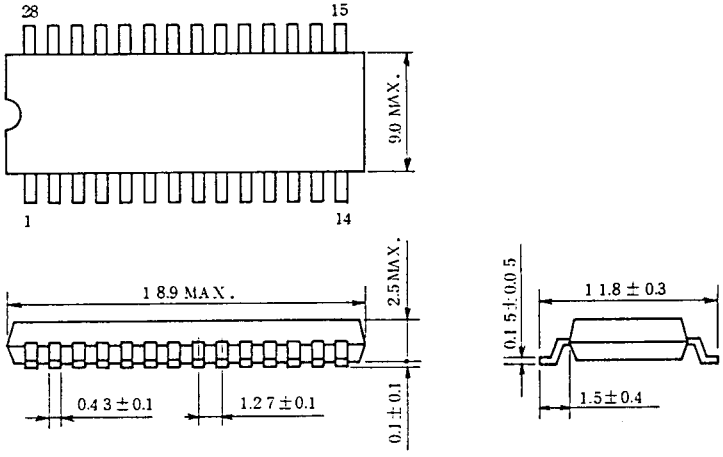
DIP 28 PIN OUTLINE DRAWING (DIP28-P-600)

Unit in mm



Note: Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

SOP 28 PIN OUTLINE DRAWING (SOP28-P-450)



Note: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.