FT7C185A-20LMB

8K X 8 CMOS SRAM

FORCE TECHNOLOGIES LTD

Features

- **High-speed address/chip select access time**
  Mil:20/25/35/45/55/70/85/100(Max)
  MB=Mil-Std-883 Method 5004
- **Low power consumption**
- **Produced with advanced CMOS high-performance technology**
- **Inputs and outputs directly TTL-compatible**
- **Three-state outputs**
- **Available in 28-pin D=CERDIP and L= LCC**

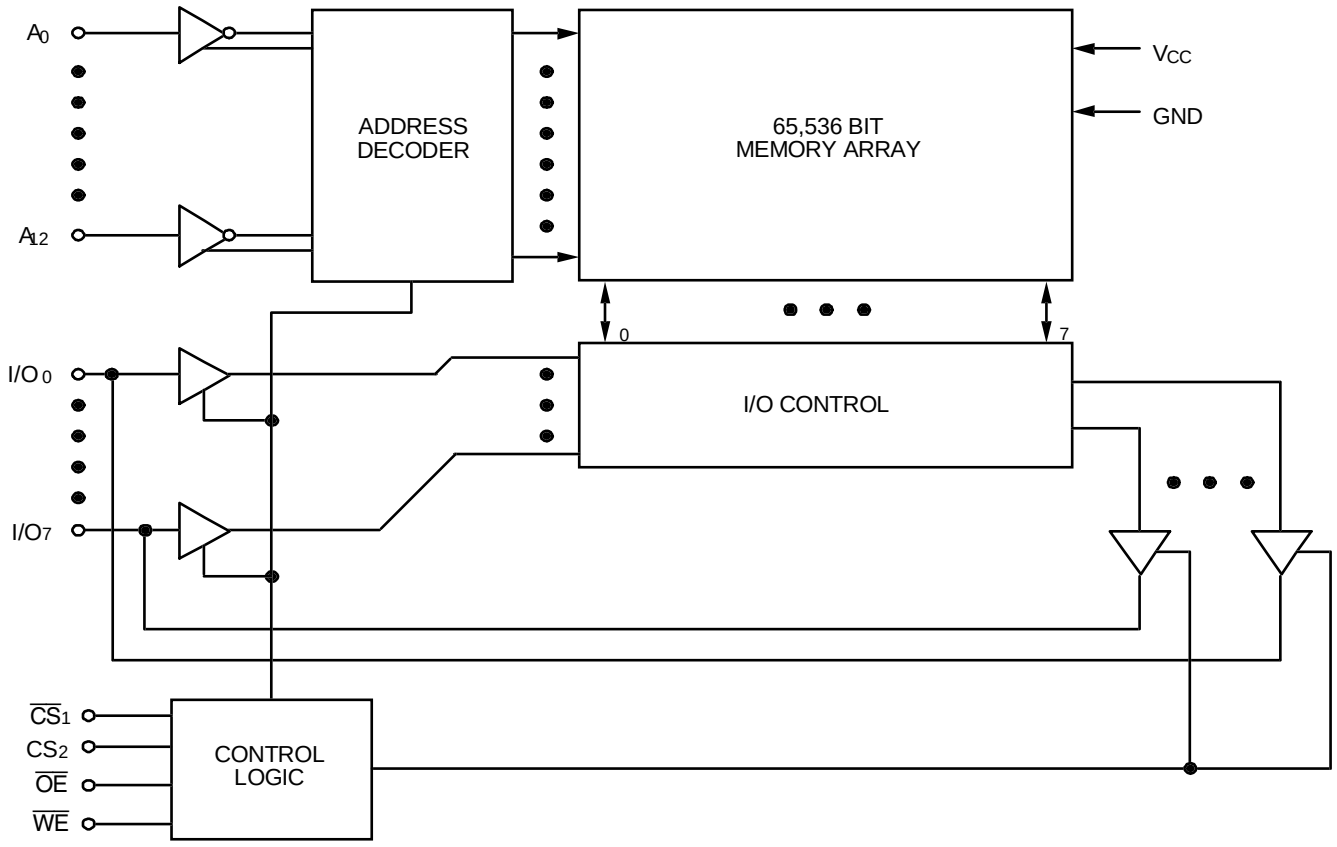
Description

The FT7C185 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using high-performance, high-reliability CMOS technology.

Address access times as fast as 15ns are available and the circuit offers a reduced power standby mode. When $\overline{CS}_1$ goes HIGH or CS_2 goes LOW, the circuit will automatically go to, and remain in, a low-power stand by mode. All inputs and outputs of the FT7C185 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The FT7C185 is packaged in a 28-pin 600 mil CERDIP and a 32-pin ceramic LCC.

Functional Block Diagram



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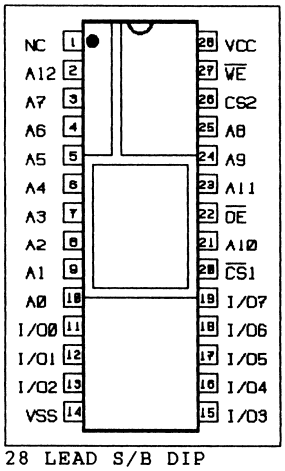
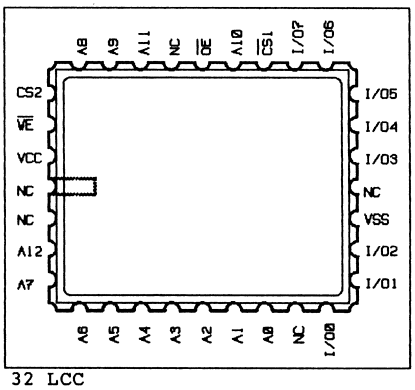
Pin Configurations



28 LEAD S/B DIP



32 LCC

Top View

Absolute Maximum Ratings[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

Pin Descriptions

Name	Description
A_0 - A_{12}	Address
I/O_0 - I/O_7	Data Input/Output
$\overline{CS_1}$	Chip Select
CS_2	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

Truth Table[1,2,3]

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O	Function
X	H	X	X	High-Z	Deselected - Standby (I_{SB})
X	X	L	X	High-Z	Deselected - Standby (I_{SB})
X	V_{HC}	V_{HC} or V_{LC}	X	High-Z	Deselected - Standby (I_{SB1})
X	X	V_{LC}	X	High-Z	Deselected - Standby (I_{SB1})
H	L	H	H	High-Z	Output Disabled
H	L	H	L	$DATA_{OUT}$	Read Data
L	L	H	X	$DATA_{IN}$	Write Data

NOTES:

1. CS_2 will power-down $\overline{CS_1}$, but $\overline{CS_1}$ will not power-down CS_2.
2. H = V_{IH}, L = V_{IL}, X = don't care.
3. V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input HIGH Voltage	2.2	—	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage	-0.5[1]	—	0.8	V

NOTE:

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Industrial	-40°C to +85°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

DC Electrical Characteristics[1] (V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	15	20		25			Unit
			Com'l.	Com'l.	Mil.	Com'l.	Ind.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open V_{CC} = Max., f = 0[2]	S	110	100	110	90	90	110	mA
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	180	170	180	170	170	180	mA
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1} \geq V_{IH}$, $CS_2 \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	S	20	20	20	20	20	20	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[2], V_{CC} = Max. 1. $\overline{CS_1} \geq V_{HC}$ and $CS_2 \geq V_{HC}$, or 2. $CS_2 \leq V_{LC}$	S	15	15	20	15	15	20	mA

Symbol	Parameter	Power	35			45	55	70	85/100	Unit
			Com'l.	Ind.	Mil.	Mil.	Mil.	Mil.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open V_{CC} = Max., f = 0[2]	S	90	90	100	100	100	100	100	mA
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	150	150	160	160	160	160	160	mA
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1} \geq V_{IH}$, $CS_2 \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	S	20	20	20	20	20	20	20	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[2], V_{CC} = Max. 1. $\overline{CS_1} \geq V_{HC}$ and $CS_2 \geq V_{HC}$, or 2. $CS_2 \leq V_{LC}$	S	15	15	20	20	20	20	20	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		S				Unit
				Min.	Max.			
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L. & IND	— —	10 5			µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L. & IND	— —	10 5			µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4			V
		I_{OL} = 10mA, V_{CC} = Min.		—	0.5			
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—			V

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

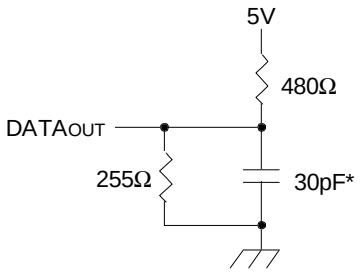


Figure 1. AC Test Load

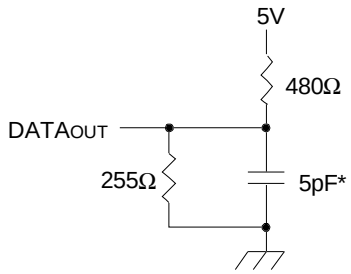


Figure 2. AC Test Load
(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Includes scope and jig capacitances

AC Electrical Characteristics (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	15[1]		20[2]		25		35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	19	—	25	—	35	ns
t_{ACS1}[3]	Chip Select-1 Access Time	—	15	—	20	—	25	—	35	ns
t_{ACS2}[3]	Chip Select-2 Access Time	—	20	—	25	—	30	—	40	ns
$t_{CLZ1,2}$[4]	Chip Select-1, 2 to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	12	—	18	ns
t_{OLZ}[4]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
$t_{CHZ1,2}$[4]	Chip Select-1,2 to Output in High-Z	—	8	—	9	—	13	—	15	ns
t_{OHZ}[4]	Output Disable to Output in High-Z	—	7	—	8	—	10	—	15	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}[4]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[4]	Chip Deselect to Power Down Time	—	15	—	20	—	25	—	35	ns
Write Cycle										
t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	ns
$t_{CW1,2}$	Chip Select to End-of-Write	14	—	15	—	18	—	25	—	ns
t_{AW}	Address Valid to End-of-Write	14	—	15	—	18	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	14	—	15	—	21	—	25	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{WHZ}[4]	Write Enable to Output in High-Z	—	6	—	8	—	10	—	14	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	13	—	15	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{OW}[4]	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns

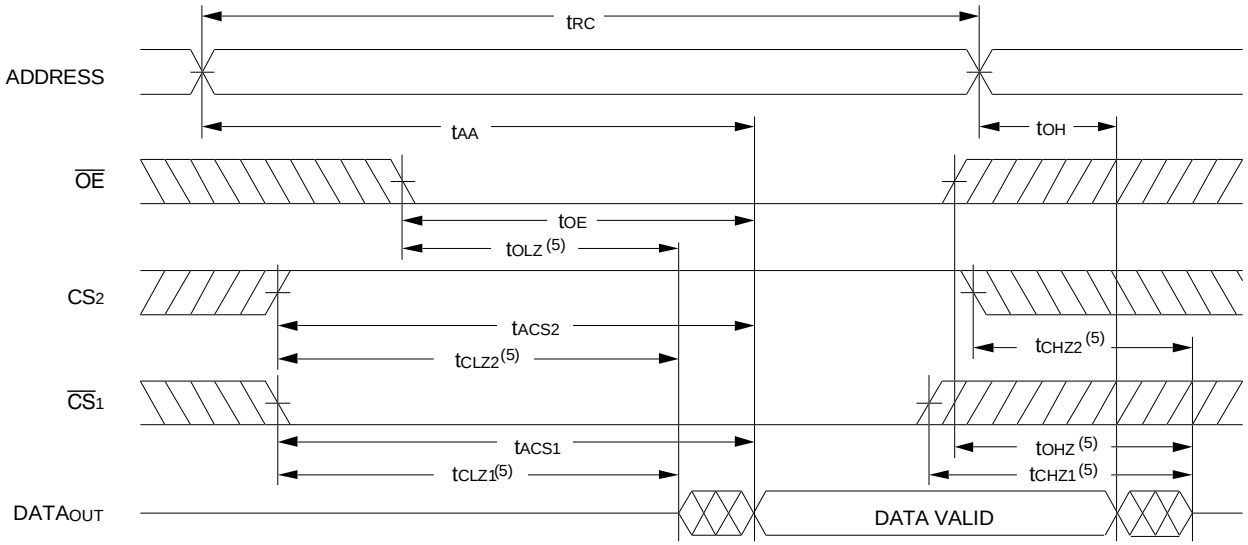
NOTES:
1. 0° to +70°C temperature range only.
2. 0° to +70°C and –55°C to +125°C temperature ranges only.
3. Both chip selects must be active for the device to be selected.
4. This parameter is guaranteed by device characterization, but is not production tested.

AC Electrical Characteristics (con't.) (Vcc = 5.0V ± 10%, Military Temperature Ranges)

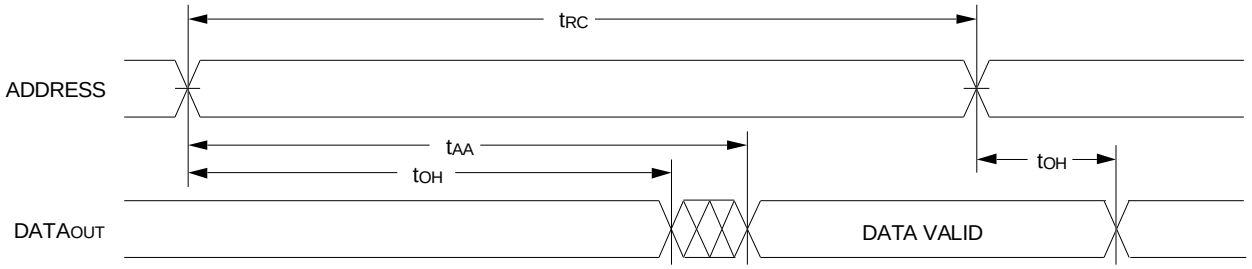
Symbol	Parameter	45		55		70		85/100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	45	—	55	—	70	—	85/100	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	—	85/100	ns
t_{ACS1}(1)	Chip Select-1 Access Time	—	45	—	55	—	70	—	85/100	ns
t_{ACS2}(1)	Chip Select-2 Access Time	—	45	—	55	—	70	—	85/100	ns
$t_{CLZ1,2}$(2)	Chip Select-1, 2 to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	35	—	40	ns
t_{OLZ}(2)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
$t_{CHZ1,2}$(2)	Chip Select-1,2 to Output in High-Z	—	20	—	25	—	30	—	35	ns
t_{OHZ}(2)	Output Disable to Output in High-Z	—	20	—	25	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}(2)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(2)	Chip Deselect to Power Down Time	—	45	—	55	—	70	—	85/100	ns
Write Cycle										
t_{WC}	Write Cycle Time	45	—	55	—	70	—	85/100	—	ns
$t_{CW1,2}$	Chip Select to End-of-Write	33	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End-of-Write	33	—	50	—	60	—	75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	50	—	60	—	75	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{WHZ}(2)	Write Enable to Output in High-Z	—	18	—	25	—	30	—	35	ns
t_{DW}	Data to Write Time Overlap	20	—	25	—	30	—	35	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{OW}(2)	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns

NOTES:
1. Both chip selects must be active for the device to be selected.
2. This parameter is guaranteed by device characterization, but is not production tested.

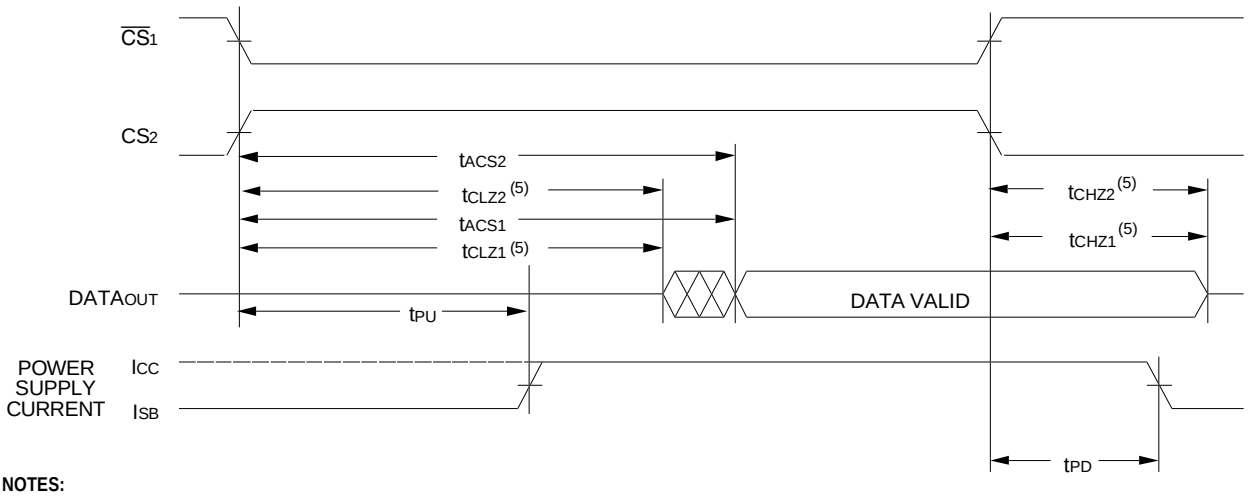
Timing Waveform of Read Cycle No. 1[1)]



Timing Waveform of Read Cycle No. 2[1,2,4)]



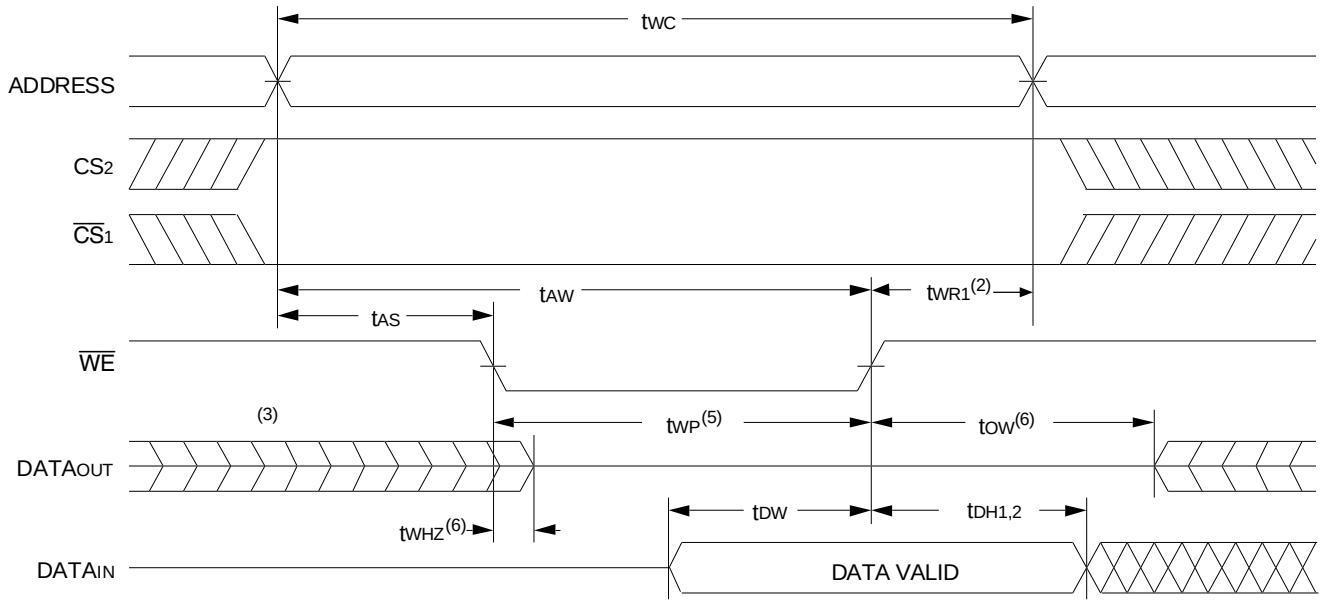
Timing Waveform of Read Cycle No. 3[1,3,4)]



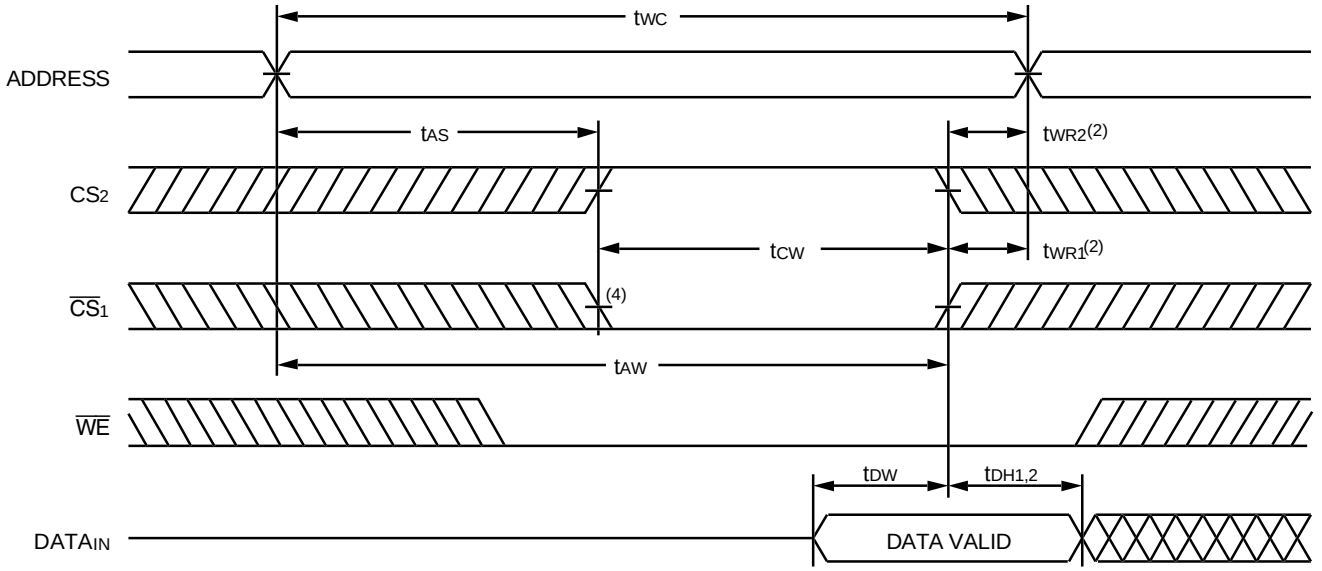
NOTES:

1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS_1}$ is LOW, CS_2 is HIGH.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition LOW and CS_2 transition HIGH.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)[1,5]



Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)[1]



NOTES:

1. A write occurs during the overlap of a LOW $\overline{WE}$, a LOW $\overline{CS}_1$ and a HIGH CS_2.
2. $t_{WR1,\ 2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going HIGH or CS_2 going LOW to the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals must not be applied.
4. If the $\overline{CS}_1$ LOW transition or CS_2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} +t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified t_{WP}.
6. Transition is measured ±200mV from steady state.

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