

Dual 1-of-4 Decoder/Demultiplexer

Product Specification

Military Logic Products

FEATURES

- Demultiplexing capability
- Two independent 1-of-4 decoders
- Multifunction capability

DESCRIPTION

The 54F139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0, A_1) and providing four mutually exclusive active Low outputs ($\bar{Q}_{0n} - \bar{Q}_{3n}$). Each decoder has an active Low Enable (\bar{E}). When \bar{E} is High, every output is forced High. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

FUNCTION TABLE

INPUTS			OUTPUTS			
E	A ₀	A ₁	Q ₀	Q ₁	Q ₂	Q ₃
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	L	L	H	H
L	H	L	L	H	L	H
L	H	H	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

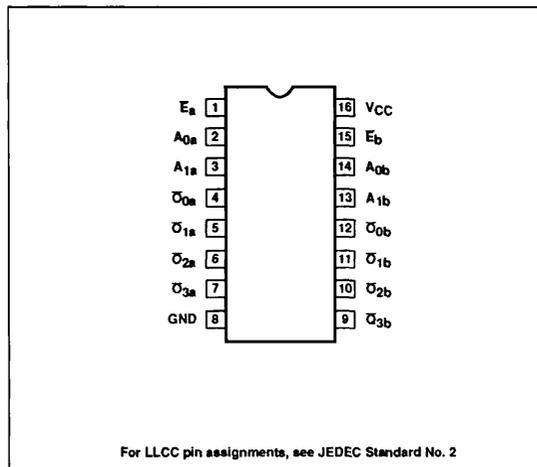
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F139/BEA
16-Pin Ceramic FlatPack	54F139/BFA
20-Pin Ceramic LLCC	54F139/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

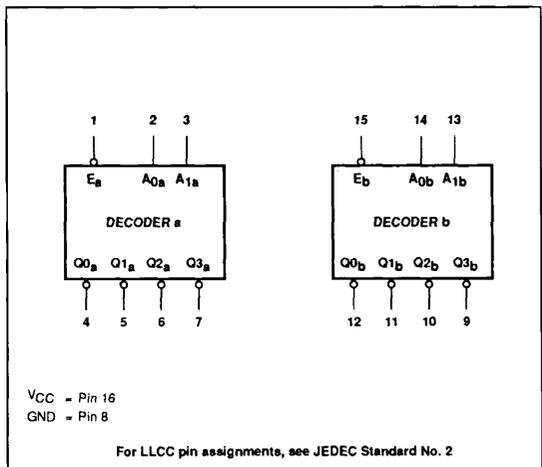
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A _{na} - A _{nb}	Address inputs	1.0/1.0	20μA/0.6mA
E _a - E _b	Enable inputs	1.0/1.0	20μA/0.6mA
Q _{0a} - Q _{3a} , Q _{0b} - Q _{3b}	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



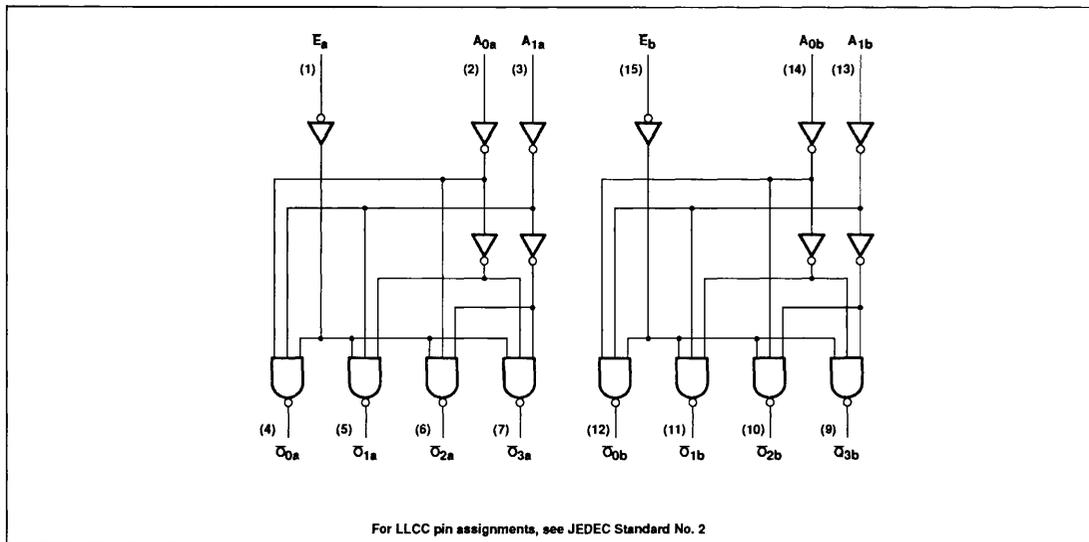
LOGIC SYMBOL



Decoder/Demultiplexer

54F139

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage range	-0.5 to +7.0	V
V _I	Input voltage range	-0.5 to +7.0	V
I _I	Input current range	-30 to +5	mA
V _O	Voltage applied to output in High output state range	-0.5 to +V _{CC}	V
I _O	Current applied to output in Low output state	40	mA
T _{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-1	mA
I _{OL}	Low-level output current			20	mA
T _A	Operating free-air temperature range	-55		+125	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			Min	Typ ²	Max	
V _{OH}	High-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OH} = Max, V _{IH} = Min	2.5			V
V _{OL}	Low-level output voltage	V _{CC} = Min, V _{IL} = Max, I _{OL} = Max, V _{IH} = Min		0.35	0.50	V
V _{IK}	Input clamp voltage	V _{CC} = Min, I _I = I _{IK}		-0.73	-1.2	V
I _{IH2}	Input current at maximum input voltage	V _{CC} = Max, V _I = 7.0V			100	μA
I _{IH1}	High-level input current	V _{CC} = Max, V _I = 2.7V		1	20	μA
I _{IL}	Low-level input current	V _{CC} = Max, V _I = 0.5V		-0.4	-0.6	mA
I _{OS}	Short-circuit output current ³	V _{CC} = Max, V _O = 0.0V	-60	-90	-150	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = Max		13	20	mA

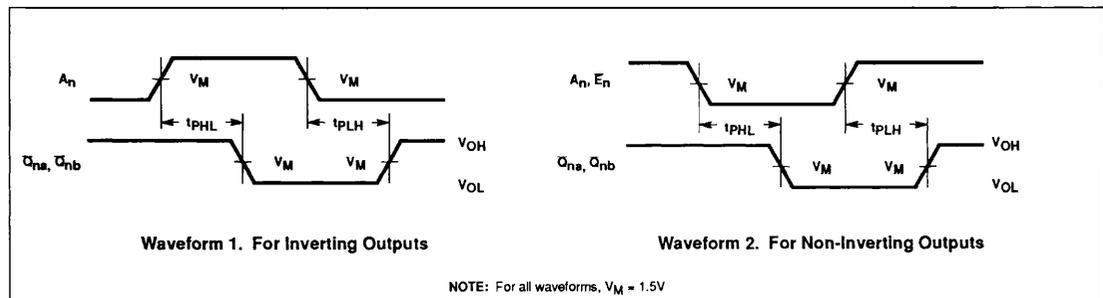
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _A = +25°C, V _{CC} = +5.0V			T _A = -55°C to +125°C		
			Min	Type	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A ₀ to A ₁ to Q _{na} , Q _{nb}	Waveform 1 and 2	3.5 4.0	5.3 6.1	7.0 8.0	2.5 3.5	12.0 9.5	ns ns
t _{PLH} t _{PHL}	Propagation delay E _n to Q _{na} , Q _{nb}	Waveform 2	3.5 3.0	5.4 4.7	7.0 6.5	3.0 2.5	9.0 8.0	ns ns

NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- To measure I_{CC}, outputs must be open, V_{IH} on all inputs = 4.5V.

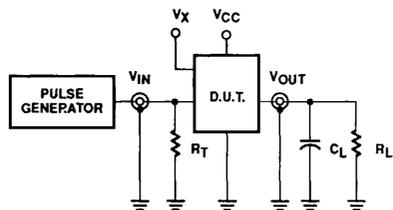
AC WAVEFORMS



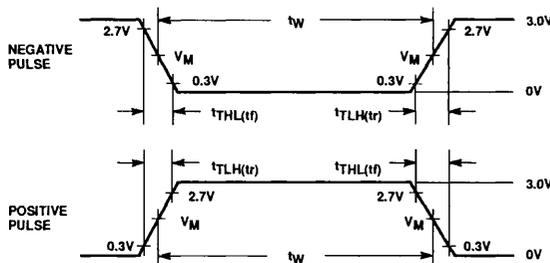
Decoder/Demultiplexer

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TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS:

- R_L = Load Resistor; see AC Characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- V_X = Unlocked pins must be held at: $\leq 0.8V$, $\geq 2.7V$ or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	$\leq 2.5ns$	$\leq 2.5ns$