



# M50LPW080

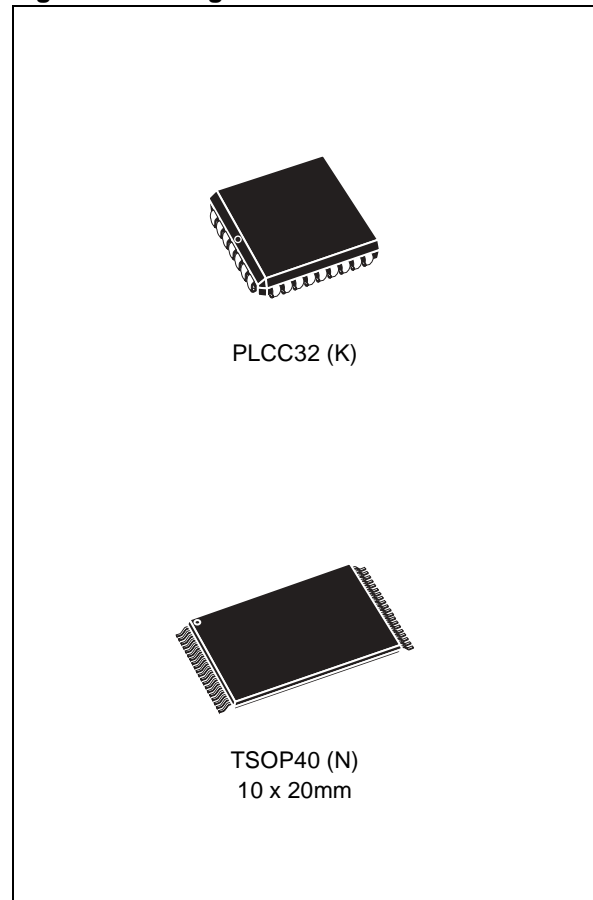
8 Mbit (1M x8, Uniform Block)  
3V Supply Low Pin Count Flash Memory

NOT FOR NEW DESIGN

## FEATURES SUMMARY

- **SUPPLY VOLTAGE**
  - $V_{CC} = 3.0$  to  $3.6V$  for Program, Erase and Read Operations
  - $V_{PP} = 12V$  for Fast Program and Fast Erase (optional)
- **TWO INTERFACES**
  - Low Pin Count (LPC) Standard Interface for embedded operation with PC Chipsets.
  - Address/Address Multiplexed (A/A Mux) Interface for programming equipment compatibility.
- **LOW PIN COUNT (LPC) HARDWARE INTERFACE MODE**
  - 5 Signal Communication Interface supporting Read and Write Operations
  - Hardware Write Protect Pins for Block Protection
  - Register Based Read and Write Protection
  - 5 Additional General Purpose Inputs for platform design flexibility
  - Synchronized with 33MHz PCI clock
- **PROGRAMMING TIME**
  - $10\mu s$  typical
  - Quadruple Byte Programming Option
- **16 UNIFORM 64 Kbyte MEMORY BLOCKS**
- **PROGRAM/ERASE CONTROLLER**
  - Embedded Byte Program and Block/Chip Erase algorithms
  - Status Register Bits
- **PROGRAM and ERASE SUSPEND**
  - Read other Blocks during Program/Erase Suspend
  - Program other Blocks during Erase Suspend
- **FOR USE in PC BIOS APPLICATIONS**
- **ELECTRONIC SIGNATURE**
  - Manufacturer Code: 20h
  - Device Code: 2Fh

Figure 1. Packages



## TABLE OF CONTENTS

<b>FEATURES SUMMARY</b> .....	<b>1</b>
Figure 1. Packages .....	1
<b>SUMMARY DESCRIPTION</b> .....	<b>6</b>
Figure 2. Logic Diagram (LPC Interface) .....	7
Figure 3. Logic Diagram (A/A Mux Interface) .....	7
Table 1. Signal Names (LPC Interface) .....	7
Table 2. Signal Names (A/A Mux Interface) .....	7
Figure 4. PLCC Connections .....	8
Figure 5. TSOP Connections .....	9
Table 3. Memory Identification Input Configuration .....	9
<b>SIGNAL DESCRIPTIONS</b> .....	<b>10</b>
<b>Low Pin Count (LPC) Signal Descriptions</b> .....	<b>10</b>
Input/Output Communications (LAD0-LAD3) .....	10
Input Communication Frame ( $\overline{\text{LFRAME}}$ ) .....	10
Identification Inputs (ID0-ID1) .....	10
General Purpose Inputs (GPIO-GPI4) .....	10
Interface Configuration (IC) .....	10
Interface Reset ( $\overline{\text{RP}}$ ) .....	10
CPU Reset ( $\overline{\text{INIT}}$ ) .....	10
Clock (CLK) .....	10
Top Block Lock ( $\overline{\text{TBL}}$ ) .....	10
Write Protect ( $\overline{\text{WP}}$ ) .....	10
Reserved for Future Use (RFU) .....	11
Table 4. Block Addresses .....	11
<b>Address/Address Multiplexed (A/A Mux) Signal Descriptions</b> .....	<b>11</b>
Address Inputs (A0-A10) .....	11
Data Inputs/Outputs (DQ0-DQ7) .....	11
Output Enable ( $\overline{\text{G}}$ ) .....	11
Write Enable ( $\overline{\text{W}}$ ) .....	11
Row/Column Address Select ( $\overline{\text{RC}}$ ) .....	11
Ready/Busy Output ( $\overline{\text{RB}}$ ) .....	11
<b>Supply Signal Descriptions</b> .....	<b>11</b>
V <sub>CC</sub> Supply Voltage .....	11
V <sub>PP</sub> Optional Supply Voltage .....	11
V <sub>SS</sub> Ground .....	12
<b>BUS OPERATIONS</b> .....	<b>12</b>
<b>Low Pin Count (LPC) Bus Operations</b> .....	<b>12</b>
Bus Read .....	12
Bus Write .....	12
Bus Abort .....	12

Standby. . . . .	12
Reset. . . . .	12
Block Protection. . . . .	12
<b>Address/Address Multiplexed (A/A Mux) Bus Operations. . . . .</b>	<b>12</b>
Bus Read. . . . .	13
Bus Write. . . . .	13
Output Disable. . . . .	13
Reset. . . . .	13
Table 5. A/A Mux Bus Operations . . . . .	13
Table 6. Manufacturer and Device Codes . . . . .	13
Table 7. LPC Bus Read Field Definitions . . . . .	14
Figure 6. LPC Bus Read Waveforms . . . . .	14
Table 8. LPC Bus Write Field Definitions. . . . .	15
Figure 7. LPC Bus Write Waveforms . . . . .	15
<b>COMMAND INTERFACE . . . . .</b>	<b>16</b>
Read Memory Array Command. . . . .	16
Read Status Register Command. . . . .	16
Read Electronic Signature Command . . . . .	16
Table 9. Read Electronic Signature. . . . .	16
Program Command . . . . .	16
Quadruple Byte Program Command. . . . .	16
Chip Erase Command. . . . .	17
Block Erase Command . . . . .	17
Clear Status Register Command. . . . .	17
Program/Erase Suspend Command . . . . .	17
Program/Erase Resume Command . . . . .	17
Table 10. Commands . . . . .	18
<b>STATUS REGISTER . . . . .</b>	<b>19</b>
Program/Erase Controller Status (Bit 7) . . . . .	19
Erase Suspend Status (Bit 6) . . . . .	19
Erase Status (Bit 5) . . . . .	19
Program Status (Bit 4). . . . .	19
V <sub>PP</sub> Status (Bit 3). . . . .	19
Program Suspend Status (Bit 2) . . . . .	20
Block Protection Status (Bit 1) . . . . .	20
Reserved (Bit 0). . . . .	20
Table 11. Status Register Bits . . . . .	20
<b>LOW PIN COUNT (LPC) INTERFACE CONFIGURATION REGISTERS. . . . .</b>	<b>21</b>
Table 12. Low Pin Count Register Configuration Map <sup>(1)</sup> . . . . .	21
<b>Lock Registers. . . . .</b>	<b>21</b>
Write Lock . . . . .	21
Read Lock . . . . .	21
Lock Down. . . . .	22

<b>General Purpose Input Register</b> .....	<b>22</b>
Table 13. Lock Register Bit Definitions .....	22
Table 14. General Purpose Input Register Definition .....	22
<b>PROGRAM AND ERASE TIMES</b> .....	<b>23</b>
Table 15. Program and Erase Times .....	23
<b>MAXIMUM RATING</b> .....	<b>24</b>
Table 16. Absolute Maximum Ratings .....	24
<b>DC AND AC PARAMETERS</b> .....	<b>25</b>
Table 17. Operating Conditions .....	25
Table 18. LPC Interface AC Measurement Conditions .....	25
Table 19. A/A Mux Interface AC Measurement Conditions .....	25
Figure 8. LPC Interface AC Testing Input Output Waveforms .....	25
Figure 9. A/A Mux Interface AC Testing Input Output Waveform .....	26
Table 20. Impedance .....	26
Table 21. DC Characteristics .....	27
Figure 10. LPC Interface Clock Waveform .....	28
Table 22. LPC Interface Clock Characteristics .....	28
Figure 11. LPC Interface AC Signal Timing Waveforms .....	29
Table 23. LPC Interface AC Signal Timing Characteristics .....	29
Figure 12. Reset AC Waveforms .....	30
Table 24. Reset AC Characteristics .....	30
Figure 13. A/A Mux Interface Read AC Waveforms .....	31
Table 25. A/A Mux Interface Read AC Characteristics .....	31
Figure 14. A/A Mux Interface Write AC Waveforms .....	32
Table 26. A/A Mux Interface Write AC Characteristics .....	32
<b>PACKAGE MECHANICAL</b> .....	<b>33</b>
Figure 15. PLCC32 – 32 pin Rectangular Plastic Leaded Chip Carrier, Package Outline .....	33
Table 27. PLCC32 – 32 pin Rectangular Plastic Leaded Chip Carrier, Package Mechanical Data .....	34
Figure 16. TSOP40 – 40 lead Plastic Thin Small Outline, 10x20 mm, Package Outline .....	35
Table 28. TSOP40 – 40 lead Plastic Thin Small Outline, 10x20 mm, Package Mechanical Data .....	35
<b>PART NUMBERING</b> .....	<b>36</b>
Table 29. Ordering Information Scheme .....	36
<b>FLOWCHARTS AND PSEUDO CODES</b> .....	<b>37</b>
Figure 17. Program Flowchart and Pseudo Code .....	37
Figure 18. Quadruple Byte Program Flowchart and Pseudo Code (A/A Mux Interface Only) .....	38
Figure 19. Program Suspend and Resume Flowchart and Pseudo Code .....	39
Figure 20. Chip Erase Flowchart and Pseudo Code (A/A Mux Interface Only) .....	40
Figure 21. Block Erase Flowchart and Pseudo Code .....	41
Figure 22. Erase Suspend and Resume Flowchart and Pseudo Code .....	42

**REVISION HISTORY** ..... 43  
    Table 30. Revision History ..... 43

### SUMMARY DESCRIPTION

The M50LPW080 is a 8 Mbit (1Mb x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (3.0 to 3.6V) supply. For fast programming and fast erasing in production lines an optional 12V power supply can be used to reduce the programming and the erasing times.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Blocks can be protected individually to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected

and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Two different bus interfaces are supported by the memory. The primary interface is the Low Pin Count (or LPC) Standard Interface. This has been designed to remove the need for the ISA bus in current PC Chipsets; the M50LPW080 acts as the PC BIOS on the Low Pin Count bus for these PC Chipsets.

The secondary interface, the Address/Address Multiplexed (or A/A Mux) Interface, is designed to be compatible with current Flash Programmers for production line programming prior to fitting to a PC Motherboard.

The memory is offered in TSOP40 (10 x 20mm) and PLCC32 packages and it is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram (LPC Interface)

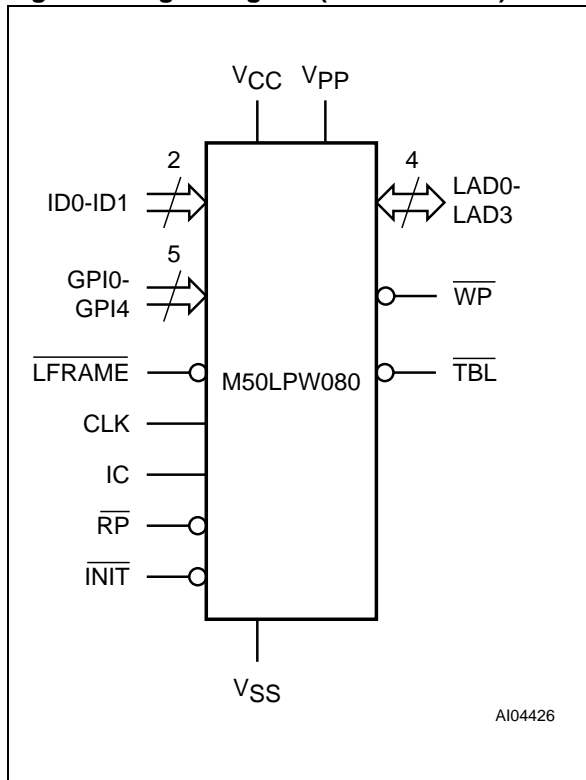


Table 1. Signal Names (LPC Interface)

LAD0-LAD3	Input/Output Communications
$\overline{\text{LFRAME}}$	Input Communication Frame
ID0-ID1	Identification Inputs
GPI0-GPI4	General Purpose Inputs
IC	Interface Configuration
$\overline{\text{RP}}$	Interface Reset
$\overline{\text{INIT}}$	CPU Reset
CLK	Clock
$\overline{\text{TBL}}$	Top Block Lock
WP	Write Protect
RFU	Reserved for Future Use. Leave disconnected
VCC	Supply Voltage
VPP	Optional Supply Voltage for Fast Erase Operations
VSS	Ground
NC	Not Connected Internally

Figure 3. Logic Diagram (A/A Mux Interface)

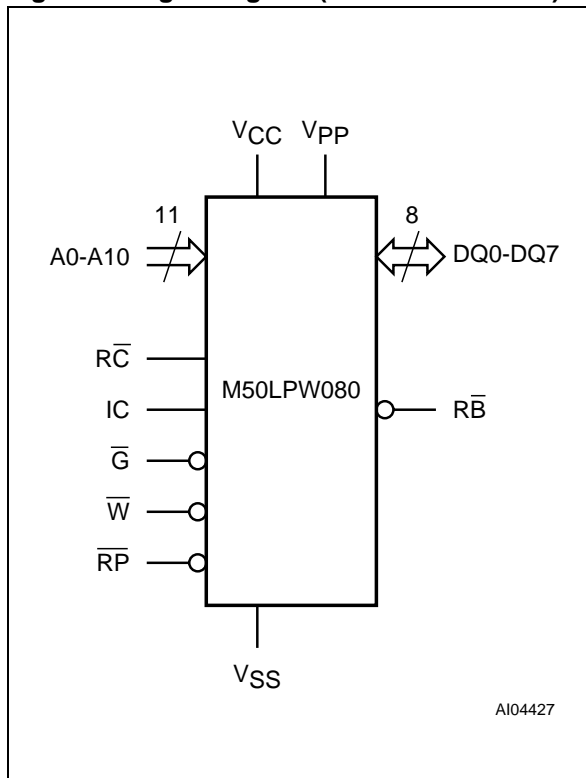
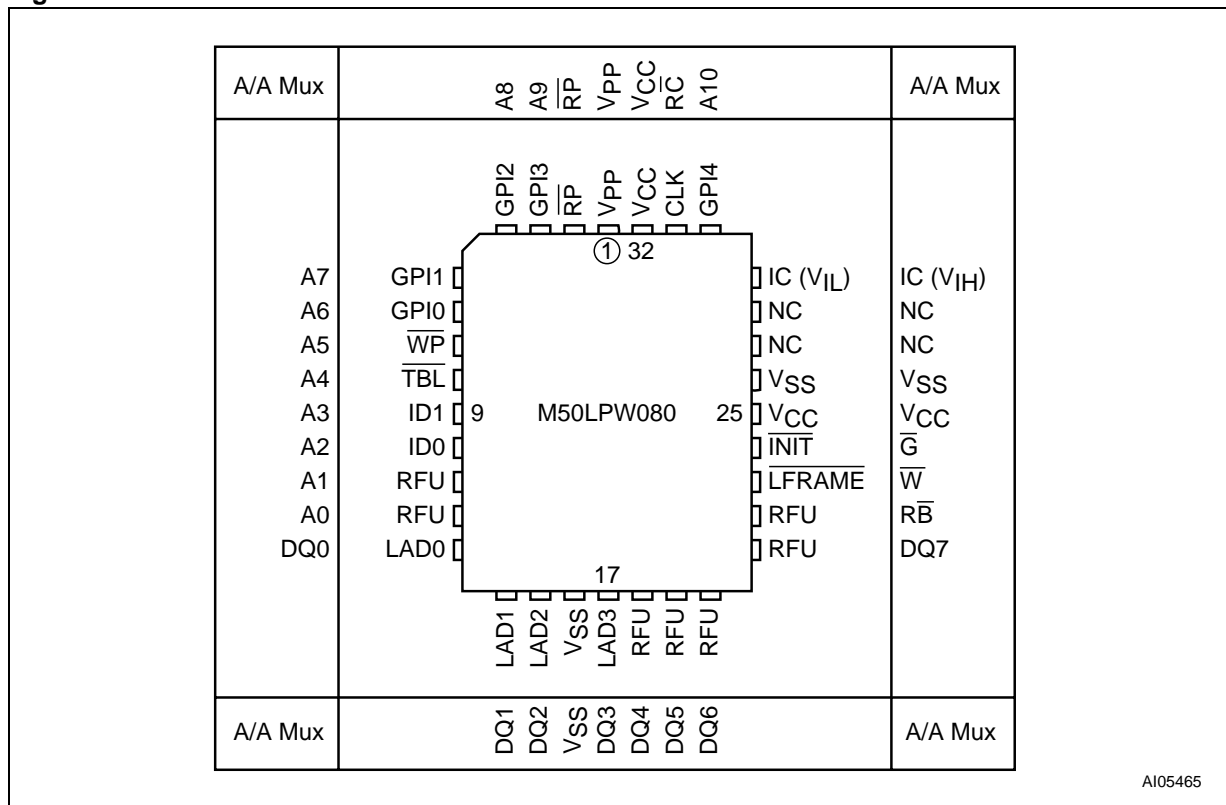


Table 2. Signal Names (A/A Mux Interface)

IC	Interface Configuration
A0-A10	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Write Enable
$\overline{\text{RC}}$	Row/Column Address Select
$\overline{\text{RB}}$	Ready/Busy Output
$\overline{\text{RP}}$	Interface Reset
VCC	Supply Voltage
VPP	Optional Supply Voltage for Fast Program and Fast Erase Operations
VSS	Ground
NC	Not Connected Internally

# M50LPW080

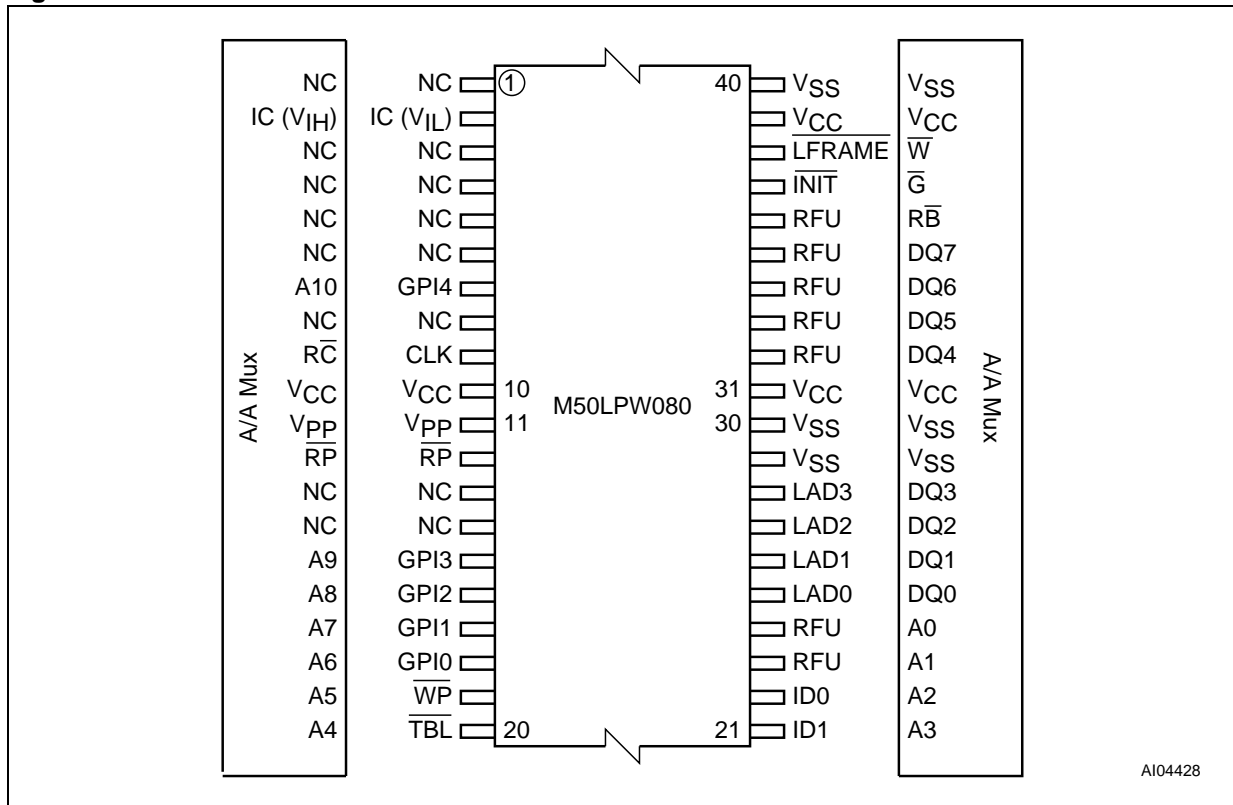
Figure 4. PLCC Connections



AI05465



Figure 5. TSOP Connections



AI04428

Table 3. Memory Identification Input Configuration

Memory Number	ID1	ID0	A21	A20
1 (Boot)	V <sub>IL</sub> or floating	V <sub>IL</sub> or floating	1	1
2	V <sub>IL</sub> or floating	V <sub>IH</sub>	1	0
3	V <sub>IH</sub>	V <sub>IL</sub> or floating	0	1
4	V <sub>IH</sub>	V <sub>IH</sub>	0	0

## SIGNAL DESCRIPTIONS

There are two different bus interfaces available on this part. The active interface is selected before power-up or during Reset using the Interface Configuration Pin, IC.

The signals for each interface are discussed in the Low Pin Count (LPC) Signal Descriptions section and the Address/Address Multiplexed (A/A Mux) Signal Descriptions section below. The supply signals are discussed in the Supply Signal Descriptions section below.

### Low Pin Count (LPC) Signal Descriptions

For the Low Pin Count (LPC) Interface see [Figure 2.](#) and [Table 1.](#)

#### Input/Output Communications (LAD0-LAD3).

All Input and Output Communication with the memory take place on these pins. Addresses and Data for Bus Read and Bus Write operations are encoded on these pins.

**Input Communication Frame (LFRAME).** The Input Communication Frame (LFRAME) signals the start of a bus operation. When Input Communication Frame is Low,  $V_{IL}$ , on the rising edge of the Clock a new bus operation is initiated. If Input Communication Frame is Low,  $V_{IL}$ , during a bus operation then the operation is aborted. When Input Communication Frame is High,  $V_{IH}$ , the current bus operation is proceeding or the bus is idle.

**Identification Inputs (ID0-ID1).** The Identification Inputs (ID0-ID1) allow to address up to 4 memories on a bus. The value on addresses A20-A21 is compared to the hardware strapping on the ID0-ID1 pins to select which memory is being addressed. For an address bit to be '1' the correspondent ID pin can be left floating or driven Low,  $V_{IL}$ ; an internal pull-down resistor is included with a value of  $R_{IL}$ . For an address bit to be '0' the correspondent ID pin must be driven High,  $V_{IH}$ ; there will be a leakage current of  $I_{L12}$  through each pin when pulled to  $V_{IH}$  (see [Table 21.](#)).

By convention the boot memory must have ID0-ID1 pins left floating or driven Low,  $V_{IL}$  and a '11' value on A20-A21 and all additional memories take sequential ID0-ID1 configuration, as shown in [Table 3.](#)

**General Purpose Inputs (GPIO-GPI4).** The General Purpose Inputs can be used as digital inputs for the CPU to read. The General Purpose Input Register holds the values on these pins. The pins must have stable data from before the start of the cycle that reads the General Purpose Input Register until after the cycle is complete. These pins must not be left to float, they should be driven Low,  $V_{IL}$ , or High,  $V_{IH}$ .

**Interface Configuration (IC).** The Interface Configuration input selects whether the Low Pin Count

(LPC) or the Address/Address Multiplexed (A/A Mux) Interface is used. The chosen interface must be selected before power-up or during a Reset and, thereafter, cannot be changed. The state of the Interface Configuration, IC, should not be changed during operation.

To select the Low Pin Count (LPC) Interface the Interface Configuration pin should be left to float or driven Low,  $V_{IL}$ ; to select the Address/Address Multiplexed (A/A Mux) Interface the pin should be driven High,  $V_{IH}$ . An internal pull-down resistor is included with a value of  $R_{IL}$ ; there will be a leakage current of  $I_{L12}$  through each pin when pulled to  $V_{IH}$ ; see [Table 21.](#)

**Interface Reset ( $\overline{RP}$ ).** The Interface Reset ( $\overline{RP}$ ) input is used to reset the memory. When Interface Reset ( $\overline{RP}$ ) is set Low,  $V_{IL}$ , the memory is in Reset mode: the outputs are put to high impedance and the current consumption is minimized. When  $\overline{RP}$  is set High,  $V_{IH}$ , the memory is in normal operation. After exiting Reset mode, the memory enters Read mode.

**CPU Reset ( $\overline{INIT}$ ).** The CPU Reset,  $\overline{INIT}$ , pin is used to Reset the memory when the CPU is reset. It behaves identically to Interface Reset,  $\overline{RP}$ , and the internal Reset line is the logical OR (electrical AND) of  $\overline{RP}$  and  $\overline{INIT}$ .

**Clock (CLK).** The Clock, CLK, input is used to clock the signals in and out of the Input/Output Communication Pins, LAD0-LAD3. The Clock conforms to the PCI specification.

**Top Block Lock ( $\overline{TBL}$ ).** The Top Block Lock input is used to prevent the Top Block (Block 15) from being changed. When Top Block Lock,  $\overline{TBL}$ , is set Low,  $V_{IL}$ , Program and Block Erase operations in the Top Block have no effect, regardless of the state of the Lock Register. When Top Block Lock,  $\overline{TBL}$ , is set High,  $V_{IH}$ , the protection of the Block is determined by the Lock Register. The state of Top Block Lock,  $\overline{TBL}$ , does not affect the protection of the Main Blocks (Blocks 0 to 14).

Top Block Lock,  $\overline{TBL}$ , must be set prior to a Program or Block Erase operation is initiated and must not be changed until the operation completes or unpredictable results may occur. Care should be taken to avoid unpredictable behavior by changing  $\overline{TBL}$  during Program or Erase Suspend.

**Write Protect ( $\overline{WP}$ ).** The Write Protect input is used to prevent the Main Blocks (Blocks 0 to 14) from being changed. When Write Protect,  $\overline{WP}$ , is set Low,  $V_{IL}$ , Program and Block Erase operations in the Main Blocks have no effect, regardless of the state of the Lock Register. When Write Protect,  $\overline{WP}$ , is set High,  $V_{IH}$ , the protection of the Block is determined by the Lock Register. The state of

Write Protect,  $\overline{WP}$ , does not affect the protection of the Top Block (Block 15).

Write Protect,  $\overline{WP}$ , must be set prior to a Program or Block Erase operation is initiated and must not be changed until the operation completes or unpredictable results may occur. Care should be taken to avoid unpredictable behavior by changing  $\overline{WP}$  during Program or Erase Suspend.

**Reserved for Future Use (RFU).** These pins do not have assigned functions in this revision of the part. They must be left disconnected.

**Table 4. Block Addresses**

Size (Kbytes)	Address Range	Block Number	Block Type
64	F0000h-FFFFFh	15	Top Block
64	E0000h-EFFFFh	14	Main Block
64	D0000h-DFFFFh	13	Main Block
64	C0000h-CFFFFh	12	Main Block
64	B0000h-BFFFFh	11	Main Block
64	A0000h-AFFFFh	10	Main Block
64	90000h-9FFFFh	9	Main Block
64	80000h-8FFFFh	8	Main Block
64	70000h-7FFFFh	7	Main Block
64	60000h-6FFFFh	6	Main Block
64	50000h-5FFFFh	5	Main Block
64	40000h-4FFFFh	4	Main Block
64	30000h-3FFFFh	3	Main Block
64	20000h-2FFFFh	2	Main Block
64	10000h-1FFFFh	1	Main Block
64	00000h-0FFFFh	0	Main Block

#### Address/Address Multiplexed (A/A Mux) Signal Descriptions

For the Address/Address Multiplexed (A/A Mux) Interface see [Figure 3](#), and [Table 2](#).

**Address Inputs (A0-A10).** The Address Inputs are used to set the Row Address bits (A0-A10) and the Column Address bits (A11-A19). They are latched during any bus operation by the Row/Column Address Select input,  $\overline{RC}$ .

**Data Inputs/Outputs (DQ0-DQ7).** The Data Inputs/Outputs hold the data that is written to or read from the memory. They output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. The Data Inputs/Outputs, DQ0-DQ7, are latched during a Bus Write operation.

**Output Enable ( $\overline{G}$ ).** The Output Enable,  $\overline{G}$ , controls the Bus Read operation of the memory.

**Write Enable ( $\overline{W}$ ).** The Write Enable,  $\overline{W}$ , controls the Bus Write operation of the memory's Command Interface.

**Row/Column Address Select ( $\overline{RC}$ ).** The Row/Column Address Select input selects whether the Address Inputs should be latched into the Row Address bits (A0-A10) or the Column Address bits (A11-A19). The Row Address bits are latched on the falling edge of  $\overline{RC}$  whereas the Column Address bits are latched on the rising edge.

**Ready/Busy Output ( $\overline{RB}$ ).** The Ready/Busy pin gives the status of the memory's Program/Erase Controller. When Ready/Busy is Low,  $V_{OL}$ , the memory is busy with a Program or Erase operation and it will not accept any additional Program or Erase command except the Program/Erase Suspend command. When Ready/Busy is High,  $V_{OH}$ , the memory is ready for any Read, Program or Erase operation.

#### Supply Signal Descriptions

The Supply Signals are the same for both interfaces.

**V<sub>CC</sub> Supply Voltage.** The V<sub>CC</sub> Supply Voltage supplies the power for all operations (Read, Program, Erase etc.).

The Command Interface is disabled when the V<sub>CC</sub> Supply Voltage is less than the Lockout Voltage, V<sub>LKO</sub>. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid. After V<sub>CC</sub> becomes valid the Command Interface is reset to Read mode.

A 0.1μF capacitor should be connected between the V<sub>CC</sub> Supply Voltage pins and the V<sub>SS</sub> Ground pin to decouple the current surges from the power supply. Both V<sub>CC</sub> Supply Voltage pins must be connected to the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

**V<sub>PP</sub> Optional Supply Voltage.** The V<sub>PP</sub> Optional Supply Voltage pin is used to select the Fast Program (see the Quadruple Byte Program Command description) and Fast Erase options of the memory and to protect the memory. When V<sub>PP</sub> < V<sub>PPLK</sub> Program and Erase operations cannot be performed and an error is reported in the Status Register if an attempt to change the memory contents is made. When V<sub>PP</sub> = V<sub>CC</sub> Program and Erase operations take place as normal. When V<sub>PP</sub> = V<sub>PPH</sub> Fast Program (if a Quadruple Byte Program Command is performed) and Fast Erase operations are

used. Any other voltage input to  $V_{PP}$  will result in undefined behavior and should not be used.

$V_{PP}$  should not be set to  $V_{PPH}$  for more than 80 hours during the life of the memory.

## BUS OPERATIONS

The two interfaces have similar bus operations but the signals and timings are completely different. The Low Pin Count (LPC) Interface is the usual interface and all of the functionality of the part is available through this interface. Only a subset of functions are available through the Address/Address Multiplexed (A/A Mux) Interface.

Follow the section Low Pin Count (LPC) Bus Operations below and the section Address/Address Multiplexed (A/A Mux) Interface Bus Operations below for a description of the bus operations on each interface.

### Low Pin Count (LPC) Bus Operations

The Low Pin Count (LPC) Interface consists of four data signals (LAD0-LAD3), one control line ( $\overline{\text{LFRAME}}$ ) and a clock (CLK). In addition protection against accidental or malicious data corruption can be achieved using two further signals ( $\overline{\text{TBL}}$  and  $\overline{\text{WP}}$ ). Finally two reset signals (RP and INIT) are available to put the memory into a known state.

The data signals, control signal and clock are designed to be compatible with PCI electrical specifications. The interface operates with clock speeds up to 33MHz.

The following operations can be performed using the appropriate bus cycles: Bus Read, Bus Write, Standby, Reset and Block Protection.

**Bus Read.** Bus Read operations read from the memory cells, specific registers in the Command Interface or Low Pin Count Registers. A valid Bus Read operation starts when Input Communication Frame,  $\overline{\text{LFRAME}}$ , is Low,  $V_{IL}$ , as Clock rises and the correct Start cycle is on LAD0-LAD3. On the following clock cycles the Host will send the Cycle Type + Dir, Address and other control bits on LAD0-LAD3. The memory responds by outputting Sync data until the wait-states have elapsed followed by Data0-Data3 and Data4-Data7.

See Table 7. and Figure 6. for a description of the Field definitions for each clock cycle of the transfer. See Table 23. and Figure 11. for details on the timings of the signals.

**Bus Write.** Bus Write operations write to the Command Interface or Low Pin Count Registers. A valid Bus Write operation starts when Input Communication Frame,  $\overline{\text{LFRAME}}$ , is Low,  $V_{IL}$ , as Clock rises and the correct Start cycle is on LAD0-LAD3.

**$V_{SS}$  Ground.**  $V_{SS}$  is the reference for all the voltage measurements.

On the following Clock cycles the Host will send the Cycle Type + Dir, Address, other control bits, Data0-Data3 and Data4-Data7 on LAD0-LAD3. The memory outputs Sync data until the wait-states have elapsed.

See Table 8. and Figure 7. for a description of the Field definitions for each clock cycle of the transfer. See Table 23. and Figure 11. for details on the timings of the signals.

**Bus Abort.** The Bus Abort operation can be used to immediately abort the current bus operation. A Bus Abort occurs when  $\overline{\text{LFRAME}}$  is driven Low,  $V_{IL}$ , during the bus operation; the memory will tristate the Input/Output Communication pins, LAD0-LAD3.

Note that, during a Bus Write operation, the Command Interface starts executing the command as soon as the data is fully received; a Bus Abort during the final TAR cycles is not guaranteed to abort the command; the bus, however, will be released immediately.

**Standby.** When  $\overline{\text{LFRAME}}$  is High,  $V_{IH}$ , the memory is put into Standby mode where LAD0-LAD3 are put into a high-impedance state and the Supply Current is reduced to the Standby level,  $I_{CC1}$ .

**Reset.** During Reset mode all internal circuits are switched off, the memory is deselected and the outputs are put in high-impedance. The memory is in Reset mode when Interface Reset,  $\overline{\text{RP}}$ , or CPU Reset, INIT, is Low,  $V_{IL}$ .  $\overline{\text{RP}}$  or INIT must be held Low,  $V_{IL}$ , for  $t_{PLPH}$ . The memory resets to Read mode upon return from Reset mode and the Lock Registers return to their default states regardless of their state before Reset (see Table 13.). If  $\overline{\text{RP}}$  or INIT goes Low,  $V_{IL}$ , during a Program or Erase operation, the operation is aborted and the memory cells affected no longer contain valid data; the memory can take up to  $t_{PLRH}$  to abort a Program or Erase operation.

**Block Protection.** Block Protection can be forced using the signals Top Block Lock,  $\overline{\text{TBL}}$ , and Write Protect,  $\overline{\text{WP}}$ , regardless of the state of the Lock Registers.

### Address/Address Multiplexed (A/A Mux) Bus Operations

The Address/Address Multiplexed (A/A Mux) Interface has a more traditional style interface. The signals consist of a multiplexed address signals (A0-

A10), data signals, (DQ0-DQ7) and three control signals ( $\overline{RC}$ ,  $\overline{G}$ ,  $\overline{W}$ ). An additional signal,  $\overline{RP}$ , can be used to reset the memory.

The Address/Address Multiplexed (A/A Mux) Interface is included for use by Flash Programming equipment for faster factory programming. Only a subset of the features available to the Low Pin Count (LPC) Interface are available; these include all the Commands but exclude the Security features and other registers.

The following operations can be performed using the appropriate bus cycles: Bus Read, Bus Write, Output Disable and Reset.

When the Address/Address Multiplexed (A/A Mux) Interface is selected all the blocks are unprotected. It is not possible to protect any blocks through this interface.

**Bus Read.** Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature and the Status Register. A valid Bus Read operation begins by latching the Row Address and Column Address signals into the memory using the Address Inputs, A0-A10, and the Row/Column Address Select  $\overline{RC}$ . Then Write Enable ( $\overline{W}$ ) and Interface Reset ( $\overline{RP}$ ) must be High,  $V_{IH}$ , and Output Enable,  $\overline{G}$ , Low,  $V_{IL}$ , in order to perform a Bus Read operation. The Data Inputs/

Outputs will output the value, see Figure 13. and Table 25. for details of when the output becomes valid.

**Bus Write.** Bus Write operations write to the Command Interface. A valid Bus Write operation begins by latching the Row Address and Column Address signals into the memory using the Address Inputs, A0-A10, and the Row/Column Address Select  $\overline{RC}$ . The data should be set up on the Data Inputs/Outputs; Output Enable,  $\overline{G}$ , and Interface Reset,  $\overline{RP}$ , must be High,  $V_{IH}$  and Write Enable,  $\overline{W}$ , must be Low,  $V_{IL}$ . The Data Inputs/Outputs are latched on the rising edge of Write Enable,  $\overline{W}$ . See Figure 14. and Table 26. for details of the timing requirements.

**Output Disable.** The data outputs are high-impedance when the Output Enable,  $\overline{G}$ , is at  $V_{IH}$ .

**Reset.** During Reset mode all internal circuits are switched off, the memory is deselected and the outputs are put in high-impedance. The memory is in Reset mode when  $\overline{RP}$  is Low,  $V_{IL}$ .  $\overline{RP}$  must be held Low,  $V_{IL}$  for  $t_{PLPH}$ . If  $\overline{RP}$  is goes Low,  $V_{IL}$ , during a Program or Erase operation, the operation is aborted and the memory cells affected no longer contain valid data; the memory can take up to  $t_{PLRH}$  to abort a Program or Erase operation.

**Table 5. A/A Mux Bus Operations**

Operation	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}$	DQ7-DQ0
Bus Read	$V_{IL}$	$V_{IH}$	$V_{IH}$	Don't Care	Data Output
Bus Write	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{CC}$ or $V_{PPH}$	Data Input
Output Disable	$V_{IH}$	$V_{IH}$	$V_{IH}$	Don't Care	Hi-Z
Reset	$V_{IL}$ or $V_{IH}$	$V_{IL}$ or $V_{IH}$	$V_{IL}$	Don't Care	Hi-Z

**Table 6. Manufacturer and Device Codes**

Operation	$\overline{G}$	$\overline{W}$	$\overline{RP}$	A19-A1	A0	DQ7-DQ0
Manufacturer Code	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	20h
Device Code	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	2Fh

Table 7. LPC Bus Read Field Definitions

Clock Cycle Number	Clock Cycle Count	Field	LAD0-LAD3	Memory I/O	Description
1	1	START	0000b	I	On the rising edge of CLK with $\overline{\text{LFRAME}}$ Low, the contents of LAD0-LAD3 must be 0000b to indicate the start of a LPC cycle.
2	1	CYCTYPE + DIR	010Xb	I	Indicates the type of cycle. Bits 3:2 must be 01b. Bit 1 indicates the direction of transfer: 0b for read. Bit 0 is don't care (X).
3-10	8	ADDR	XXXX	I	A 32-bit address phase is transferred starting with the most significant nibble first. A23-A31 must be set to 1. A22 = 1 for Array, A22 = 0 for registers access. For A20-A21 values, see Table 3..
11	1	TAR	1111b	I	The host drives LAD0-LAD3 to 1111b to indicate a turnaround cycle.
12	1	TAR	1111b (float)	O	The LPC Flash Memory takes control of LAD0-LAD3 during this cycle.
13-14	2	WSYNC	0101b	O	The LPC Flash Memory drives LAD0-LAD3 to 0101b (short wait-sync) for two clock cycles, indicating that the data is not yet available. Two wait-states are always included.
15	1	RSYNC	0000b	O	The LPC Flash Memory drives LAD0-LAD3 to 0000b, indicating that data will be available during the next clock cycle.
16-17	2	DATA	XXXX	O	Data transfer is two CLK cycles, starting with the least significant nibble.
18	1	TAR	1111b	O	The LPC Flash Memory drives LAD0-LAD3 to 1111b to indicate a turnaround cycle.
19	1	TAR	1111b (float)	N/A	The LPC Flash Memory floats its outputs, the host takes control of LAD0-LAD3.

Figure 6. LPC Bus Read Waveforms

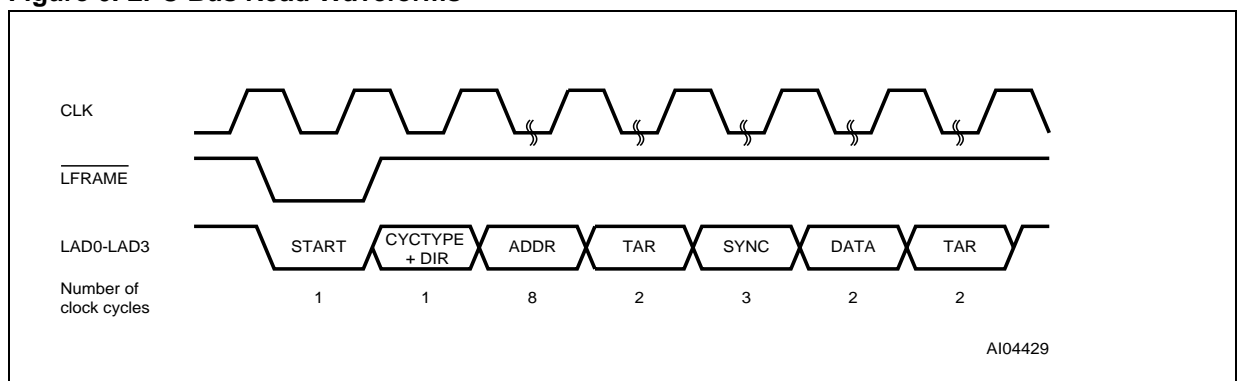
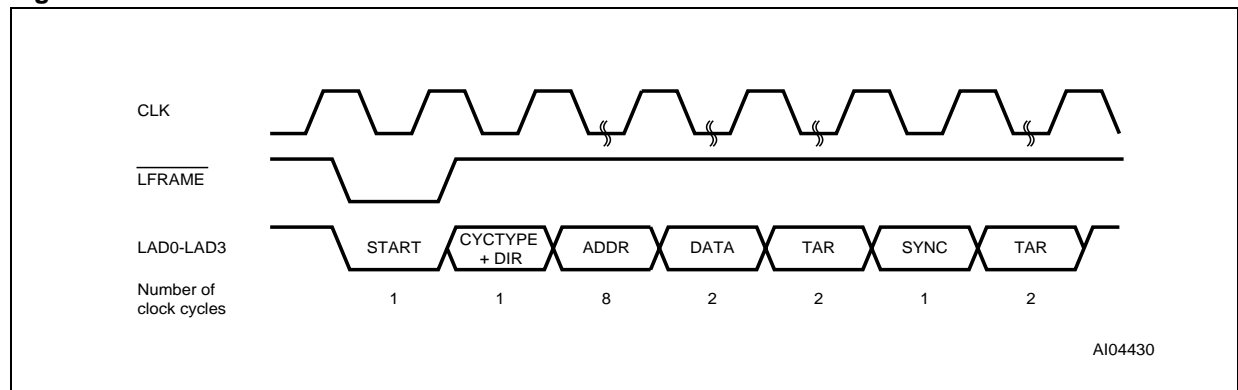


Table 8. LPC Bus Write Field Definitions

Clock Cycle Number	Clock Cycle Count	Field	LAD0-LAD3	Memory I/O	Description
1	1	START	0000b	I	On the rising edge of CLK with $\overline{\text{LFRAME}}$ Low, the contents of LAD0-LAD3 must be 0000b to indicate the start of a LPC cycle.
2	1	CYCTY PE + DIR	011Xb	I	Indicates the type of cycle. Bits 3:2 must be 01b. Bit 1 indicates the direction of transfer: 1b for write. Bit 0 is don't care (X).
3-10	8	ADDR	XXXX	I	A 32-bit address phase is transferred starting with the most significant nibble first. A23-A31 must be set to 1. A22 = 1 for Array, A22 = 0 for registers access. For A20-A21 values, see Table 3..
11-12	2	DATA	XXXX	I	Data transfer is two cycles, starting with the least significant nibble.
13	1	TAR	1111b	I	The host drives LAD0-LAD3 to 1111b to indicate a turnaround cycle.
14	1	TAR	1111b (float)	O	The LPC Flash Memory takes control of LAD0-LAD3 during this cycle.
15	1	SYNC	0000b	O	The LPC Flash Memory drives LAD0-LAD3 to 0000b, indicating it has received data or a command.
16	1	TAR	1111b	O	The LPC Flash Memory drives LAD0-LAD3 to 1111b, indicating a turnaround cycle.
17	1	TAR	1111b (float)	N/A	The LPC Flash Memory floats its outputs and the host takes control of LAD0-LAD3.

Figure 7. LPC Bus Write Waveforms



## COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations.

After power-up or a Reset operation the memory enters Read mode.

The commands are summarized in [Table 10](#). The following text descriptions should be read in conjunction with [Table 10](#).

**Read Memory Array Command.** The Read Memory Array command returns the memory to its Read mode where it behaves like a ROM or EPROM. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Once the command is issued the memory remains in Read mode until another command is issued. From Read mode Bus Read operations will access the memory array.

While the Program/Erase Controller is executing a Program or Erase operation the memory will not accept the Read Memory Array command until the operation completes.

**Read Status Register Command.** The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued subsequent Bus Read operations read the Status Register until another command is issued. See the section on the Status Register for details on the definitions of the Status Register bits.

**Read Electronic Signature Command.** The Read Electronic Signature command is used to read the Manufacturer Code and the Device Code. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations read the Manufacturer Code or the Device Code until another command is issued.

After the Read Electronic Signature Command is issued the Manufacturer Code and Device Code can be read using Bus Read operations using the addresses in [Table 9](#).

**Table 9. Read Electronic Signature**

Code	Address	Data
Manufacturer Code	00000h	20h
Device Code	00001h	2Fh

**Program Command.** The Program command can be used to program a value to one address in the memory array at a time. Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the address and data

in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

If the address falls in a protected block then the Program operation will abort, the data in the memory array will not be changed and the Status Register will output the error.

During the Program operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Program times are given in [Table 15](#).

Note that the Program command cannot change a bit set at '0' back to '1' and attempting to do so will not cause any modification on its value. One of the Erase commands must be used to set all of the bits in the block to '1'.

See [Figure 17](#) for a suggested flowchart on using the Program command.

**Quadruple Byte Program Command.** The Quadruple Byte Program Command can be only used in A/A Mux mode to program four adjacent bytes in the memory array at a time. The four bytes must differ only for the addresses A0 and A10. Programming should not be attempted when  $V_{PP}$  is not at  $V_{PPH}$ . The operation can also be executed if  $V_{PP}$  is below  $V_{PPH}$ , but result could be uncertain. Five Bus Write operations are required to issue the command. The second, the third and the fourth Bus Write cycle latches respectively the address and data of the first, the second and the third byte in the internal state machine. The fifth Bus Write cycle latches the address and data of the fourth byte in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Quadruple Byte Program operation the memory will only accept the Read Status register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Quadruple Byte Program times are given in [Table 15](#).

Note that the Quadruple Byte Program command cannot change a bit set to '0' back to '1' and attempting to do so will not cause any modification on its value. One of the Erase commands must be used to set all of the bits in the block to '1'.

See [Figure 18](#) for a suggested flowchart on using the Quadruple Byte Program command.



**Chip Erase Command.** The Chip Erase Command can be only used in A/A Mux mode to erase the entire chip at a time. Erasing should not be attempted when  $V_{PP}$  is not at  $V_{PPH}$ . The operation can also be executed if  $V_{PP}$  is below  $V_{PPH}$ , but result could be uncertain. Two Bus Write operations are required to issue the command and start the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits. During the Chip Erase operation the memory will only accept the Read Status Register command. All other commands will be ignored. Typical Chip Erase times are given in [Table 15](#). The Chip Erase command sets all of the bits in the memory to '1'. See [Figure 20](#) for a suggested flowchart on using the Chip Erase command.

**Block Erase Command.** The Block Erase command can be used to erase a block. Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

If the block is protected then the Block Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

During the Block Erase operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Block Erase times are given in [Table 15](#).

The Block Erase command sets all of the bits in the block to '1'. All previous data in the block is lost.

See [Figure 21](#) for a suggested flowchart on using the Block Erase command.

**Clear Status Register Command.** The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One Bus Write is required to issue the Clear Status Register command. Once the command is issued the memory returns to its previous mode, subsequent Bus Read operations continue to output the same data.

The bits in the Status Register are sticky and do not automatically return to '0' when a new Program or Erase command is issued. If an error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program or Erase command.

**Program/Erase Suspend Command.** The Program/Erase Suspend command can be used to pause a Program or Block Erase operation. One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/Erase Controller has paused. After the Program/Erase Controller has paused, the memory will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing it is possible for the operation to complete. Once Program/Erase Controller Status bit indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit or the Erase Suspend Status bit can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see [Table 15](#).

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Block Erase then the Program command will also be accepted; only the blocks not being erased may be read or programmed correctly.

See [Figure 19](#) and [Figure 22](#) for suggested flowcharts on using the Program/Erase Suspend command.

**Program/Erase Resume Command.** The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command. Once the command is issued subsequent Bus Read operations read the Status Register.

Table 10. Commands

Command	Cycles	Bus Write Operations									
		1st		2nd		3rd		4th		5th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read Memory Array	1	X	FFh								
Read Status Register	1	X	70h								
Read Electronic Signature	1	X	90h								
	1	X	98h								
Program	2	X	40h	PA	PD						
	2	X	10h	PA	PD						
Quadruple Byte Program	5	X	30h	A <sub>1</sub>	PD	A <sub>2</sub>	PD	A <sub>3</sub>	PD	A <sub>4</sub>	PD
Chip Erase	2	X	80h	X	10h						
Block Erase	2	X	20h	BA	D0h						
Clear Status Register	1	X	50h								
Program/Erase Suspend	1	X	B0h								
Program/Erase Resume	1	X	D0h								
Invalid/Reserved	1	X	00h								
	1	X	01h								
	1	X	60h								
	1	X	2Fh								
	1	X	C0h								

Note: X Don't Care, PA Program Address, PD Program Data, A<sub>1,2,3,4</sub> Consecutive Addresses, BA Any address in the Block.

**Read Memory Array.** After a Read Memory Array command, read the memory as normal until another command is issued.

**Read Status Register.** After a Read Status Register command, read the Status Register as normal until another command is issued.

**Read Electronic Signature.** After a Read Electronic Signature command, read Manufacturer Code, Device Code until another command is issued.

**Block Erase, Program.** After these commands read the Status Register until the command completes and another command is issued.

**Quadruple Byte Program.** This command is only valid in A/A Mux mode. Addresses A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub> and A<sub>4</sub> must be consecutive addresses differing only for address bit A0 and A10. After this command read the Status Register until the command completes and another command is issued.

**Chip Erase.** This command is only valid in A/A Mux mode. After this command read the Status Register until the command completes and another command is issued.

**Clear Status Register.** After the Clear Status Register command bits 1, 3, 4 and 5 in the Status Register are reset to '0'.

**Program/Erase Suspend.** After the Program/Erase Suspend command has been accepted, issue Read Memory Array, Read Status Register, Program (during Erase suspend) and Program/Erase resume commands.

**Program/Erase Resume.** After the Program/Erase Resume command the suspended Program/Erase operation resumes, read the Status Register until the Program/Erase Controller Do not use Invalid or Reserved commands not use Invalid or Reserved commands.

## STATUS REGISTER

The Status Register provides information on the current or previous Program or Erase operation. Different bits in the Status Register convey different information and errors on the operation.

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase and Program/Erase Resume commands are issued. The Status Register can be read from any address.

The Status Register bits are summarized in [Table 11](#). The following text descriptions should be read in conjunction with [Table 11](#).

**Program/Erase Controller Status (Bit 7).** The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is '0', the Program/Erase Controller is active; when the bit is '1', the Program/Erase Controller is inactive.

The Program/Erase Controller Status is '0' immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is '1'.

During Program and Erase operation the Program/Erase Controller Status bit can be polled to find the end of the operation. The other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is '1'.

After the Program/Erase Controller completes its operation the Erase Status, Program Status,  $V_{PP}$  Status and Block Protection Status bits should be tested for errors.

**Erase Suspend Status (Bit 6).** The Erase Suspend Status bit indicates that a Block Erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is '1' (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode. When the Erase Suspend Status bit is '0' the Program/Erase Controller is active or has completed its operation; when the bit is '1' a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns to '0'.

**Erase Status (Bit 5).** The Erase Status bit can be used to identify if the memory has applied the maximum number of erase pulses to the block(s)

and still failed to verify that the block(s) has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is '1' (Program/Erase Controller inactive).

When the Erase Status bit is '0' the memory has successfully verified that the block(s) has erased correctly; when the Erase Status bit is '1' the Program/Erase Controller has applied the maximum number of pulses to the block(s) and still failed to verify that the block(s) has erased correctly.

Once the Erase Status bit is set to '1' it can only be reset to '0' by a Clear Status Register command or a hardware reset. If it is set to '1' it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

**Program Status (Bit 4).** The Program Status bit can be used to identify if the memory has applied the maximum number of program pulses to the byte and still failed to verify that the byte has programmed correctly. The Program Status bit should be read once the Program/Erase Controller Status bit is '1' (Program/Erase Controller inactive).

When the Program Status bit is '0' the memory has successfully verified that the byte has programmed correctly; when the Program Status bit is '1' the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that the byte has programmed correctly.

Once the Program Status bit is set to '1' it can only be reset to '0' by a Clear Status Register command or a hardware reset. If it is set to '1' it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

**$V_{PP}$  Status (Bit 3).** The  $V_{PP}$  Status bit can be used to identify an invalid voltage on the  $V_{PP}$  pin during Program and Erase operations. The  $V_{PP}$  pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if  $V_{PP}$  becomes invalid during a Program or Erase operation.

When the  $V_{PP}$  Status bit is '0' the voltage on the  $V_{PP}$  pin was sampled at a valid voltage; when the  $V_{PP}$  Status bit is '1' the  $V_{PP}$  pin has a voltage that is below the  $V_{PP}$  Lockout Voltage,  $V_{PPLK}$ , the memory is protected; Program and Erase operation cannot be performed.

Once the  $V_{PP}$  Status bit set to '1' it can only be reset to '0' by a Clear Status Register command or a hardware reset. If it is set to '1' it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

**Program Suspend Status (Bit 2).** The Program Suspend Status bit indicates that a Program operation has been suspended and is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is '1' (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Program Suspend Status bit is '0' the Program/Erase Controller is active or has completed its operation; when the bit is '1' a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns to '0'.

**Block Protection Status (Bit 1).** The Block Protection Status bit can be used to identify if the Pro-

gram or Block Erase operation has tried to modify the contents of a protected block. When the Block Protection Status bit is to '0' no Program or Block Erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset; when the Block Protection Status bit is '1' a Program or Block Erase operation has been attempted on a protected block.

Once it is set to '1' the Block Protection Status bit can only be reset to '0' by a Clear Status Register command or a hardware reset. If it is set to '1' it should be reset before a new Program or Block Erase command is issued, otherwise the new command will appear to fail.

Using the A/A Mux Interface the Block Protection Status bit is always '0'.

**Reserved (Bit 0).** Bit 0 of the Status Register is reserved. Its value should be masked.

**Table 11. Status Register Bits**

Operation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
Program active	'0'	X <sup>(1)</sup>	'0'	'0'	'0'	'0'	'0'
Program suspended	'1'	X <sup>(1)</sup>	'0'	'0'	'0'	'1'	'0'
Program completed successfully	'1'	X <sup>(1)</sup>	'0'	'0'	'0'	'0'	'0'
Program failure due to V <sub>PP</sub> Error	'1'	X <sup>(1)</sup>	'0'	'0'	'1'	'0'	'0'
Program failure due to Block Protection (LPC Interface only)	'1'	X <sup>(1)</sup>	'0'	'0'	'0'	'0'	'1'
Program failure due to cell failure	'1'	X <sup>(1)</sup>	'0'	'1'	'0'	'0'	'0'
Erase active	'0'	'0'	'0'	'0'	'0'	'0'	'0'
Block Erase suspended	'1'	'1'	'0'	'0'	'0'	'0'	'0'
Erase completed successfully	'1'	'0'	'0'	'0'	'0'	'0'	'0'
Erase failure due to V <sub>PP</sub> Error	'1'	'0'	'0'	'0'	'1'	'0'	'0'
Block Erase failure due to Block Protection (LPC Interface only)	'1'	'0'	'0'	'0'	'0'	'0'	'1'
Erase failure due to failed cell(s)	'1'	'0'	'1'	'0'	'0'	'0'	'0'

Note: 1. For Program operations during Erase Suspend Bit 6 is '1', otherwise Bit 6 is '0'.

## LOW PIN COUNT (LPC) INTERFACE CONFIGURATION REGISTERS

When the Low Pin Count Interface is selected several additional registers can be accessed. These registers control the protection status of the Blocks and read the General Purpose Input pins. See [Table 12](#).

[Figure 12](#) for an example of the Register Configuration map, valid for the boot memory, i.e. ID0-ID1 floating or driven LOW,  $V_{IL}$  and A20-A21 set to '1'.

**Table 12. Low Pin Count Register Configuration Map <sup>(1)</sup>**

Mnemonic	Register Name	Memory Address	Default Value	Access
T_BLOCK_LK	Top Block Lock Register (Block 15)	FFBF0002h	01h	R/W
T_MINUS01_LK	Top Block [-1] Lock Register (Block 14)	FFBE0002h	01h	R/W
T_MINUS02_LK	Top Block [-2] Lock Register (Block 13)	FFBD0002h	01h	R/W
T_MINUS03_LK	Top Block [-3] Lock Register (Block 12)	FFBC0002h	01h	R/W
T_MINUS04_LK	Top Block [-4] Lock Register (Block 11)	FFBB0002h	01h	R/W
T_MINUS05_LK	Top Block [-5] Lock Register (Block 10)	FFBA0002h	01h	R/W
T_MINUS06_LK	Top Block [-6] Lock Register (Block 9)	FFB90002h	01h	R/W
T_MINUS07_LK	Top Block [-7] Lock Register (Block 8)	FFB80002h	01h	R/W
T_MINUS08_LK	Top Block [-8] Lock Register (Block 7)	FFB70002h	01h	R/W
T_MINUS09_LK	Top Block [-9] Lock Register (Block 6)	FFB60002h	01h	R/W
T_MINUS10_LK	Top Block [-10] Lock Register (Block 5)	FFB50002h	01h	R/W
T_MINUS11_LK	Top Block [-11] Lock Register (Block 4)	FFB40002h	01h	R/W
T_MINUS12_LK	Top Block [-12] Lock Register (Block 3)	FFB30002h	01h	R/W
T_MINUS13_LK	Top Block [-13] Lock Register (Block 2)	FFB20002h	01h	R/W
T_MINUS14_LK	Top Block [-14] Lock Register (Block 1)	FFB10002h	01h	R/W
T_MINUS15_LK	Top Block [-15] Lock Register (Block 0)	FFB00002h	01h	R/W
GPI_REG	General Purpose Input Register	FFBC0100h	N/A	R

Note: 1. This map is referred to the boot memory (ID0-ID1 floating or driven, LOW,  $V_{IL}$  and A20-A21 set to '1').

### Lock Registers

The Lock Registers control the protection status of the Blocks. Each Block has its own Lock Register. Three bits within each Lock Register control the protection of each block, the Write Lock Bit, the Read Lock Bit and the Lock Down Bit.

The Lock Registers can be read and written, though care should be taken when writing as, once the Lock Down Bit is set, '1', further modifications to the Lock Register cannot be made until cleared, to '0', by a reset or power-up.

See [Table 13](#) for details on the bit definitions of the Lock Registers.

**Write Lock.** The Write Lock Bit determines whether the contents of the Block can be modified (using the Program or Block Erase Command). When the Write Lock Bit is set, '1', the block is write protected; any operations that attempt to change the data in the block will fail and the Status Register will report the error. When the Write Lock Bit is reset, '0', the block is not write protected

through the Lock Register and may be modified unless write protected through some other means.

When  $V_{PP}$  is less than  $V_{PPLK}$  all blocks are protected and cannot be modified, regardless of the state of the Write Lock Bit. If Top Block Lock,  $\overline{TBL}$ , is Low,  $V_{IL}$ , then the Top Block (Block 15) is write protected and cannot be modified. Similarly, if Write Protect,  $\overline{WP}$ , is Low,  $V_{IL}$ , then the Main Blocks (Blocks 0 to 14) are write protected and cannot be modified.

After power-up or reset the Write Lock Bit is always set to '1' (write protected).

**Read Lock.** The Read Lock bit determines whether the contents of the Block can be read (from Read mode). When the Read Lock Bit is set, '1', the block is read protected; any operation that attempts to read the contents of the block will read 00h instead. When the Read Lock Bit is reset, '0', read operations in the Block return the data programmed into the block as expected.

After power-up or reset the Read Lock Bit is always reset to '0' (not read protected).

**Lock Down.** The Lock Down Bit provides a mechanism for protecting software data from simple hacking and malicious attack. When the Lock Down Bit is set, '1', further modification to the Write Lock, Read Lock and Lock Down Bits cannot be performed. A reset or power-up is required before changes to these bits can be made. When the Lock Down Bit is reset, '0', the Write Lock, Read Lock and Lock Down Bits can be changed.

**General Purpose Input Register**

The General Purpose Input Register holds the state of the General Purpose Input pins, GPIO-GPI4. When this register is read, the state of these pins is returned. This register is read-only and writing to it has no effect.

The signals on the General Purpose Input pins should remain constant throughout the whole Bus Read cycle in order to guarantee that the correct data is read.

**Table 13. Lock Register Bit Definitions**

Bit	Bit Name	Value	Function
7-3			Reserved
2	Read-Lock	'1'	Bus Read operations in this Block always return 00h.
		'0'	Bus read operations in this Block return the Memory Array contents. (Default value).
1	Lock-Down	'1'	Changes to the Read-Lock bit and the Write-Lock bit cannot be performed. Once a '1' is written to the Lock-Down bit it cannot be cleared to '0'; the bit is always reset to '0' following a Reset (using RP or INIT) or after power-up.
		'0'	Read-Lock and Write-Lock can be changed by writing new values to them. (Default value).
0	Write-Lock	'1'	Program and Block Erase operations in this Block will set an error in the Status Register. The memory contents will not be changed. (Default value).
		'0'	Program and Block Erase operations in this Block are executed and will modify the Block contents.

Note: Applies to Top Block Lock Register (T\_BLOCK\_LK) and Top Block [-1] Lock Register (T\_MINUS01\_LK) to Top Block [-15] Lock Register (T\_MINUS15\_LK).

**Table 14. General Purpose Input Register Definition**

Bit	Bit Name	Value	Function
7-5			Reserved
4	GPI4	'1'	Input Pin GPI4 is at V <sub>IH</sub>
		'0'	Input Pin GPI4 is at V <sub>IL</sub>
3	GPI3	'1'	Input Pin GPI3 is at V <sub>IH</sub>
		'0'	Input Pin GPI3 is at V <sub>IL</sub>
2	GPI2	'1'	Input Pin GPI2 is at V <sub>IH</sub>
		'0'	Input Pin GPI2 is at V <sub>IL</sub>
1	GPI1	'1'	Input Pin GPI1 is at V <sub>IH</sub>
		'0'	Input Pin GPI1 is at V <sub>IL</sub>
0	GPIO	'1'	Input Pin GPIO is at V <sub>IH</sub>
		'0'	Input Pin GPIO is at V <sub>IL</sub>

Note: Applies to the General Purpose Input Register (GPI\_REG).

## PROGRAM AND ERASE TIMES

The Program and Erase times are shown in [Table 15.](#)

**Table 15. Program and Erase Times**

Parameter	Interface	Test Condition	Min	Typ <sup>(1)</sup>	Max	Unit
Byte Program				10	200	μs
Quadruple Byte Program	A/A Mux	$V_{PP} = 12V \pm 5\%$		10	200	μs
Chip Erase	A/A Mux	$V_{PP} = 12V \pm 5\%$		9		sec
Block Program	A/A Mux	$V_{PP} = 12V \pm 5\%$		0.1 <sup>(2)</sup>	5	sec
		$V_{PP} = V_{CC}$		0.4	5	sec
Block Erase		$V_{PP} = 12V \pm 5\%$		0.75	8	sec
		$V_{PP} = V_{CC}$		1	10	sec
Program/Erase Suspend to Program pause <sup>(3)</sup>					5	μs
Program/Erase Suspend to Block Erase pause <sup>(3)</sup>					30	μs

Note: 1.  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V}$

2. This time is obtained executing the Quadruple Byte Program Command.

3. Sampled only, not 100% tested.

**MAXIMUM RATING**

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 16. Absolute Maximum Ratings**

Symbol	Parameter	Min.	Max.	Unit
T <sub>STG</sub>	Storage Temperature	-65	150	°C
T <sub>LEAD</sub>	Lead Temperature during Soldering	See note <sup>1</sup>		°C
V <sub>IO</sub>	Input or Output range <sup>2</sup>	-0.60	V <sub>CC</sub> + 0.6	V
V <sub>CC</sub>	Supply Voltage	-0.60	4	V
V <sub>PP</sub>	Program Voltage	-0.6	13	V
V <sub>ESD</sub>	Electrostatic Discharge Voltage (Human Body model) <sup>3</sup>	-2000	2000	V

- Note: 1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK<sup>®</sup> 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU  
 2. Minimum voltage may undershoot to -2V for less than 20ns during transitions. Maximum voltage may overshoot to V<sub>CC</sub> + 2V for less than 20ns during transitions.  
 3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)



## DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement

Conditions summarized in [Table 17.](#), [Table 18.](#) and [Table 19.](#) Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 17. Operating Conditions**

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Supply Voltage	3.0	3.6	V
$T_A$	Ambient Operating Temperature (Device Grade 1)	0	70	°C
	Ambient Operating Temperature (Device Grade 5)	-20	85	°C

**Table 18. LPC Interface AC Measurement Conditions**

Parameter	Value	Unit
Load Capacitance ( $C_L$ )	10	pF
Input Rise and Fall Times	$\leq 1.4$	ns
Input Pulse Voltages	$0.2 V_{CC}$ and $0.6 V_{CC}$	V
Input and Output Timing Ref. Voltages	$0.4 V_{CC}$	V

**Table 19. A/A Mux Interface AC Measurement Conditions**

Parameter	Value	Unit
Load Capacitance ( $C_L$ )	30	pF
Input Rise and Fall Times	$\leq 10$	ns
Input Pulse Voltages	0 to 3	V
Input and Output Timing Ref. Voltages	1.5	V

**Figure 8. LPC Interface AC Testing Input Output Waveforms**

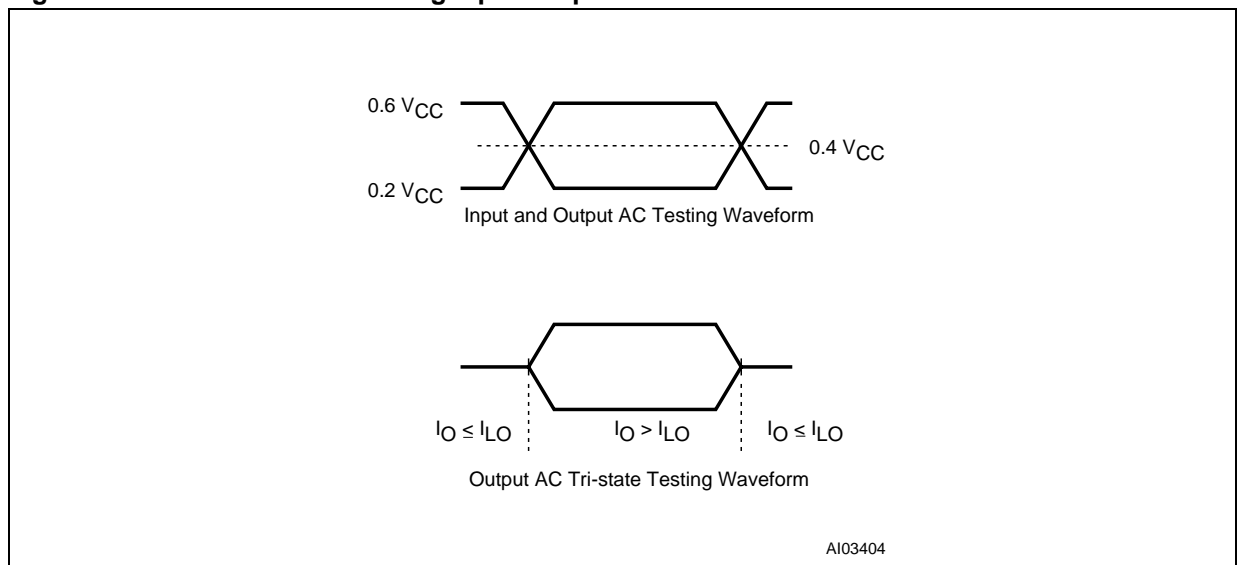


Figure 9. A/A Mux Interface AC Testing Input Output Waveform

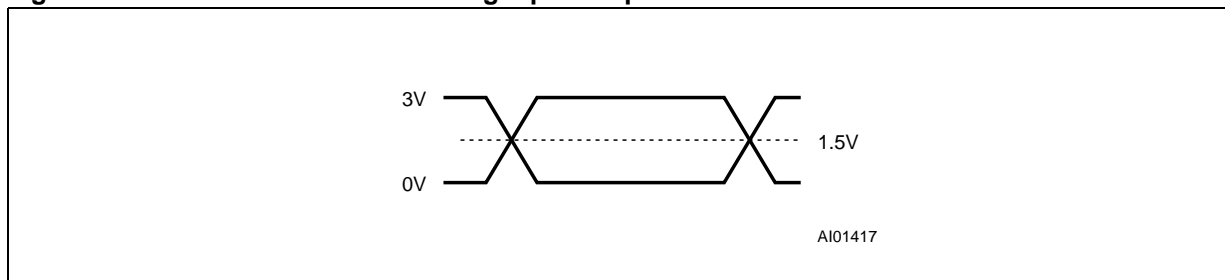


Table 20. Impedance

Symbol	Parameter	Test Condition <sup>(3)</sup>	Min	Max	Unit
$C_{IN}^{(1)}$	Input Capacitance	$V_{IN} = 0V$		13	pF
$C_{CLK}^{(1)}$	Clock Capacitance	$V_{IN} = 0V$	3	12	pF
$L_{PIN}^{(2)}$	Recommended Pin Inductance			20	nH

Note: 1. Sampled only, not 100% tested.

2. See PCI Specification.

3.  $T_A = 25^{\circ}C$ ,  $f = 1MHz$ .

Table 21. DC Characteristics

Symbol	Parameter	Interface	Test Condition	Min	Max	Unit
$V_{IH}$	Input High Voltage	LPC		$0.5 V_{CC}$	$V_{CC} + 0.5$	V
		A/A Mux		$0.7 V_{CC}$	$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	LPC		-0.5	$0.3 V_{CC}$	V
		A/A Mux		-0.5	0.8	V
$V_{IH}(\overline{INIT})$	$\overline{INIT}$ Input High Voltage	LPC		1.35	$V_{CC} + 0.5$	V
$V_{IL}(\overline{INIT})$	$\overline{INIT}$ Input Low Voltage	LPC		-0.5	$0.2 V_{CC}$	V
$I_{LI}^{(2)}$	Input Leakage Current		$0V \leq V_{IN} \leq V_{CC}$		$\pm 10$	$\mu A$
$I_{LI2}$	IC, IDx Input Leakage Current		IC, ID0, ID1 = $V_{CC}$		200	$\mu A$
$R_{IL}$	IC, IDx Input Pull Low Resistor			20	100	k $\Omega$
$V_{OH}$	Output High Voltage	LPC	$I_{OH} = -500\mu A$	$0.9 V_{CC}$		V
		A/A Mux	$I_{OH} = -100\mu A$	$V_{CC} - 0.4$		V
$V_{OL}$	Output Low Voltage	LPC	$I_{OL} = 1.5mA$		$0.1 V_{CC}$	V
		A/A Mux	$I_{OL} = 1.8mA$		0.45	V
$I_{LO}$	Output Leakage Current		$0V \leq V_{OUT} \leq V_{CC}$		$\pm 10$	$\mu A$
$V_{PP1}$	$V_{PP}$ Voltage			3	3.6	V
$V_{PPH}$	$V_{PP}$ Voltage (Fast Program/Fast Erase)			11.4	12.6	V
$V_{PPLK}^{(1)}$	$V_{PP}$ Lockout Voltage			1.5		V
$V_{LKO}^{(1)}$	$V_{CC}$ Lockout Voltage			1.8	2.3	V
$I_{CC1}$	Supply Current (Standby)	LPC	$\overline{LFRAME} = 0.9 V_{CC}$ , $V_{PP} = V_{CC}$ All other inputs $0.9 V_{CC}$ to $0.1 V_{CC}$ $V_{CC} = 3.6V$ , $f(CLK) = 33MHz$		100	$\mu A$
$I_{CC2}$	Supply Current (Standby)	LPC	$\overline{LFRAME} = 0.1 V_{CC}$ , $V_{PP} = V_{CC}$ All other inputs $0.9 V_{CC}$ to $0.1 V_{CC}$ $V_{CC} = 3.6V$ , $f(CLK) = 33MHz$		10	mA
$I_{CC3}$	Supply Current (Any internal operation active)	LPC	$V_{CC} = V_{CC} \text{ max}$ , $V_{PP} = V_{CC}$ $f(CLK) = 33MHz$ $I_{OUT} = 0mA$		60	mA
$I_{CC4}$	Supply Current (Read)	A/A Mux	$\overline{G} = V_{IH}$ , $f = 6MHz$		20	mA
$I_{CC5}^{(1)}$	Supply Current (Program/Erase)	A/A Mux	Program/Erase Controller Active		20	mA
$I_{PP}$	$V_{PP}$ Supply Current (Read/Standby)		$V_{PP} \geq V_{CC}$		400	$\mu A$
$I_{PP1}^{(1)}$	$V_{PP}$ Supply Current (Program/Erase active)		$V_{PP} = V_{CC}$		40	mA
			$V_{PP} = 12V \pm 5\%$		15	mA

Note: 1. Sampled only, not 100% tested.

2. Input leakage currents include High-Z output leakage for all bi-directional buffers with tri-state outputs.

Figure 10. LPC Interface Clock Waveform

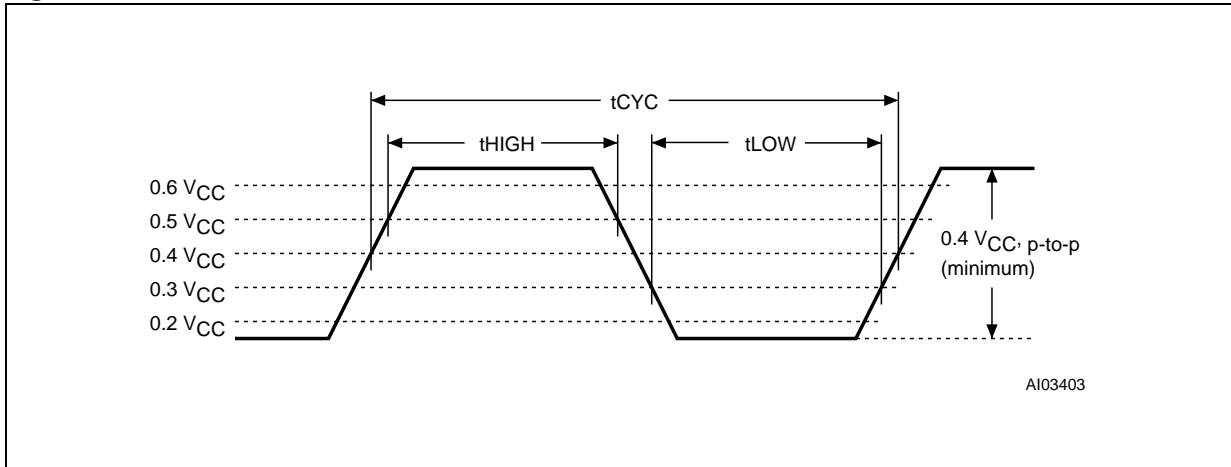


Table 22. LPC Interface Clock Characteristics

Symbol	Parameter	Test Condition		Value	Unit
t <sub>CYC</sub>	CLK Cycle Time <sup>(1)</sup>		Min	30	ns
t <sub>HIGH</sub>	CLK High Time		Min	11	ns
t <sub>LOW</sub>	CLK Low Time		Min	11	ns
	CLK Slew Rate	peak to peak	Min	1	V/ns
			Max	4	V/ns

Note: 1. Devices on the PCI Bus must work with any clock frequency between DC and 33MHz. Below 16MHz devices may be guaranteed by design rather than tested. Refer to PCI Specification.

Figure 11. LPC Interface AC Signal Timing Waveforms

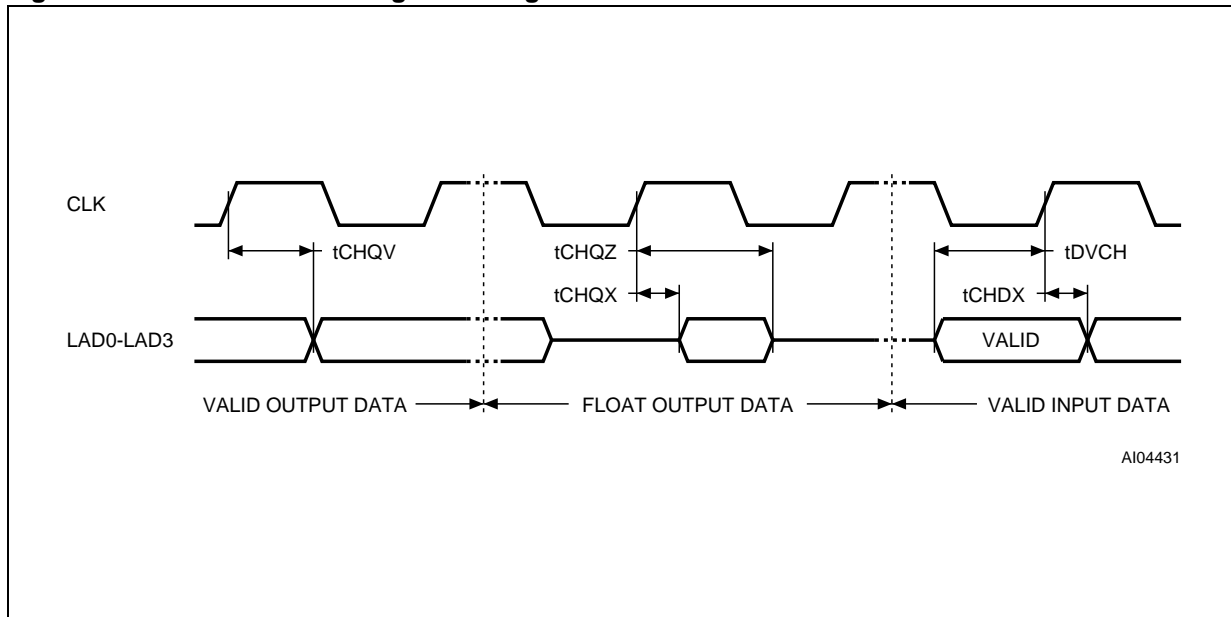


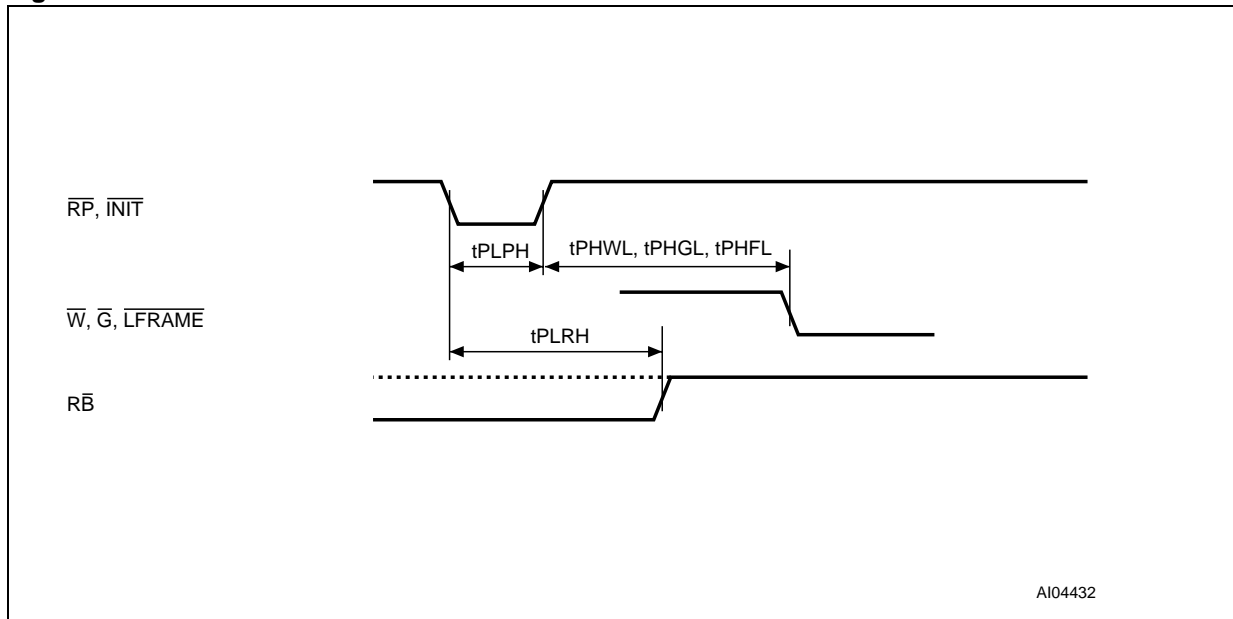
Table 23. LPC Interface AC Signal Timing Characteristics

Symbol	PCI Symbol	Parameter	Test Condition		Value	Unit
$t_{\text{CHQV}}$	$t_{\text{val}}$	CLK to Data Out		Min	2	ns
				Max	11	ns
$t_{\text{CHQX}}^{(1)}$	$t_{\text{on}}$	CLK to Active (Float to Active Delay)		Min	2	ns
$t_{\text{CHQZ}}$	$t_{\text{off}}$	CLK to Inactive (Active to Float Delay)		Max	28	ns
$t_{\text{AVCH}}$ $t_{\text{DVCH}}$	$t_{\text{su}}$	Input Set-up Time <sup>(2)</sup>		Min	7	ns
$t_{\text{CHAX}}$ $t_{\text{CHDX}}$	$t_{\text{h}}$	Input Hold Time <sup>(2)</sup>		Min	0	ns

Note: 1. The timing measurements for Active/Float transitions are defined when the current through the pin equals the leakage current specification.

2. Applies to all inputs except CLK.

Figure 12. Reset AC Waveforms



AI04432

Table 24. Reset AC Characteristics

Symbol	Parameter	Test Condition		Value	Unit
$t_{PLPH}$	$\overline{RP}$ or $\overline{INIT}$ Reset Pulse Width		Min	100	ns
$t_{PLRH}$	$\overline{RP}$ or $\overline{INIT}$ Low to Reset	Program/Erase Inactive	Max	100	ns
		Program/Erase Active	Max	30	$\mu$ s
	$\overline{RP}$ or $\overline{INIT}$ Slew Rate <sup>(1)</sup>	Rising edge only	Min	50	mV/ns
$t_{PHFL}$	$\overline{RP}$ or $\overline{INIT}$ High to $\overline{LFRAME}$ Low	LPC Interface only	Min	30	$\mu$ s
$t_{PHWL}$ $t_{PHGL}$	$\overline{RP}$ High to Write Enable or Output Enable Low	A/A Mux Interface only	Min	50	$\mu$ s

Note: 1. See Chapter 4 of the PCI Specification.

Figure 13. A/A Mux Interface Read AC Waveforms

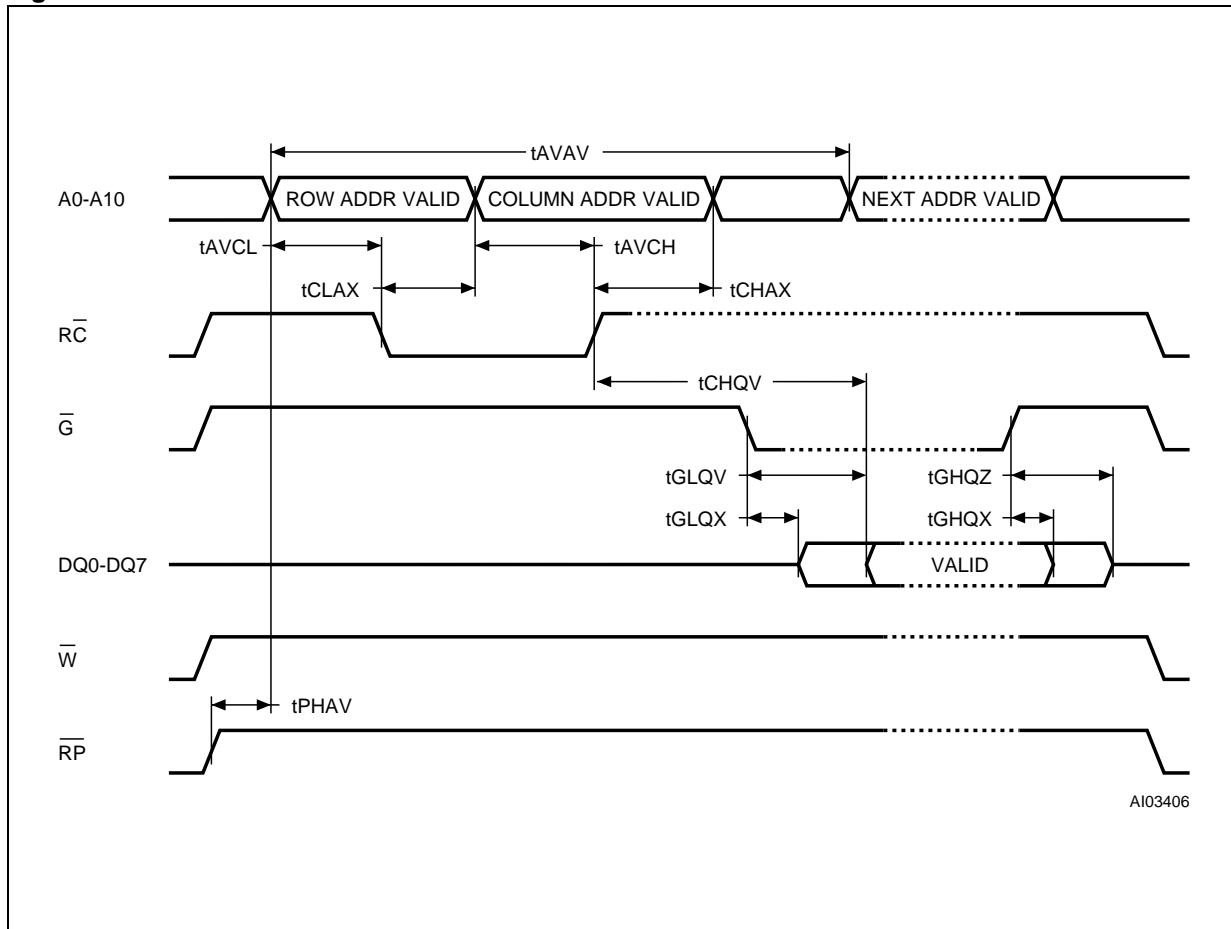
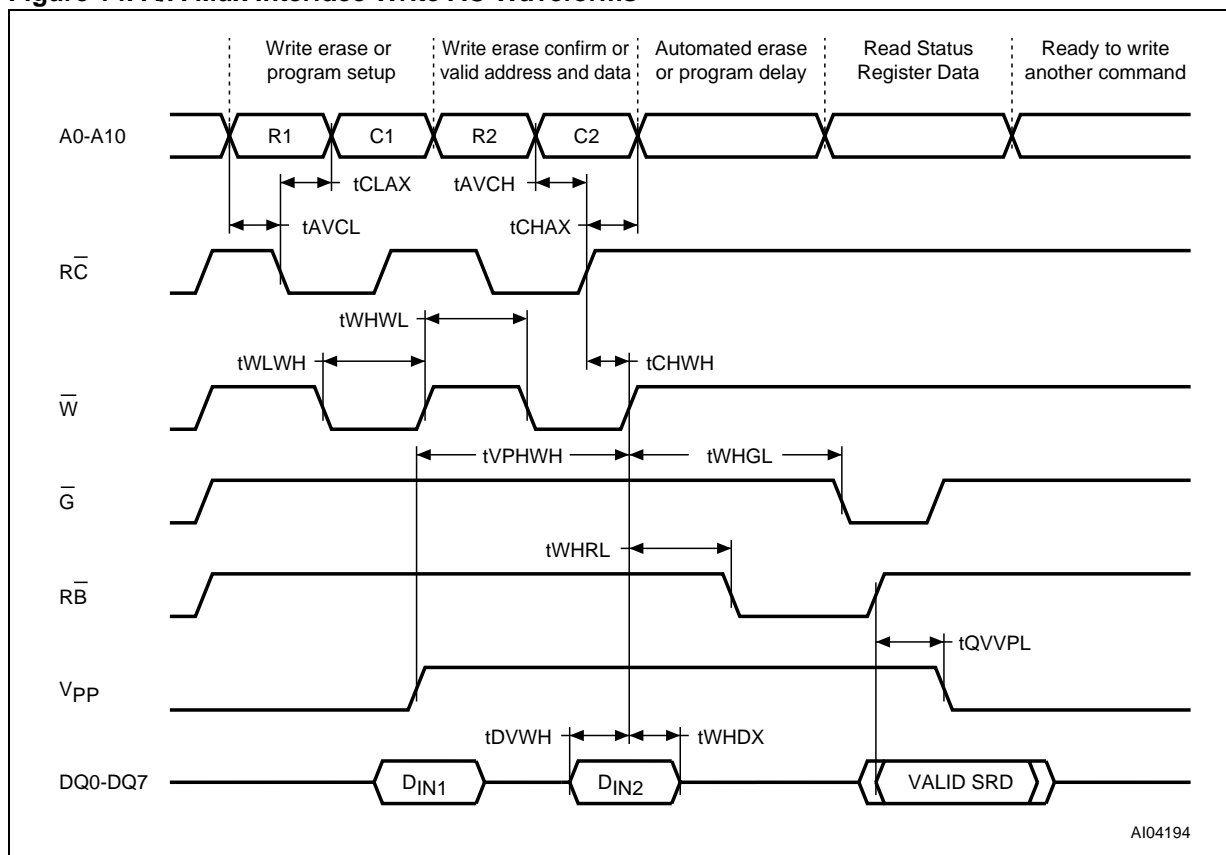


Table 25. A/A Mux Interface Read AC Characteristics

Symbol	Parameter	Test Condition	Value	Unit
$t_{AVAV}$	Read Cycle Time	Min	250	ns
$t_{AVCL}$	Row Address Valid to $\overline{RC}$ Low	Min	50	ns
$t_{CLAX}$	$\overline{RC}$ Low to Row Address Transition	Min	50	ns
$t_{AVCH}$	Column Address Valid to $\overline{RC}$ high	Min	50	ns
$t_{CHAX}$	$\overline{RC}$ High to Column Address Transition	Min	50	ns
$t_{CHQV}^{(1)}$	$\overline{RC}$ High to Output Valid	Max	150	ns
$t_{GLQV}^{(1)}$	Output Enable Low to Output Valid	Max	50	ns
$t_{PHAV}$	$\overline{RP}$ High to Row Address Valid	Min	1	$\mu$ s
$t_{GLQX}$	Output Enable Low to Output Transition	Min	0	ns
$t_{GHQZ}$	Output Enable High to Output Hi-Z	Max	50	ns
$t_{GHQX}$	Output Hold from Output Enable High	Min	0	ns

Note: 1.  $\overline{G}$  may be delayed up to  $t_{CHQV} - t_{GLQV}$  after the rising edge of  $\overline{RC}$  without impact on  $t_{CHQV}$ .

Figure 14. A/A Mux Interface Write AC Waveforms



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Table 26. A/A Mux Interface Write AC Characteristics

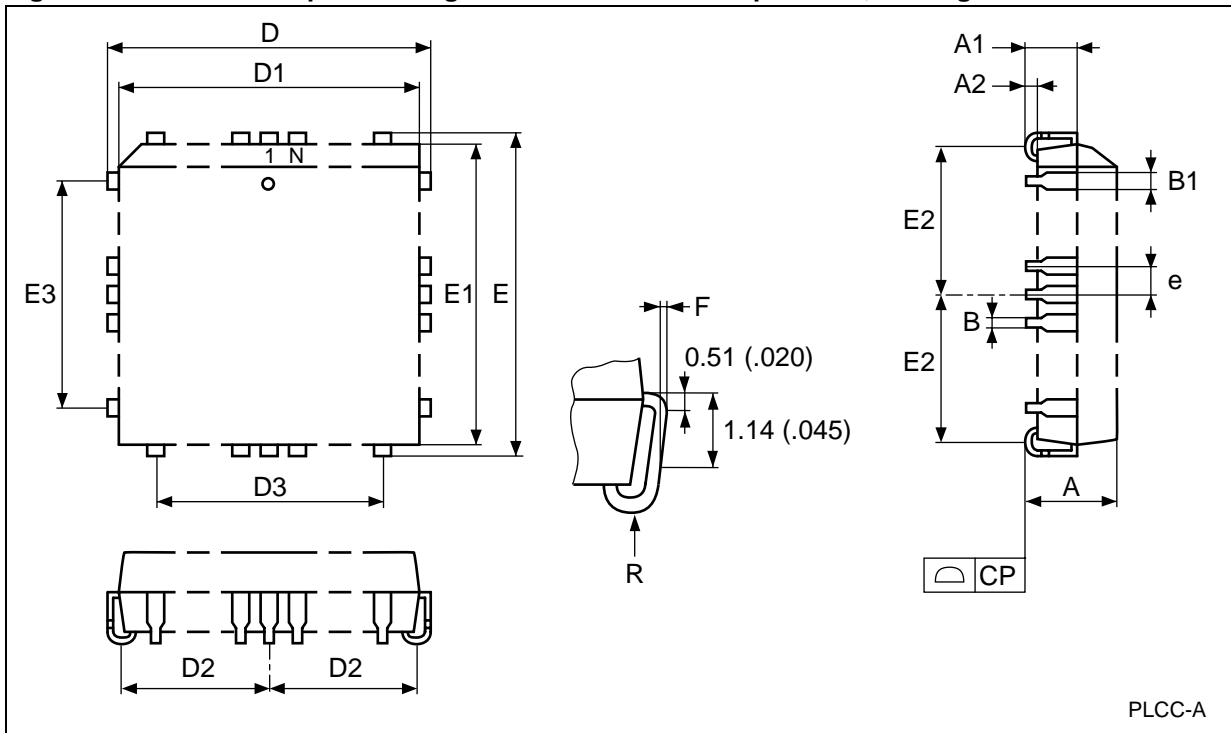
Symbol	Parameter	Test Condition	Value	Unit
t <sub>WLWH</sub>	Write Enable Low to Write Enable High	Min	100	ns
t <sub>DVWH</sub>	Data Valid to Write Enable High	Min	50	ns
t <sub>WHDX</sub>	Write Enable High to Data Transition	Min	5	ns
t <sub>AVCL</sub>	Row Address Valid to $\overline{RC}$ Low	Min	50	ns
t <sub>CLAX</sub>	$\overline{RC}$ Low to Row Address Transition	Min	50	ns
t <sub>AVCH</sub>	Column Address Valid to $\overline{RC}$ High	Min	50	ns
t <sub>CHAX</sub>	$\overline{RC}$ High to Column Address Transition	Min	50	ns
t <sub>WHWL</sub>	Write Enable High to Write Enable Low	Min	100	ns
t <sub>CHWH</sub>	$\overline{RC}$ High to Write Enable High	Min	50	ns
t <sub>VPHWH</sub> <sup>(1)</sup>	V <sub>PP</sub> High to Write Enable High	Min	100	ns
t <sub>WHGL</sub>	Write Enable High to Output Enable Low	Min	30	ns
t <sub>WHRL</sub>	Write Enable High to $\overline{RB}$ Low	Min	0	ns
t <sub>QVPL</sub> <sup>(1,2)</sup>	Output Valid, $\overline{RB}$ High to V <sub>PP</sub> Low	Min	0	ns

Note: 1. Sampled only, not 100% tested.  
 2. Applicable if V<sub>PP</sub> is seen as a logic input (V<sub>PP</sub> < 3.6V).



PACKAGE MECHANICAL

Figure 15. PLCC32 – 32 pin Rectangular Plastic Leaded Chip Carrier, Package Outline

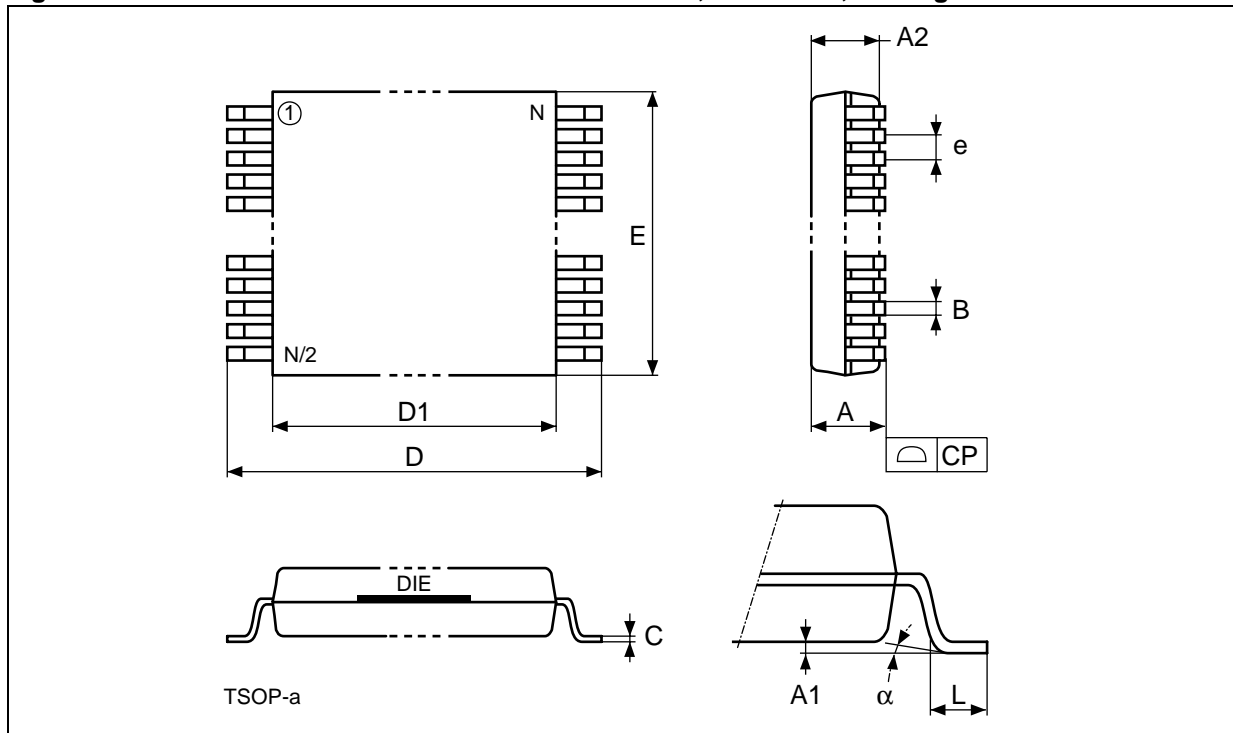


Note: Drawing is not to scale.

**Table 27. PLCC32 – 32 pin Rectangular Plastic Leaded Chip Carrier, Package Mechanical Data**

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.18	3.56		0.125	0.140
A1		1.53	2.41		0.060	0.095
A2		0.38	–		0.015	–
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
CP			0.10			0.004
D		12.32	12.57		0.485	0.495
D1		11.35	11.51		0.447	0.453
D2		4.78	5.66		0.188	0.223
D3	7.62	–	–	0.300	–	–
E		14.86	15.11		0.585	0.595
E1		13.89	14.05		0.547	0.553
E2		6.05	6.93		0.238	0.273
E3	10.16	–	–	0.400	–	–
e	1.27	–	–	0.050	–	–
F		0.00	0.13		0.000	0.005
R	0.89	–	–	0.035	–	–
N		32			32	

Figure 16. TSOP40 – 40 lead Plastic Thin Small Outline, 10x20 mm, Package Outline



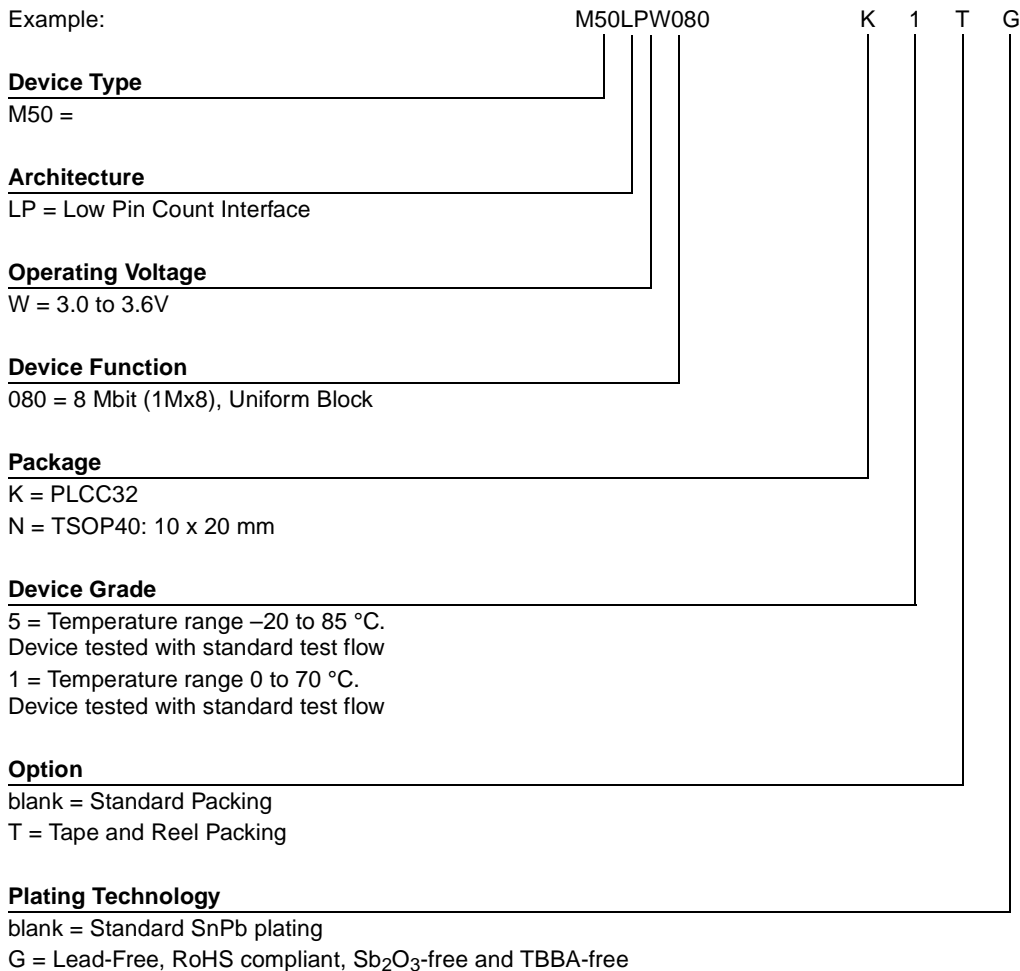
Note: Drawing is not to scale.

Table 28. TSOP40 – 40 lead Plastic Thin Small Outline, 10x20 mm, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
B		0.170	0.270		0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.100			0.0039
D		19.800	20.200		0.7795	0.7953
D1		18.300	18.500		0.7205	0.7283
e	0.500	–	–	0.0197	–	–
E		9.900	10.100		0.3898	0.3976
L		0.500	0.700		0.0197	0.0276
$\alpha$		0°	5°		0°	5°
N		40			40	

**PART NUMBERING**

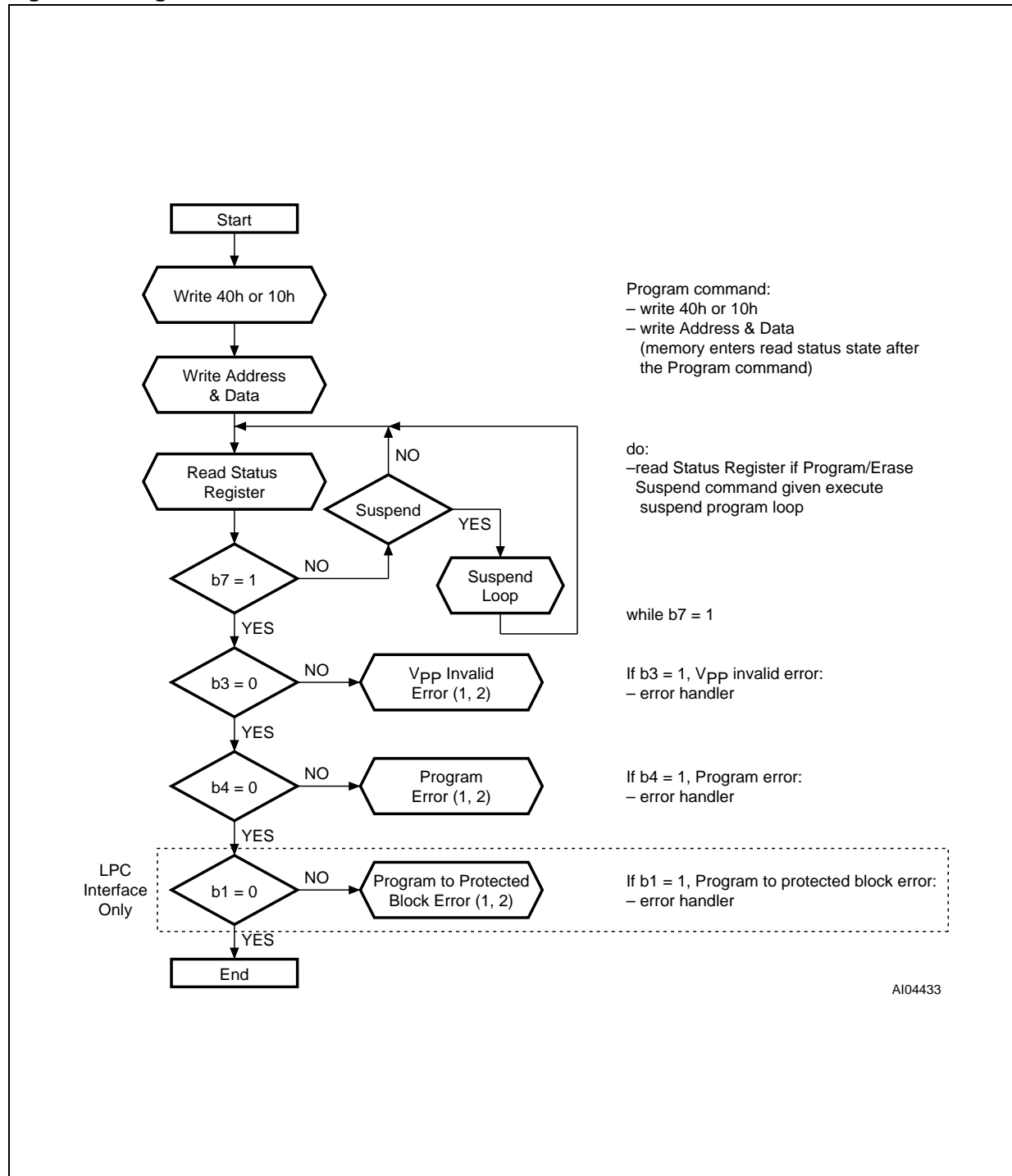
**Table 29. Ordering Information Scheme**



Devices are shipped from the factory with the memory content bits erased to '1'.  
 For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device,  
 please contact your nearest ST Sales Office.

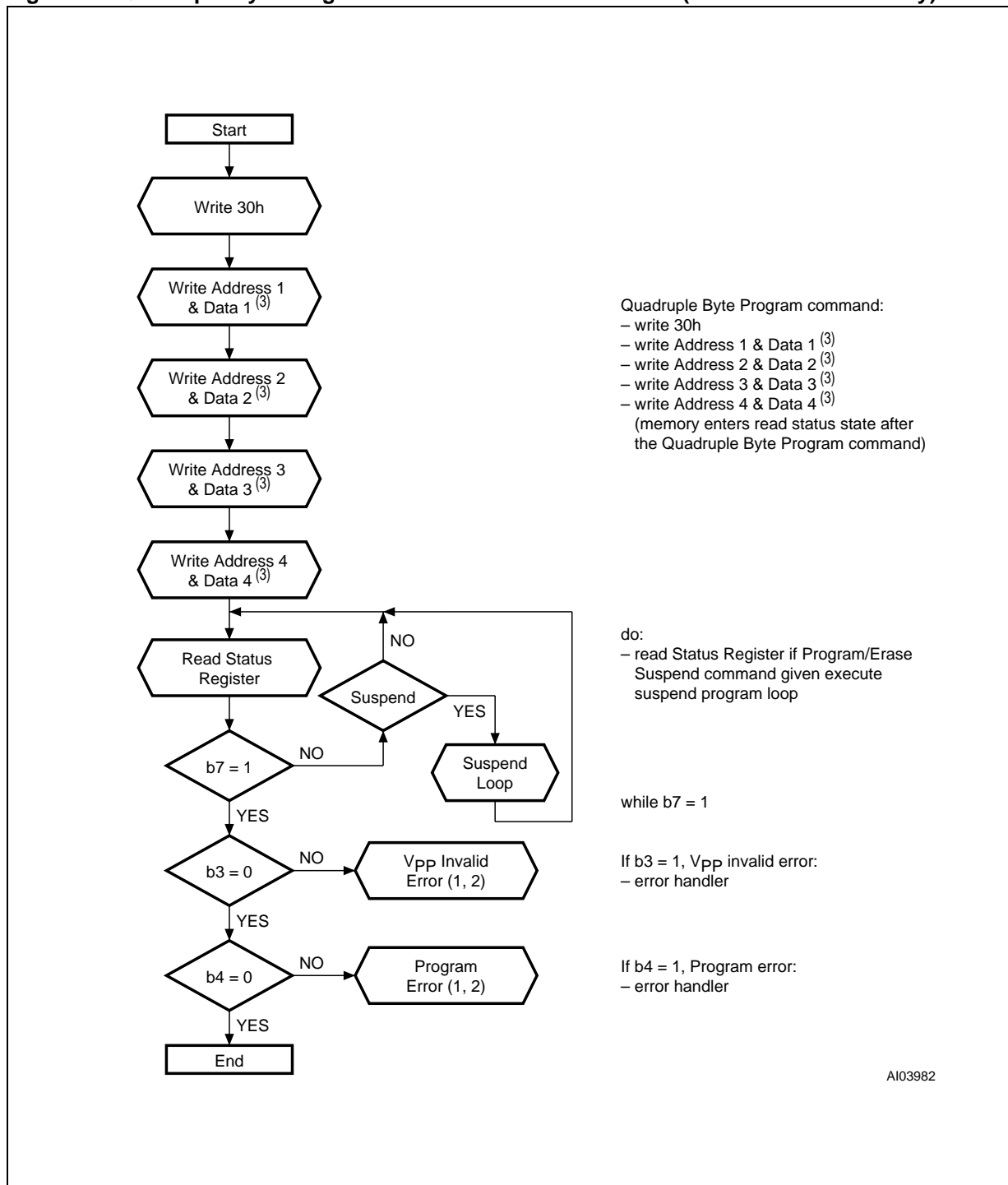
## FLOWCHARTS AND PSEUDO CODES

Figure 17. Program Flowchart and Pseudo Code



Note: 1. A Status check of b1 (Protected Block), b3 (Vpp invalid) and b4 (Program Error) can be made after each Program operation by following the correct command sequence.  
 2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 18. Quadruple Byte Program Flowchart and Pseudo Code (A/A Mux Interface Only)



Note: 1. A Status check of b3 (Vpp invalid) and b4 (Program Error) can be made after each Program operation by following the correct command sequence.  
 2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.  
 3. Address 1, Address 2, Address 3 and Address 4 must be consecutive addresses differing only for address bits A0 and A10.

Figure 19. Program Suspend and Resume Flowchart and Pseudo Code

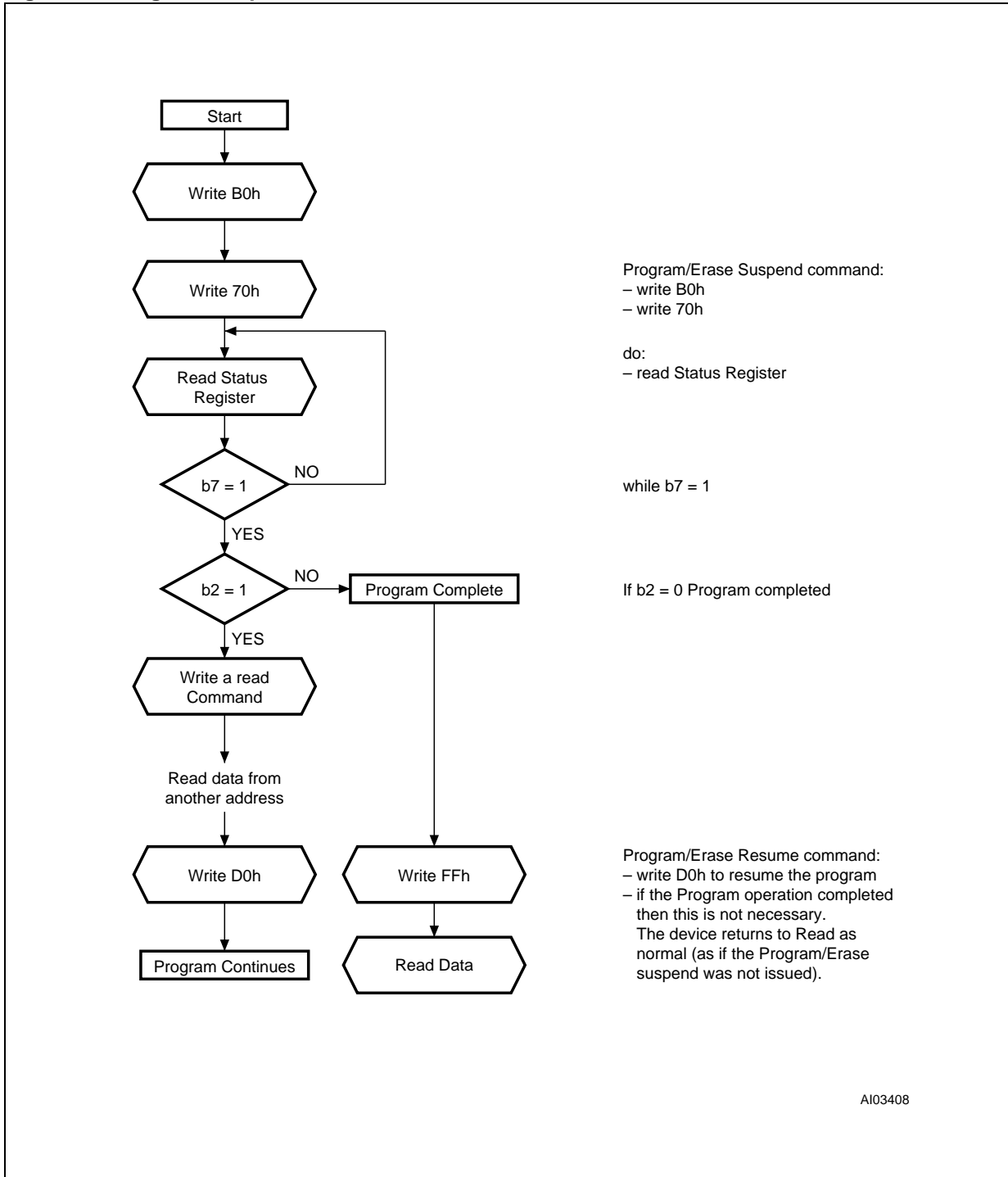
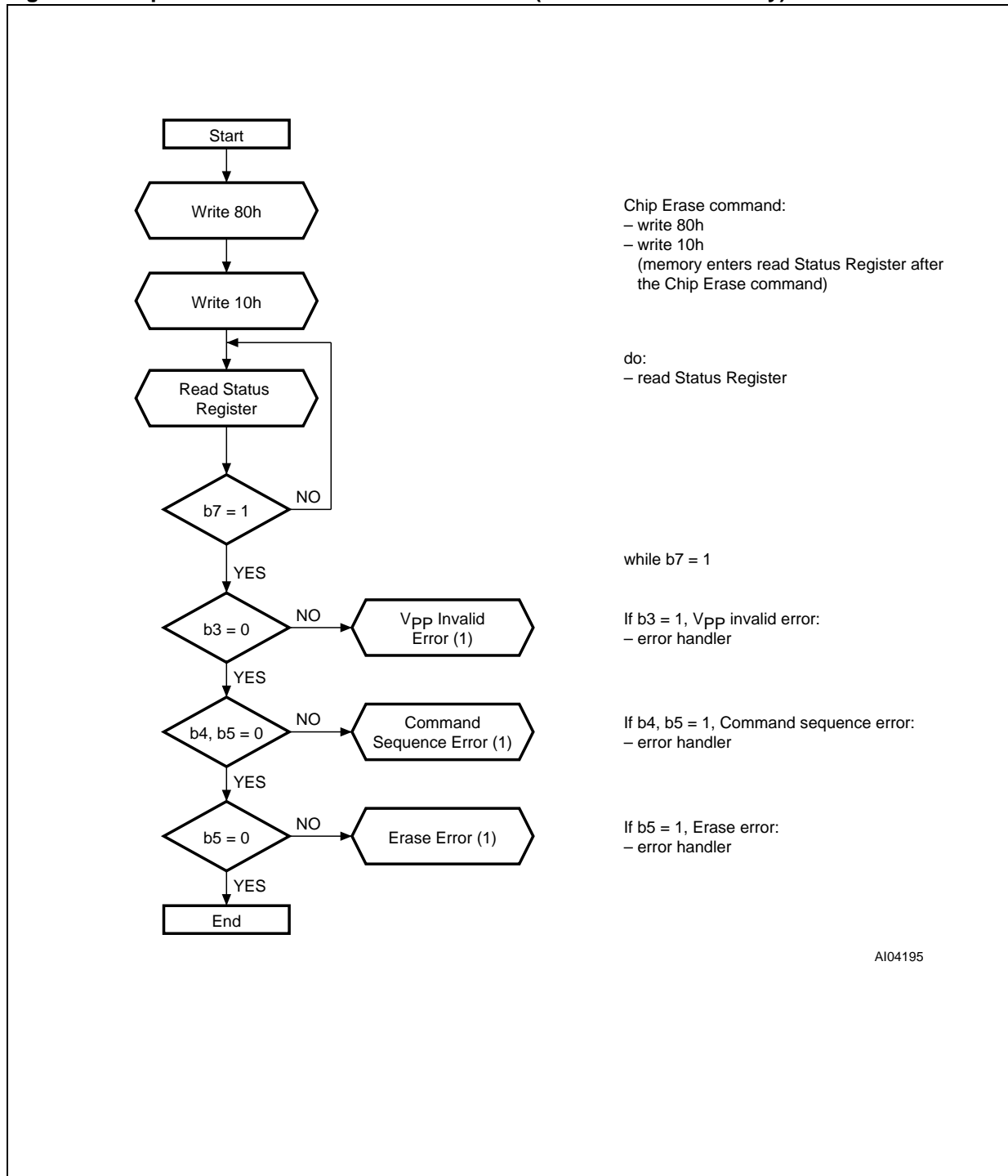


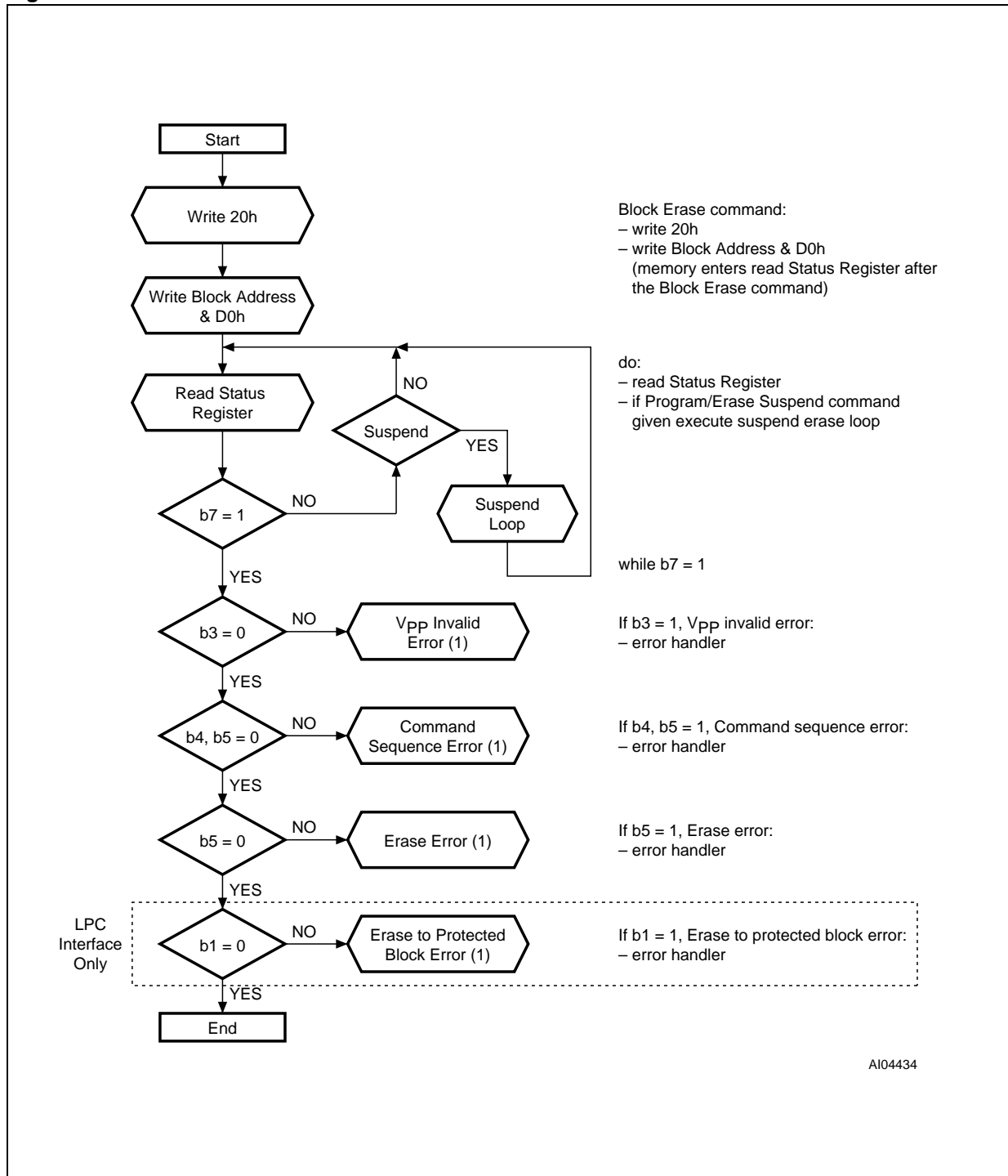
Figure 20. Chip Erase Flowchart and Pseudo Code (A/A Mux Interface Only)



Note: If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

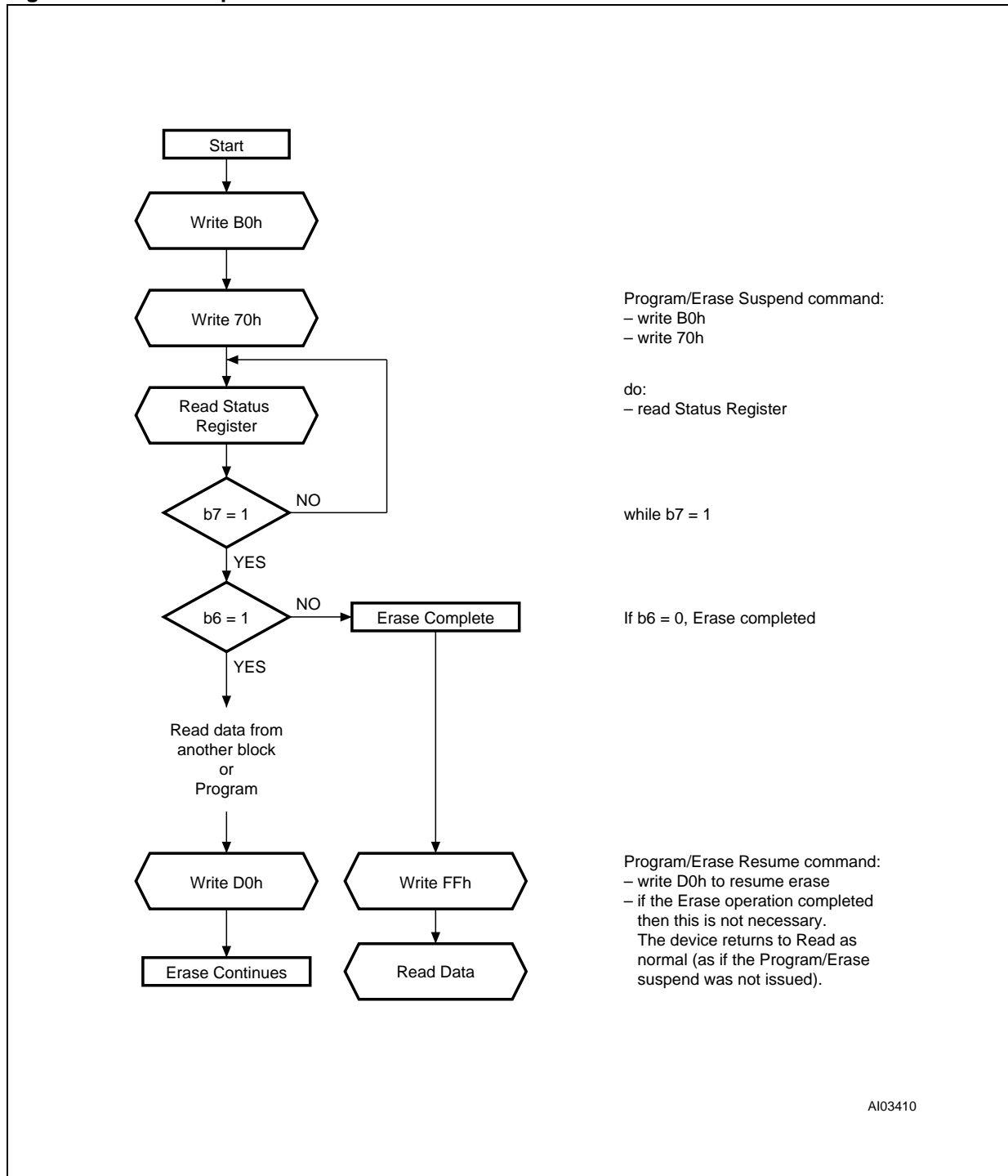


Figure 21. Block Erase Flowchart and Pseudo Code



Note: If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 22. Erase Suspend and Resume Flowchart and Pseudo Code



## REVISION HISTORY

**Table 30. Revision History**

Date	Version	Revision Details
April 2001	-01	First Issue
22-June-2001	-02	Clock Cycle Number 2 changed ( <a href="#">Table 7.</a> and <a href="#">Table 8.</a> ) Low Pin Count Register Configuration Map ( <a href="#">Table 12.</a> ) clarification
03-Sep-2001	-03	PLCC32 package added Note 2 changed under <a href="#">Table 4.</a>
24-Oct-2001	-04	Document Status changed from Product Preview to Preliminary Data $V_{PP}$ Optional Supply Voltage section clarified
12-Mar-2002	-05	RFU pins must be left disconnected Specification of PLCC32 package mechanical data revised
02-Aug-2004	8.0	Revision numbering modified. Document reformatted. Temperature Range ordering information replaced by Device Grade, Standard packing option added and Plating Technology added. $T_{LEAD}$ parameter added to Absolute Maximum Ratings and $T_{BIAS}$ parameter removed. Inch values corrected in TSOP40 package mechanical data.
07-Jul-2005	9.0	Datasheet Status updated to NOT FOR NEW DESIGN.

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