



# High-Speed CMOS 8-Bit Bus Interface Register Transceivers

QS54/74FCT646T  
QS54/74FCT2646T

## FEATURES/BENEFITS

- Pin and function compatible to the 74F646 74FCT646 and 74FCT646T
- CMOS power levels: <7.5mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

### FCT-T 646T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std., A, and C speed grades with 4.8ns  $t_{PD}$  for C
- $I_{OL} = 64mA$  Ind., 48mA Mil.

### FCT-T 2646T

- Built-in 25 $\Omega$  series resistor outputs reduce reflection and other system noise
- Std., A, and C speed grades with 4.8ns  $t_{PD}$  for C
- $I_{OL} = 12mA$  Ind.

## DESCRIPTION

The QSFCT646T and QSFCT2646T are 8-bit high-speed CMOS TTL-compatible registered bus transceivers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2646 device is a 25 $\Omega$  resistor output version useful for driving transmission lines and reducing system noise. The 2646 series parts can replace the 646 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when  $V_{CC}$  is removed from the device.

Figure 1. Functional Block Diagram

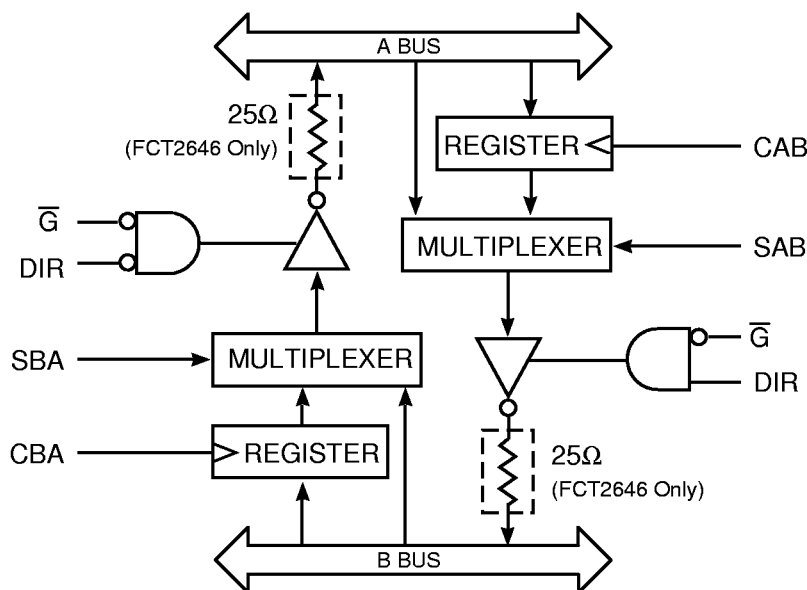
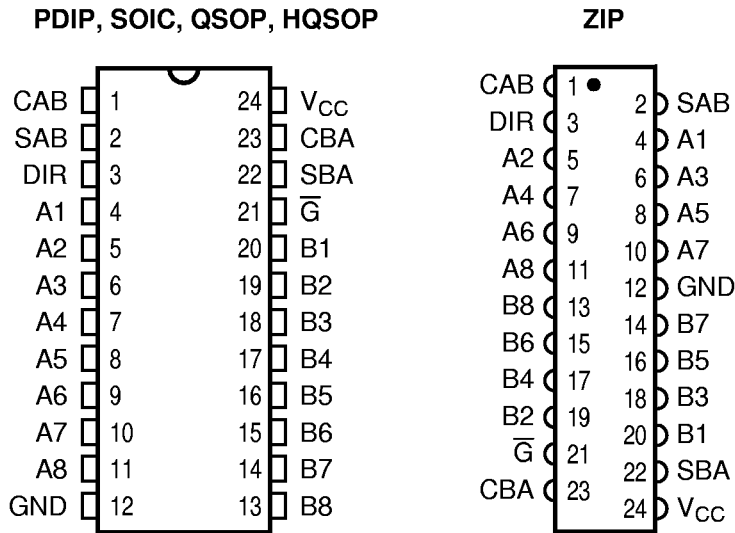


Figure 2. Pin Configurations (All Pins Top View)



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Table 1. Pin Description

Name	I/O	Description
A8-A1	I/O	A Bus
B8-B1	I/O	B Bus
CAB	I	Clock A to Register
CBA	I	Clock B to Register
SAB	I	A Bus or Reg to B
SBA	I	B Bus or Reg to A
DIR	I	Direction, A → B or B → A
$\bar{G}$	I	Output Enable

Table 2. Function Table

Inputs						Outputs		Function
$\bar{G}$	DIR	CAB	CBA	SAB	SBA	A8-A1	B8-B1	
H	—	—	—	—	—	Hi-Z	Hi-Z	Disabled
L	L	—	—	—	—	A	Hi-Z	Output A
L	H	—	—	—	—	Hi-Z	B	Output B
—	—	↑	—	—	—	—	—	Load A Register
—	—	—	↑	—	—	—	—	Load B Register
—	—	—	—	L	—	—	—	A Bus → B Bus
—	—	—	—	H	—	—	—	A Reg → B Bus
—	—	—	—	—	L	—	—	B Bus → A Bus
—	—	—	—	—	H	—	—	B Reg → A Bus

**Table 3. Absolute Maximum Ratings**

Supply Voltage to Ground .....	-0.5V to 7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to 7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to 7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50mA
DC Output Current Max. Sink Current/Pin .....	120mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to 150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

**Table 4. Capacitance**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ ,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
—	4	4	5	7	pF
—	6	6	7	9	pF
1-11, 13-23	8	8	9	10	pF

**Note:** Capacitance is characterized but not tested.

**Table 5. Power Supply Characteristics**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ , $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4\text{V}$ , $\text{freq} = 0$ <sup>(2)</sup>	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ , Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or $V_{CC}$ <sup>(3,4)</sup>	—	0.25	mA/MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

**Table 6. DC Electrical Characteristics Over Operating Range**Industrial  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ 

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current (FCT646)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$I_{OR}$	Current Drive (FCT2646)	$V_{CC} = \text{Max.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -12\text{mA}$ (MIL) $I_{OH} = -15\text{mA}$ (IND)	2.4 2.4	— —	— —	V
$V_{OL}$	Output LOW Voltage (FCT646)	$V_{CC} = \text{Min.}$ $I_{OL} = 48\text{mA}$ (MIL) $I_{OL} = 64\text{mA}$ (IND)	— —	— —	0.55 0.55	V
$V_{OL}$	Output LOW Voltage (FCT2646- 25 $\Omega$ )	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$ (MIL) $I_{OL} = 12\text{mA}$ (IND)	— —	— —	0.50 0.50	V
$R_{OUT}$	Output Resistance (FCT2646- 25 $\Omega$ )	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$ (MIL) $I_{OL} = 12\text{mA}$ (IND)	— 20	25 28	— 40	$\Omega$

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**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

**Table 7. Switching Characteristics Over Operating Range**

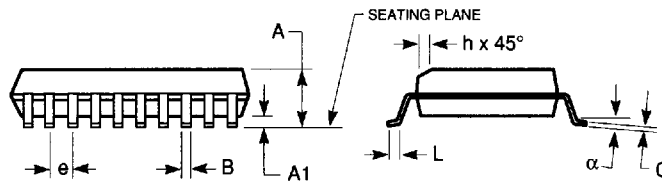
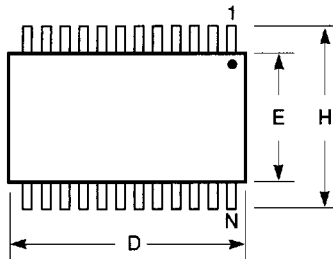
Industrial  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$       Military  $T_A = -55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$   
 $C_{LOAD} = 50\text{pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>		646 2646		646A 2646A		646C 2646C		646D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PHLB}$ $t_{PLHB}$	Bus to Bus Delay, 646	Ind Mil	2.0 2.0	9.0 11	2.0 2.0	6.3 7.7	1.5 1.5	5.4 6.0	1.5 —	4.8 —	ns
$t_{PHLB}$ $t_{PLHB}$	Bus to Bus Delay, 2646	Ind Mil	2.0 2.0	9.0 11	2.0 2.0	6.3 7.7	1.5 1.5	5.4 6.0	1.5 —	4.8 —	ns
$t_{PZH}$ $t_{PZL}$	Ouput Enable Time, 646	Ind Mil	2.0 2.0	14 15	2.0 2.0	9.8 10.5	1.5 1.5	7.8 8.9	1.5 —	7.3 —	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time, 2646	Ind Mil	2.0 2.0	14 15	2.0 2.0	9.8 10.5	1.5 1.5	7.8 8.9	1.5 —	7.3 —	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time	Ind <sup>(2)</sup> Mil <sup>(2)</sup>	2.0 2.0	9.0 11	2.0 2.0	6.3 7.7	1.5 1.5	6.3 7.7	1.5 —	6.3 —	ns
$t_{PHLC}$ $t_{PLHC}$	Clock to Bus Delay, 646	Ind Mil	2.0 2.0	9.0 10	2.0 2.0	6.3 7.0	1.5 1.5	5.7 6.3	1.5 —	5.2 —	ns
$t_{PHLC}$ $t_{PLHC}$	Clock to Bus Delay, 2646	Ind Mil	2.0 2.0	9.0 10	2.0 2.0	6.3 7.0	1.5 1.5	5.7 6.3	1.5 —	5.2 —	ns
$t_{PHLS}$ $t_{PLHS}$	SBA/SAB to Bus Delay, 646	Ind Mil	2.0 2.0	11 12	2.0 2.0	7.7 8.4	1.5 1.5	6.2 7.0	1.5 —	5.8 —	ns
$t_{PHLS}$ $t_{PLHS}$	SBA/SAB to Bus Delay, 2646	Ind Mil	2.0 2.0	11 12	2.0 2.0	7.7 8.4	1.5 1.5	6.2 7.0	1.5 —	5.8 —	ns
$t_S$	Data Setup Time	Ind Mil	4.0 4.5	— —	2.0 2.0	— —	2.0 2.0	— —	2.0 —	— —	ns
$t_H$	Data Hold Time	Ind Mil	2.0 2.0	— —	1.5 1.5	— —	1.5 1.5	— —	1.5 —	— —	ns
$t_{PWH}$ $t_{PWL}$	Clock Pulse Width HIGH or LOW	Ind <sup>(2)</sup> Mil <sup>(2)</sup>	6.0 6.0	— —	5.0 5.0	— —	5.0 5.0	— —	5.0 —	— —	ns

**Notes:**

1. Minimums guaranteed but not tested for all parameters except  $t_S$  and  $t_H$ .
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

**300-MIL SOIC - Package Code SO**  
Plastic Small Outline Gull-Wing



**Notes:**

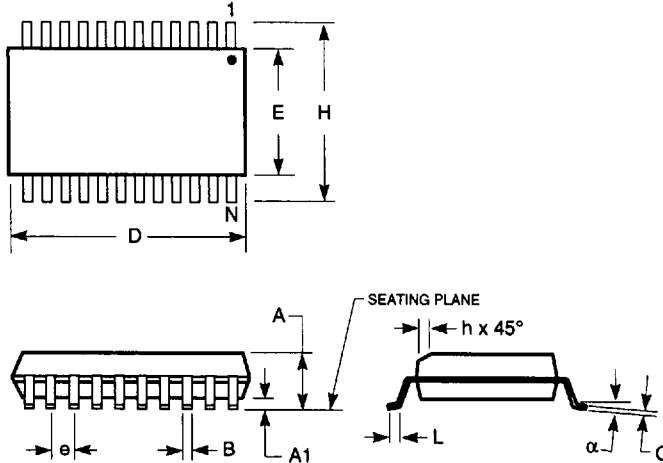
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.

JEDEC#	MS-013AA		MS-013AC		MS-013AD		MS-013AE	
DWG#	PS16A		PS20A		PS24A		PS28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.096	0.104
A1	0.005	0.011	0.005	0.011	0.005	0.011	0.005	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.402	0.412	0.500	0.510	0.602	0.612	0.701	0.711
E	0.292	0.299	0.292	0.299	0.292	0.299	0.292	0.299
e	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056
H	0.396	0.416	0.396	0.416	0.396	0.416	0.396	0.416
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
N	16		20		24		28	
$\alpha$	0°	8°	0°	8°	0°	8°	0°	8°

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QUALITY SEMICONDUCTOR, INC.

**150-MIL SOIC - Package Code S1**  
**Plastic Small Outline Gull-Wing**



JEDEC#	MS-012AB			MS-012AC		
DWG#	PS-14B			PS-16B		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008
B	0.014	0.016	0.019	0.014	0.016	0.019
C	0.0075	0.008	0.0098	0.0075	0.008	0.0098
D	0.337	0.341	0.346	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157
e	0.050 BSC			0.050 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035
N	14			16		
$\alpha$	0°	5°	8°	0°	5°	8°

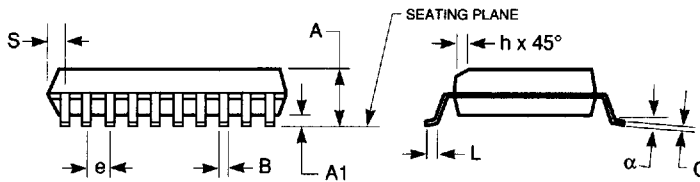
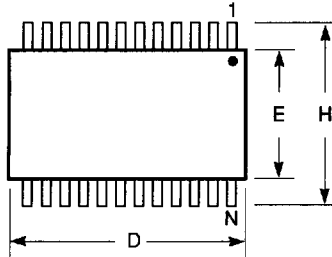
**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.

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**150-MIL QSOP - Package Code Q**

**Quarter-Size Outline Package  
Plastic Small Outline Gull-Wing**



**Notes:**

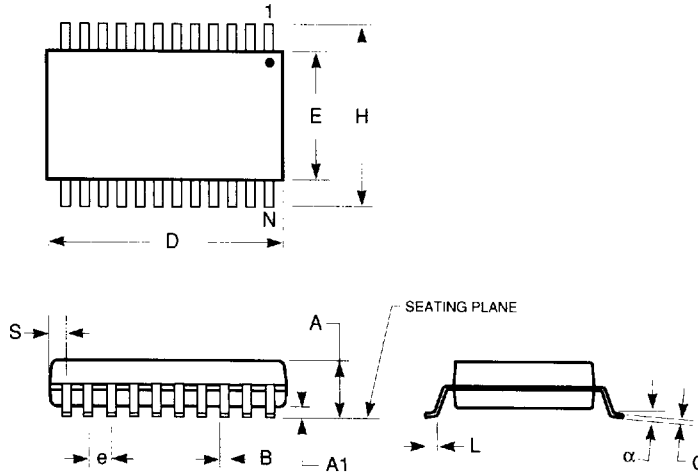
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.

JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
alpha	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035

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**150-MIL HQSOP - Package Code H**  
Hermetic Quarter-Size Outline Package  
Ceramic Small Outline Gull-Wing



JEDEC#	TBD			TBD		
DWG#	HSS-20A			HSS-24A		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.070	0.074	0.078	0.070	0.074	0.078
A1	0.008	0.012	0.016	0.008	0.012	0.016
B	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010
D	0.337	0.342	0.350	0.337	0.342	0.350
E	0.150	0.155	0.158	0.150	0.155	0.158
e	0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244
L	0.016	0.025	0.035	0.016	0.025	0.035
N	20			24		
$\alpha$	0°	5°	8°	0°	5°	8°
S	0.056	0.058	0.062	0.031	0.033	0.037

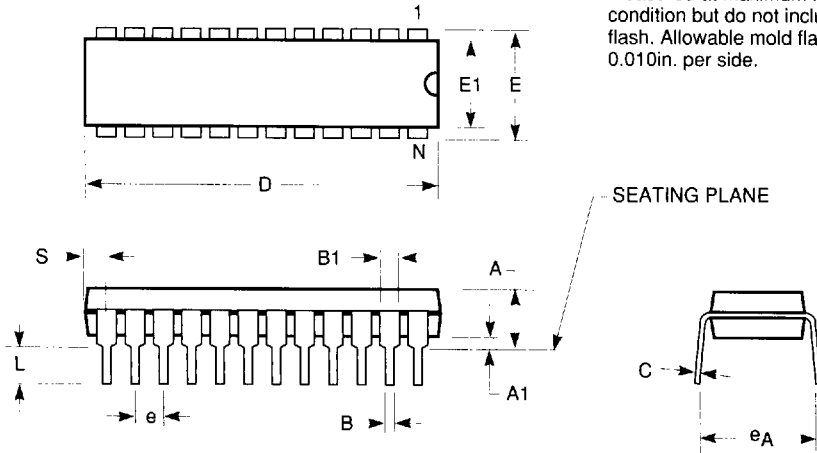
**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition.
5. Lead coplanarity is 0.004in. maximum.

**300-MIL PDIP - Package Code P**  
**Plastic Dual In-line Package**

**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E1 are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010in. per side.

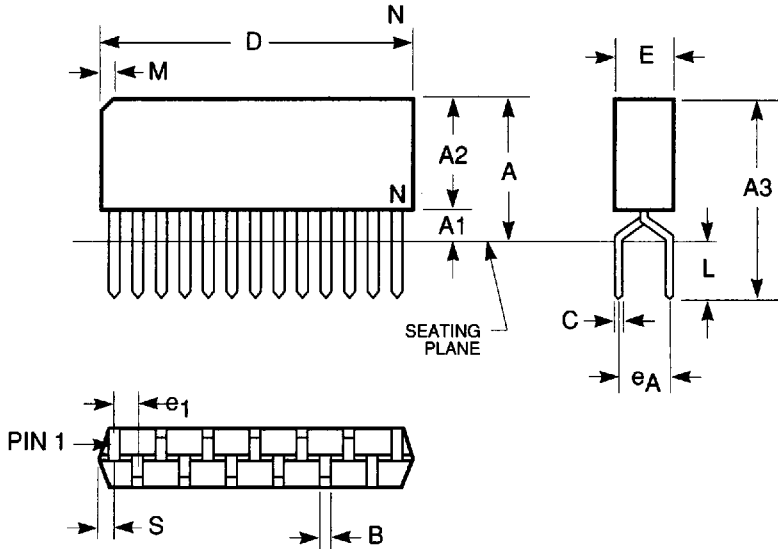


JEDEC#	MS-001AC		MS001AA		MS-001AE		N/A		MS-001AF		MO-095AH	
DWG#	PD14A		PD16A		PD20A		PT22B		PT24A		PT28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.170	0.130	0.180
A1	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
B	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020
B1	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.070	0.045	0.060
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.745	0.765	0.745	0.765	1.020	1.040	1.020	1.040	1.150	1.260	1.345	1.385
E	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
E1	0.240	0.270	0.240	0.270	0.240	0.270	0.240	0.270	0.250	0.280	0.275	0.295
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
e <sub>A</sub>	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380	0.310	0.380
L	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
S	0.070	0.080	0.020	0.035	0.060	0.070	0.010	0.020	0.025	0.080	0.020	0.040
N	14		16		20		22		24		28	

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**300-MIL ZIP - Package Code Z**  
Zig-zag In-line Packages



JEDEC#	MO-072AB		MO-072AC		MO-072AD	
DWG#	PZ20A		PZ24A		PZ28A	
Symbol	Min	Max	Min	Max	Min	Max
A	0.350	0.400	0.350	0.400	0.350	0.400
A1	0.030	0.070	0.030	0.070	0.032	0.055
A2	0.280	0.340	0.320	0.350	0.335	0.345
A3	0.450	0.550	0.450	0.550	0.460	0.550
B	0.015	0.024	0.015	0.024	0.015	0.024
C	0.008	0.012	0.008	0.012	0.008	0.012
D	1.008	1.030	1.200	1.250	1.409	1.424
E	0.100	0.120	0.100	0.120	0.110	0.120
e1	0.050 BSC		0.050 BSC		0.050 BSC	
eA	0.100 BSC		0.100 BSC		0.100 BSC	
L	0.100	0.150	0.100	0.150	0.110	0.150
M	0.035	0.085	0.035	0.085	0.035	0.085
N	20		24		28	
S	0.018	0.032	0.018	0.032	0.025	0.038

**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.010in. per side.