256Kx4 Monolithic CMOS Static RAM High Speed

The EDI84256CS is a high speed, high performance, megabit density monolithic Static RAM organized as 256Kx4 bits.

Inputs and outputs are TTL compatible and allow for direct interfacing with common system bus architecture.

A low power version, EDI84256LPS, includes a 2V Data Retention Function for battery back-up operation.

Industrial grade product is also available.

Features

256Kx4 bit CMOS Static Random Access Memory

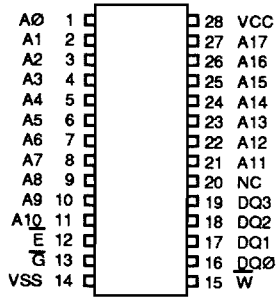
- Fast Access Times of 17, 20, 25, and 35ns
- $\overline{E}$ and $\overline{G}$ Functions for Bus Control
- 2V Data Retention Function (EDI84256LPS)
- TTL Compatible I/O
- Common Data Inputs and Outputs
- Fully Static, No Clocks

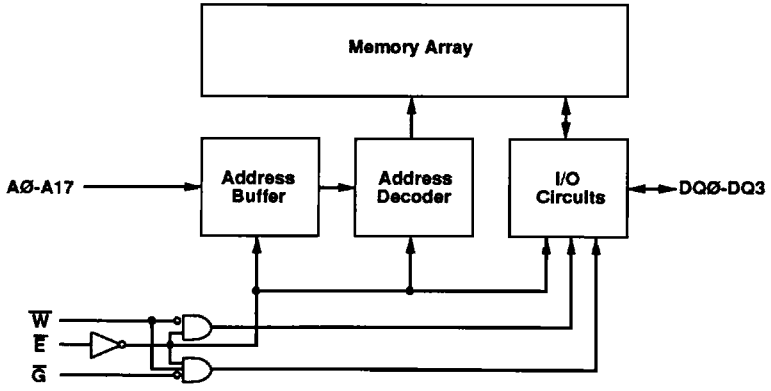
JEDEC Pinout, Thru-hole and Surface Mount Package Options

- 28 Pin Dual-in-line Packages
  Ceramic DIP, 400 mils Wide, No. 101
- 28 Lead Plastic SOJ, No. 22

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A17	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ3	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to +70°C
Industrial ..... -40°C to +85°C
Storage Temperature
Plastic ..... -55°C to +125°C
Ceramic ..... -65°C to +150°C
Power Dissipation ..... 2 Watts
Output Current ..... 40 mA
Junction Temperature, TJ ..... 175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	–	VCC+0.5	V
Input Low Voltage	VIL	-0.3	–	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 3ns
Input and Output Timing Levels 1.5V
Output Load ..... Figure 1
(note: For TEHQZ,TGHQZ and TWLQZ ..... Figure 2)

Figure 1

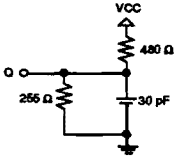
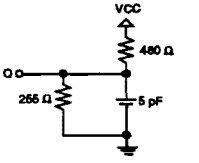


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, I/O = 0mA	17ns			245	mA
			20ns			225	mA
			25-35ns			180	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIL ≥ VIN ≥ VIH				20	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V	CS		1	5	mA
		VIN ≥ VCC-0.2V or VIN ≤ 0.2V	LPS			2	mA
Input Leakage Current	ILI	VIN = 0V to VCC		–	–	±5	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		–	–	±10	µA
Output High Voltage	VOH	IOH = -4.0mA		2.4			V
Output Low Voltage	VOL	IOL = 8.0mA				0.4	V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max		Unit
		Plastic SOJ	Ceramic DIP	
Address Lines	CI	6	12	pF
Data Lines	CD/Q	8	14	pF

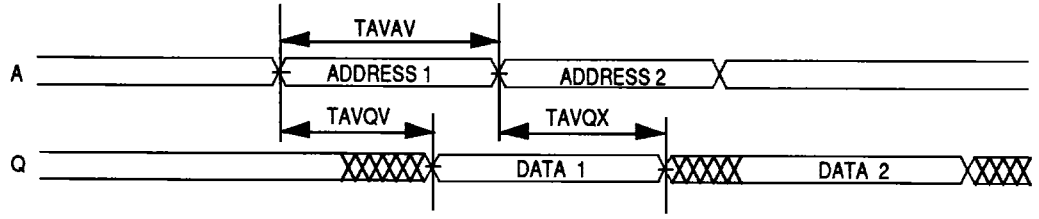
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

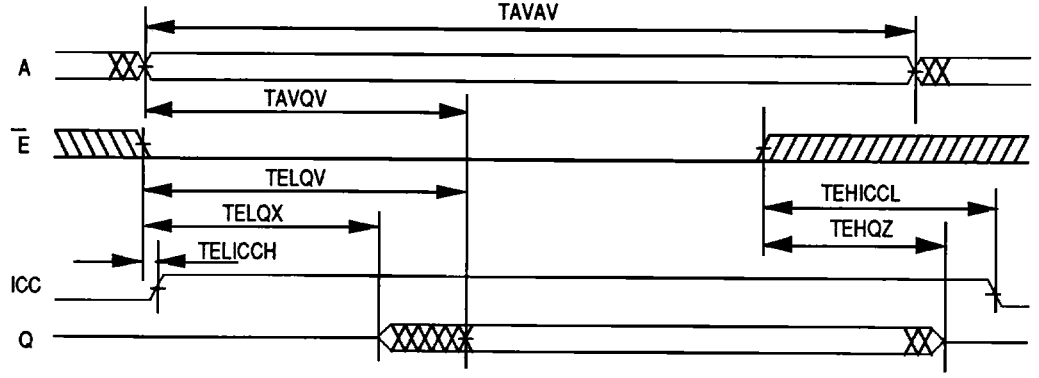
Parameter	Symbol JEDEC	Symbol Alt.		17ns Min	17ns Max	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Read Cycle Time	TAVAV	TRC		17		20		25		35		ns
Address Access Time	TAVQV	TAA			17		20		25		35	ns
Chip Enable Access Time	TELQV	TACS			17		20		25		35	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ		3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ			9		10		12		20	ns
Output Hold from Address Change	TAVQX	TOH		3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE			7		8		10		20	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ		0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ			7		8		10		20	ns
Chip Enable to Power Up	TELICCH	TPU		0		0		0		0		ns
Chip Enable to Power Down	TEHICCL	TPD			17		20		25		35	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High

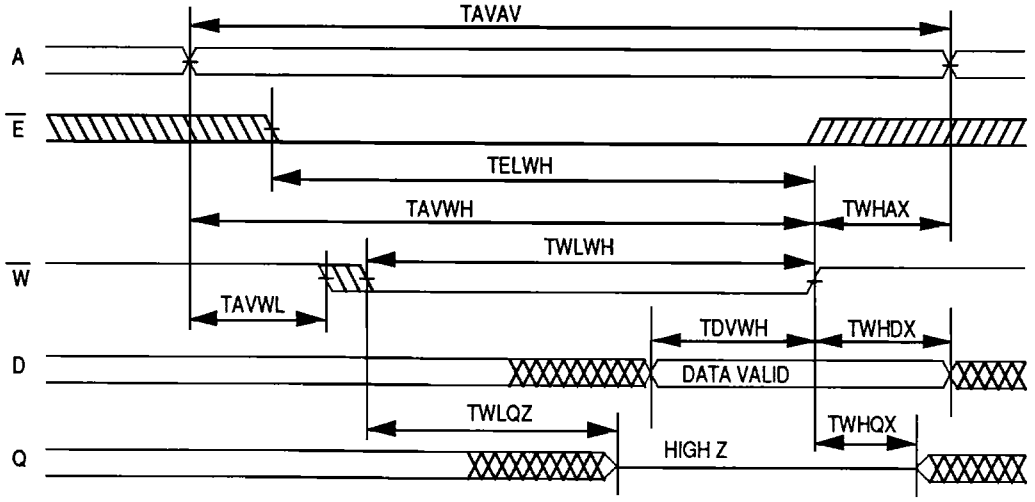


AC Characteristics
Write Cycle

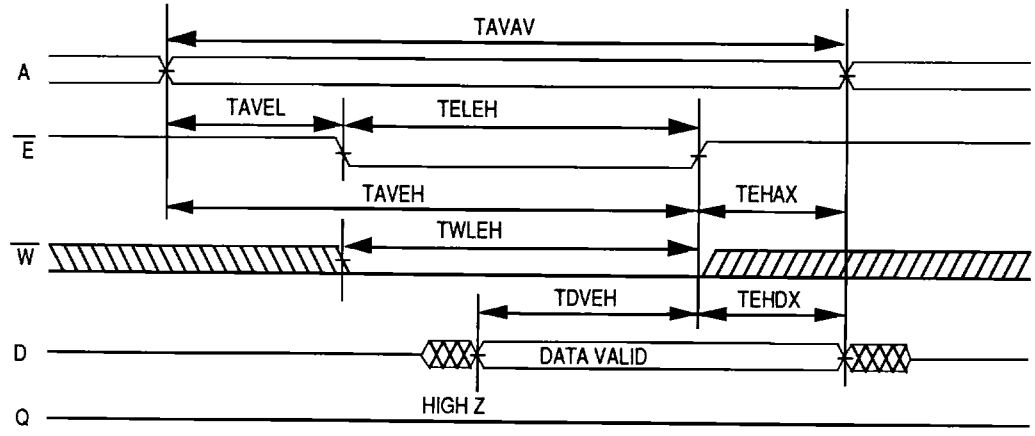
Parameter	Symbol			17ns		20ns		25ns		35ns		Units
	JEDEC	Alt.		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC		17		20		25		35		ns
Chip Enable to End of Write	TELWH	TCW		13		15		20		30		ns
	TELEH	TCW		13		15		20		30		ns
Address Setup Time	TAVWL	TAS		0		0		0		0		ns
	TAVEL	TAS		0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW		13		15		20		30		ns
	TAVEH	TAW		13		15		20		30		ns
Write Pulse Width	TWLWH	TWP		13		15		20		30		ns
	TWLEH	TWP		13		15		20		30		ns
Write Recovery Time	TWHAX	TWR		0		0		0		0		ns
	TEHAX	TWR		0		0		0		0		ns
Data Hold Time	TWHDX	TDH		0		0		0		0		ns
	TEHDX	TDH		0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ		0	6	0	8	0	10	0	15	ns
Data to Write Time	TDVWH	TDW		7		12		15		20		ns
	TDVEH	TDW		7		12		15		20		ns
Output Active from End of Write (1)	TWHQX	TWLZ		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



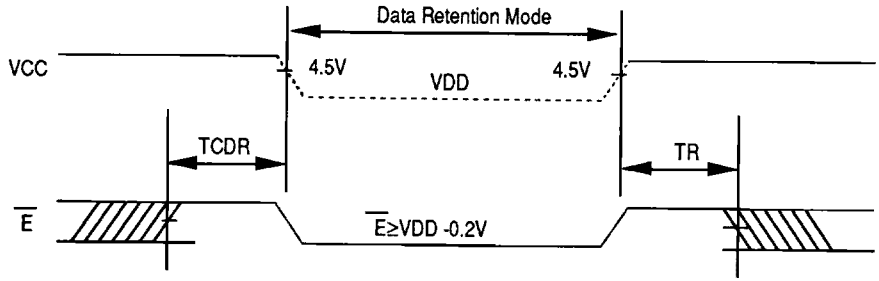
Data Retention Characteristics

Low Power (LPS) Version Only

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E} \geq$ VDD -0.2V	--		500	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥ VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤ 0.2V	TAVAV*		--	ns

*Read Cycle Time

Data Retention
$\overline{E}$ Controlled



Ordering Information

Commercial* Standard Power	Speed ns	Leads	Package Style	No.
EDI84256CS17MC	17	28	SOJ	22
EDI84256CS20MC	20	28	SOJ	22
EDI84256CS25MC	25	28	SOJ	22
EDI84256CS35MC	35	28	SOJ	22
EDI84256CS17TC	17	.28	0.4 DIP	101
EDI84256CS20TC	20	28	0.4 DIP	101
EDI84256CS25TC	25	28	0.4 DIP	101
EDI84256CS35TC	35	28	0.4 DIP	101

Low Power with Data Retention	Speed ns	Leads	Package Style	No.
EDI84256LPS17MC	17	28	SOJ	22
EDI84256LPS20MC	20	28	SOJ	22
EDI84256LPS25MC	25	28	SOJ	22
EDI84256LPS35MC	35	28	SOJ	22
EDI84256LPS17TC	17	28	0.4 DIP	101
EDI84256LPS20TC	20	28	0.4 DIP	101
EDI84256LPS25TC	25	28	0.4 DIP	101
EDI84256LPS35TC	35	28	0.4 DIP	101

* For Industrial grade product I replaces C in part number, e.g. EDI84256CS20MC becomes EDI84256CS20MI.