Differential Clock Generator

Features

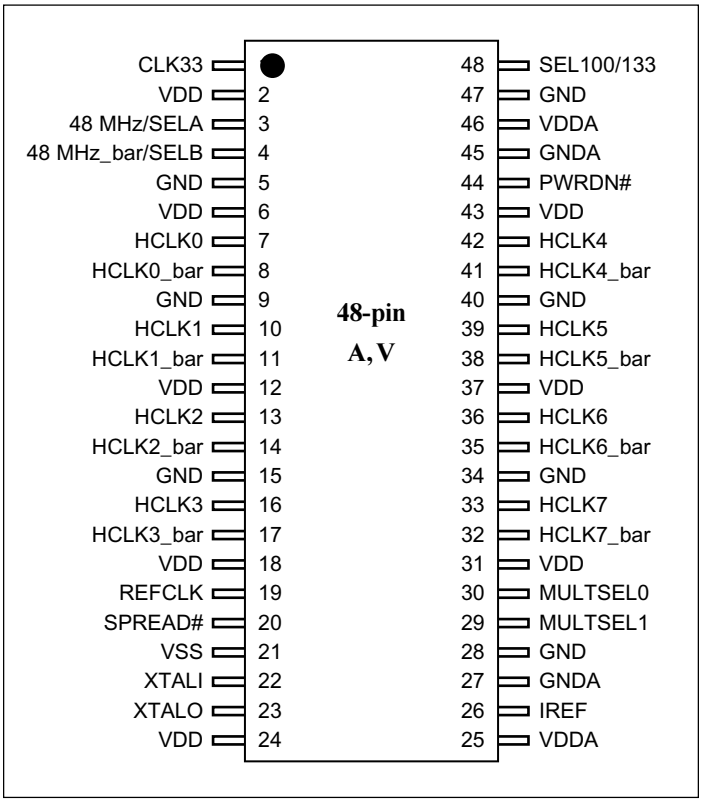
- Eight copies of Differential CPU Clock Output at 100 MHz
- One copy of CLK33
- One copy of 14.31818 MHz Reference Clock
- One copy of Differential 48 MHz Clock
- External Resistor for Current Reference
- Selection Logic for Differential Swing Control, Test Mode, HI-Z, Power-Down, Spread Spectrum
- Available Packaging:
  – 48-pin TSSOP (A package)
  – 48-pin SSOP (V package)

Description

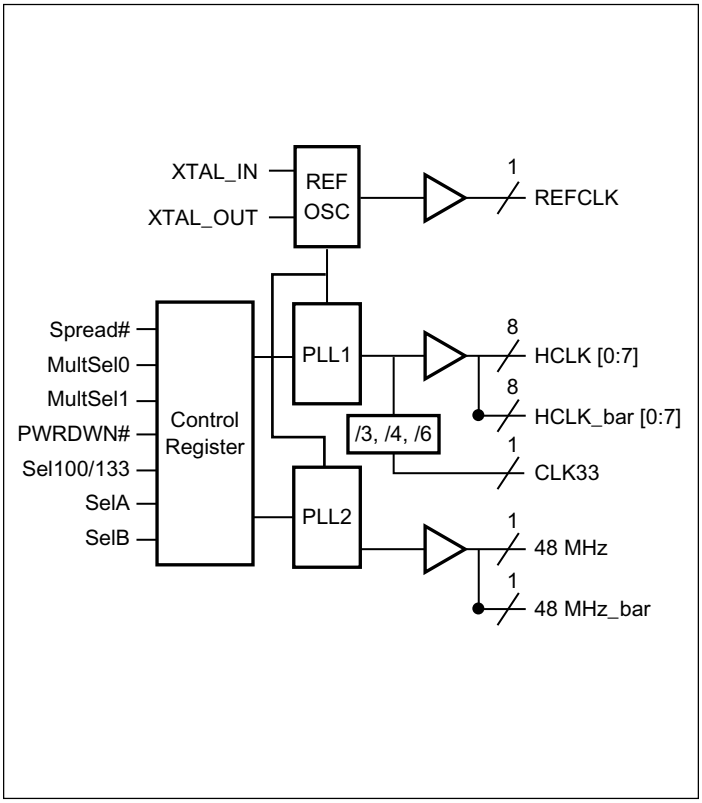
Pericom's PI6C210 is produced using the Company's advanced submicron technology.

The clocks for the CPU are provided by HCLK and HCLK_bar [0:7] outputs. These eight differential CPU clock pairs run at 100 MHz. The V_{OH} swing amplitude is configured by the MultSel0 and MultSel1 pins.

Pin Configuration



Block Diagram



Pin Description

Pin Name	Pin Type	Pin Description
HCLK, HCLK_bar	O	Host Clock Outputs. these eight Differential CPU clock pairs run at 100 MHz. The V_{OH} swing amplitude is configured by the Multsel0, Multsel1 pins.
CLK33	O	33 MHz Reference Clock. Host clock divided by 3, 4, or 6.
48 MHz, 48 MHz_bar	I/O	48 MHz Differential Clocks.
REFCLK	O	14.318 MHz Reference Clock Output. 3.3V copies of the 14.318 MHz reference clock.
XTALI	I	Crystal connection or External Reference Frequency Input. Connect to either a 14.318 MHz crystal or an external reference signal.
XTALO	O	Crystal Connection. An output connection for an external 14.318 MHz crystal. If using an external reference, this pin must be left unconnected.
SPREAD#	I	Spread Spectrum Enable. 3.3V LVTTL compatible input that enables spread spectrum mode when held LOW.
PWRDN#	I	Power Down Input. 3.3V LVTTL compatible asynchronous input that requests the device to enter power-down mode when it is held low.
SELA, SELB	I/O	Logic Select Pins. Select the mode of operation
MultSel0, MultSel1	I	Select Pins for V_{OH} swing amplitude of HCLK and HCLK_bar
V_{CC}	P	Power Supply
IREF	I	Current Reference. This pin establishes the reference current for the host clock pairs.

Group Skew and Jitter Specification

Output Group	Pin-to-pin Skew, Pair-to-pair Skew	Cycle-cycle Jitter	Duty Cycle	Type	Measured @
Host Clock	100ps	150ps	45/55	Differential	Crossing
CLK33	–	500ps	45/55	Single ended 3.3V	1.5V
REFCLK	–	1000ps	45/55	Single ended 3.3V	1.5V
48 MHz	–	350ps	45/55	Single ended 3.3V	1.5V

Group Offset Specification

Group	Offset	Comments
Host to CLK33	No requirement	
Host to REF	No requirement	

Select Signal Configurations

SEL100/133	SELA	SELB	HCLK	CLK33	48 MHz, 48 MHz_bar	REF	Notes
0	0	0	100 MHz	33 MHz	48 MHz	14.318	Normal Operation
0	0	1	100 MHz	33 MHz	Disable	14.318	Test Mode (recommended)
0	1	0	100 MHz	Disable	Disable	14.318	Test Mode (optional)
0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z All Outputs
1	0	0	133 MHz	33 MHz	48 MHz	14.318	Optional
1	0	1	133 MHz	33 MHz	Disable	14.318	Optional
1	1	0	200 MHz	33 MHz	48 MHz	14.318	Optional
1	1	1	TCLK/2	TCLK/8	TCLK/2	TCLK	RESERVED

Absolute Maximum DC Power Supply

Symbol	Parameter	Min.	Max.	Units	Notes
V_{DD3}	3.3V Core Supply Voltage	–0.5	4.6	V	
V_{DDQ3}	3.3V I/O Supply Voltage	–0.5	4.6	V	
T_S	Storage Temperature	–65	150	°C	2

Note:
Maximum V_{IH} not to exceed V_{DD3} +0.7V

Absolute Maximum DC I/O

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH3}	3.3V Input High Voltage	–0.5	4.6	V	1
V_{IL3}	3.3V Input Low Voltage	–0.5		V	
ESD prot.	Input ESD Protection	2000		V	2

Notes:
1. Maximum V_{IH} is not to exceed maximum 0.7V above V_{DD}
2. Human body model

DC Operating Requirements

Symbol	Parameter	Condition	Min.	Max.	Units	Notes
V_{DD3}	3.3V Supply Voltage	3.3V ±5%	3.135	3.465	V	4
V_{IH3}	3.3V Input High Voltage	V_{DD3}	2.0	V_{DD} +0.3	V	7
V_{IL3}	3.3V Input Low Voltage		V_{SS} –0.3	0.8	V	7
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{DDQ3}$	–5	+5	µA	3, 7
V_{OH3}	3.3V Output High Voltage	I_{OH} = –1mA	2.4		V	1
V_{OL3}	3.3V Output Low Voltage	I_{OL} = 1mA		0.4	V	1
V_{POH}	PCI Bus Output High Voltage	I_{OH} = –1mA	2.4		V	1
V_{POL}	PCI Bus Output Low Voltage	I_{OL} = 1mA		0.55	V	1, 5
C_{IN}	Input Pin Capacitance			5	pF	2
C_{XTAL}	Xtal Pin Capacitance		13.5	22.5	pF	6
T_A	Ambient Temperature	No Airflow	0	70	°C	

Notes:
1. Signal edge is required to be monotonic when transitioning through this region.
2. This is a recommendation, not an absolute requirement.
3. Input Leakage Current does not include inputs with Pull-up or Pull-down resistors. Inputs with resistors should state current requirements.
4. No power sequencing is implied or allowed to be required in the system.
5. Conforms to 5V PCI signaling specification.
6. As seen by the crystal. Device is intended to be used with a 17-20pF AT crystal.
7. All inputs referenced to 3.3V power supply.

Maximum Current Draw During PWRDWN#

Parameter	Min.	Max.	Units	Note
Current from 3.3V supply	N/A	120	mA	Configured w/475 Ohm current reference resistor

Maximum Current Draw

Parameter	Min.	Max.	Units	Note
Current from 3.3V supply	N/A	400	mA	Max. power supply (3.465V), all active, 475 Ohm current reference resistor, Host = 133 MHz

Buffer Types

Buffer Name	V_{CC} Range (V)	Impedance (Ohms)	Buffer Type
48 MHz, REF	3.135-3.465	20-60	Type 3
CLK33	3.135-3.465	12-55	Type 5
Host/Host_bar			Type X1

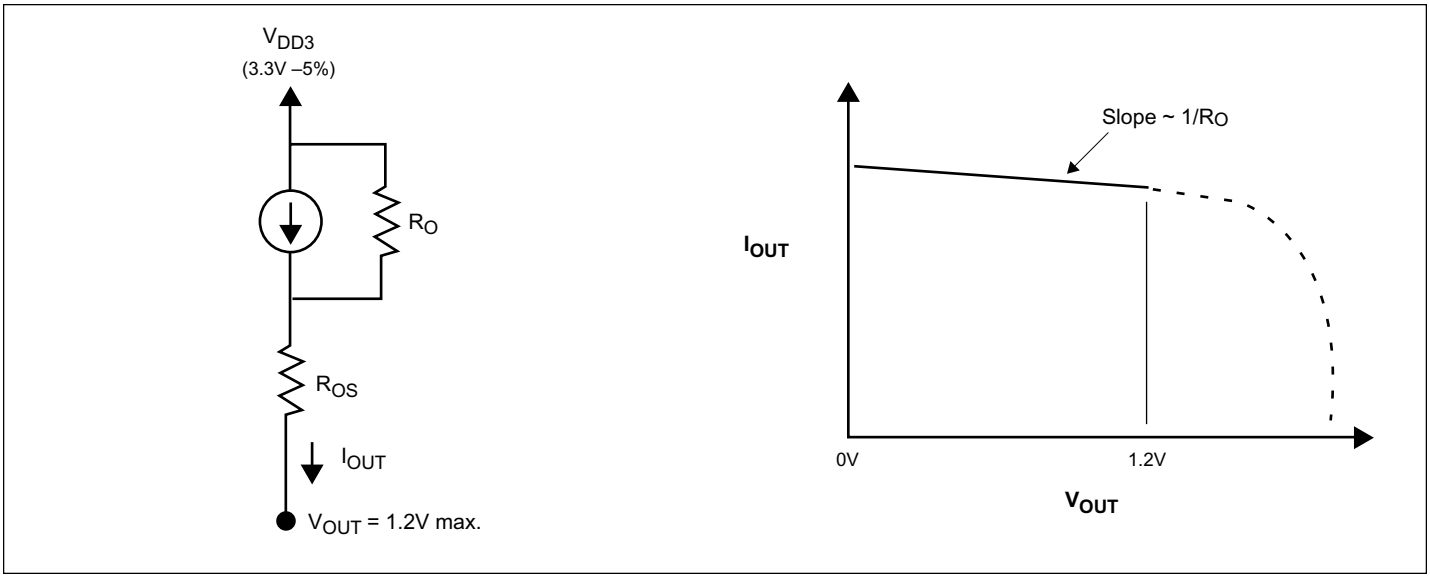
48 MHz, REF Operating Requirements

Symbol	Parameter	Condition	Min.	Max.	Units
I_{OHMIN}	Pull-up Current	V_{OUT} = 1.0V	–29		mA
I_{OHMAX}	Pull-up Current	V_{OUT} = 3.135V		–23	mA
I_{OLMIN}	Pull-down Current	V_{OUT} = 1.95V	29		mA
I_{OLMAX}	Pull-down Current	V_{OUT} = 0.4V		27	mA
t_{RH}	3.3V Type 3 Output Rise Edge Rate	3.3V ±5% @ 0.4V –2.4V	0.5	2.0	V/nS
t_{FH}	3.3V Type 3 Output Rise Fall Rate	3.3V ±5% @ 2.4V –0.4V	0.5	2.0	V/nS

CLK33 Operating Requirements

Symbol	Parameter	Condition	Min.	Max.	Units
I_{OHMIN}	Pull-up Current	V_{OUT} = 1.0V	–33		mA
I_{OHMAX}	Pull-up Current	V_{OUT} = 3.135V		–33	mA
I_{OLMIN}	Pull-down Current	V_{OUT} = 1.95V	30		mA
I_{OLMAX}	Pull-down Current	V_{OUT} = 0.4V		38	mA
t_{RH}	3.3V Type 4 Output Rise Edge Rate	3.3V ±5% @ 0.4V –2.4V	1/1	4/1	V/ns
t_{FH}	3.3V Type 4 Output Rise Fall Rate	3.3V ±5% @ 2.4V –0.4V	1/1	4/1	V/ns

Current-Mode Output Buffer Characteristics HCLK, HCLK_bar [0:7]



Host Clock (HCSL) Buffer Characteristics

	Minimum	Maximum
R_O	3000 Ohms (recommended)	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	1.2V

Note: I_{OUT} is selectable depending on implementation. The parameters above, however, apply to all configurations. V_{OUT} is the voltage at the pin of the device.

Current Accuracy

	Conditions	Load	Min.	Max.
I_{OUT}	V_{DD} = nominal (3.30V)	Nominal test load for given configuration	–7% $I_{NOMINAL}$	+7% $I_{NOMINAL}$
I_{OUT}	V_{DD} = 3.30 ±5%	Nominal test load for given configuration	–12% $I_{NOMINAL}$	+12% $I_{NOMINAL}$

Note: $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

AC Timing Requirements

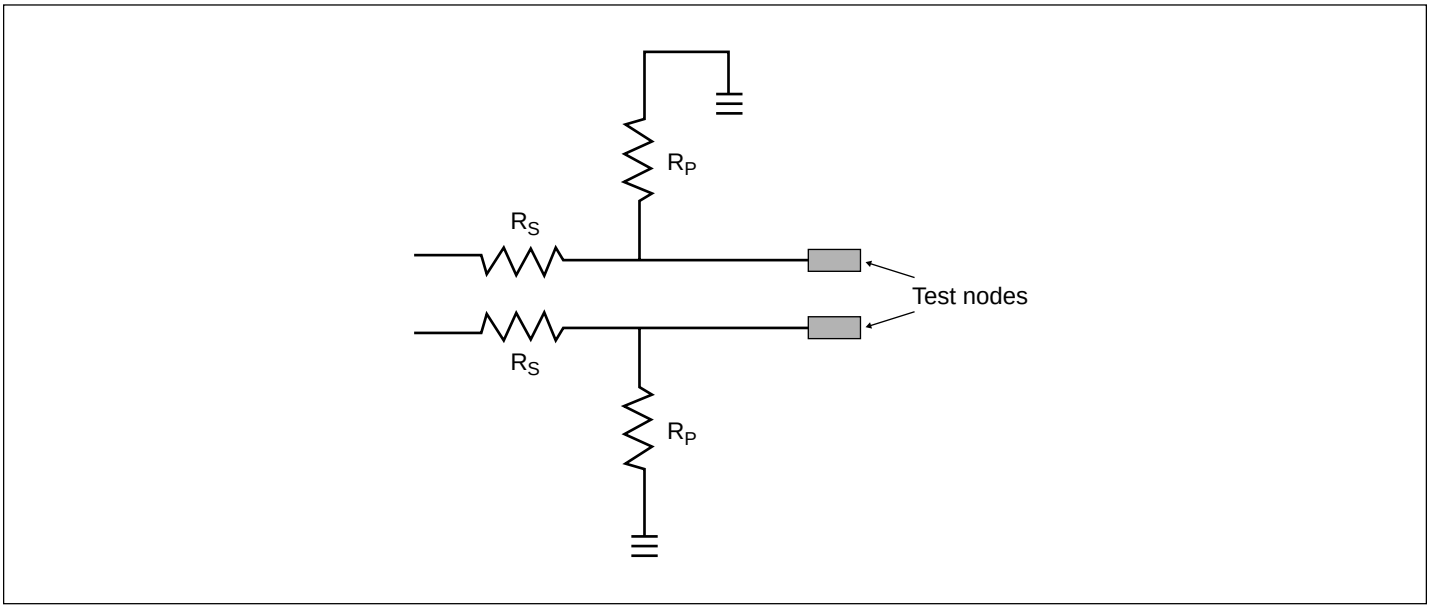
Symbol	Parameter	133 MHz Host		100 MHz Host		Units	Notes
		Min.	Max.	Min.	Max.		
TPeriod	Host CLK period - average	7.5	7.65	10.0	10.2	nS	11,14
AbsMinPeriod	Absolute minimum Host CLK Period	7.35	N/A	9.85	N/A	nS	11,14
I_{OH} (V_{OH})	Output Current (Voltage at given load)	12.9 (0.65)	14.9 (0.74)	12.9 (0.65)	14.9 (0.74)	mA (V)	11, 13,17
V_{OL}		V_{SS} = 0.0	0.05	V_{SS} = 0.0	0.05	V	11
Vcrossover		45% V_{OH}	55% V_{OH}	45% V_{OH}	55% V_{OH}	V	11,14
TRISE	Host/CPU CLK Rise Time	175	700	175	700	pS	11,15
TFALL	Host/CPU CLK Fall Time	175	700	175	700	pS	11,15
Rise/Fall Matching	Rise Time and Fall Time Matching		20%		20%		11,16
Overshoot			V_{OH} +0.2V		V_{OH} +0.2V		11,16
Undershoot		–0.2V		–0.2V			11
Duty Cycle		45%	55%	45%	55%		11,14
TPeriod	CLK33 period	30.0	N/A	30.0	N/A	nS	2,3,9
THIGH	CLK33 high time	12.0	N/A	12.0	N/A	nS	5,10
TLOW	CLK33 low time	12.0	N/A	12.0	N/A	nS	6,10
TRISE	CLK33 rise time	0.5	2.0	0.5	2.0	nS	8
TFALL	CLK33 fall time	0.5	2.0	0.5	2.0	nS	8
t_{PZL}, t_{PZH}	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	nS	
t_{PLZ}, t_{PZH}	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	nS	
tstable	All clock stabilization from power-up		3		3	mS	7

Notes:
1. Output drivers must have monotonic rise/fall times through the specified V_{OL}/V_{OH} levels.
2. Period, Jitter, Offset, and Skew measured on rising edge @1.25V for 2.5V clocks and 1.5V for 3.3V clocks.
3. The PCI clock is the Host clock divided by four at Host = 133 MHz. PCI clock is the Host clock divided by three at Host = 100 MHz.
4. PCI clock id the Host clock divided by six at Host = 200 MHz.
5. THIGH is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.
6. TLOW is measured at 0.4V for all outputs.
7. The time specified is measured from when V_{DDQ} achieves its nominal operating level (typical condition V_{DDQ}=3.3V) till the frequency output is stable and operating within specification.
8. TRISE and TFALL are measured as a transition through the threshold region V_{OL}=0.4V, and V_{OH}=2.4V (1mA) JEDEC Specification
9. The average period over any 1uS period of time must be greater than the minimum specified period.
10. Calculated at minimum edge-rate (1V/nS) to guarantee 45/55% duty-cycle. Pulsewidth is required to be wider at faster edge-rate to ensure duty-cycle specification is met.
11. Test load is R_S=33.2 Ohms, R_P=49.9.
12. Must be guaranteed in realistic system environment.
13. Configured for I_{OH}=6* I_{REF}.
14. Measured at crossing points.
15. Measured at 20% to 80%.
16. Determined as a fraction of 2* (Trp–Trn) / (Trp+Trn) where Trp is a rising edge and Trn is an intersecting falling edge.
17. These Min. and Max. voltages and currents assume a power supply of 3.30V. For system considerations, the voltages will need to be degraded to account for the ±5% variation in the 3.3V supply.

Lumped Capacitive Test Loads for Single ended Outputs

Clock	Min. Load	Max. Load	Units	Notes
3V66	10	30	pF	1 device load, possible 2 loads
48 MHz Clock	10	20	pF	1 device load
REF	10	20	pF	1 device load

Notes:
1. Maximum rise/fall times are to be guaranteed at a maximum specified load for each type of output buffer.
2. Minimum rise/fall times are to be guaranteed at a minimum specified load for each type of output buffer.
3. Rise/fall times are specified with pure capacitive load as shown. testing may be done with an additional 500 ohm resistor in parallel if properly correlated with the capacitie load.



Lumped Test Load Configurations for the Differential Host Clock Outputs

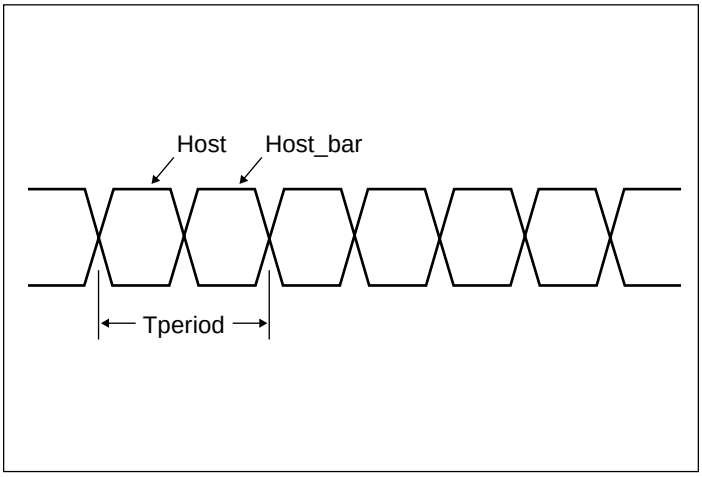
Minimum and Maximum Lumped Resistive Test Loads

Clock	Min. Load	Max. Load	Units	Notes
Host Clocks	20	105	Ohms	

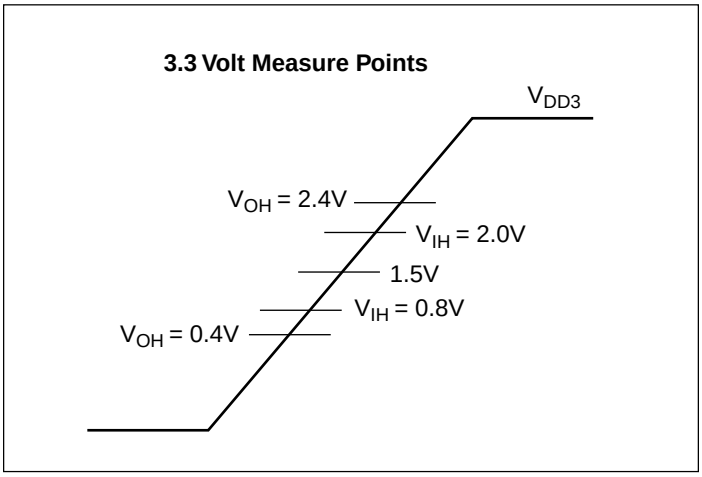
Resistive Lumped Test Loads for Differential Host Clock

Clock	R_S	R_P	Units	Notes
Host Clocks 60 ohm configurations	33.2 1%	61.9 1%	Ohms	2, 3, 5
Host Clocks 50 ohm configurations	33.2 1%	49.9 1%	Ohms	1, 2, 3, 5
Host Clocks Double terminated Configuration	0	24.9 1%	Ohms	4

Notes:
1. Expected test load configuration unless otherwise noted. This is a 50 ohm environment test load. This assumes device is configured for 50 ohm environment.
2. Test load for 60 ohm environment. This assumes device is configured for a 60 ohm environment.
3. Suppliers must correlate parameters measured in 50 ohm environment to a 60 ohm environment with the appropriate configurations of the device for each load.
4. Test load for dual terminated (ie both source and load) 50 ohm environment.
5. For configurations of the device intended to create output current greater than 14mA these test loads may not be appropriate. For such configurations, a value of $R_S = 0$ should be used.



Host Waveforms



Component vs. System Measure Points for Single Ended Clocks

PWRDWN# Mode

PWRDWN#	Host/Host_bar	CLK33	48 MHz	14.318, REF
Asserted = 0 = low	Host = 2*Iref Host_bar = undriven	Low	Low	Low (if applicable)

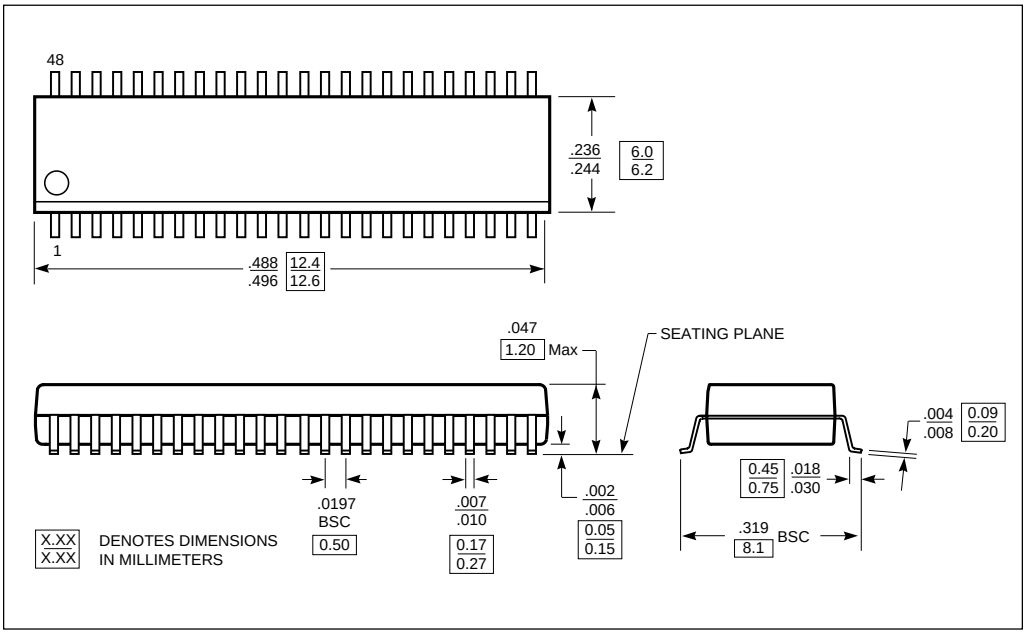
Notes:
1. When PWRDWN# is asserted, a voltage must be held across the differential outputs.
2. There are no specific timing requirements for entering or exiting PWRDWN# mode.

Host Swing Select Functions

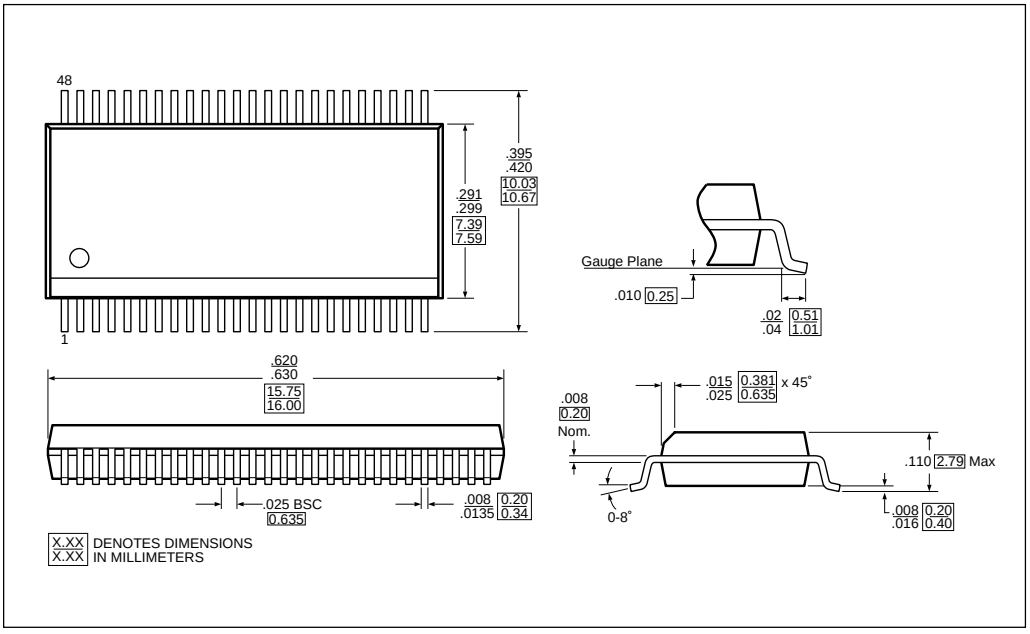
MultSel0	MultSel1	Board target Trace/Term Z	Reference R, Iref = $V_{DD/3(3*Rr)}$	Output Current	V_{OH} @ Z, Iref = 2.32mA
0	**0**	**60 ohms**	**Rr = 475 1%, Iref = 2.32mA**	**I_{OH} = 5*Iref**	**0.71V @ 60**
0	0	50 ohms	Rr = 475 1%, Iref = 2.32mA	I_{OH} = 5*Iref	0.59V @ 50
0	1	60 ohms	Rr = 475 1%, Iref = 2.32mA	I_{OH} = 6*Iref	0.85V @ 60
0	**1**	**50 ohms**	**Rr = 475 1%, Iref = 2.32mA**	**I_{OH} = 6*Iref**	**0.71V @ 50**
1	0	60 ohms	Rr = 475 1%, Iref = 2.32mA	I_{OH} = 4*Iref	0.56V @ 60
1	0	50 ohms	Rr = 475 1%, Iref = 2.32mA	I_{OH} = 4*Iref	0.47V @ 50
1	1	60 ohms	Rr = 475 1%, Iref = 2.32mA	I_{OH} = 7*Iref	0.99V @ 60
1	1	50 ohms	Rr = 475 1%, Iref = 2.32mA	I_{OH} = 7*Iref	0.82V @ 50
0	0	30 (DC equiv)	Rr = 221 1%, Iref = 5mA	I_{OH} = 5*Iref	0.75V @ 30
0	0	25 (DC equiv)	Rr = 221 1%, Iref = 5mA	I_{OH} = 5*Iref	0.62V @ 20
0	1	30 (DC equiv)	Rr = 221 1%, Iref = 5mA	I_{OH} = 6*Iref	0.90V @ 30
0	1	25 (DC equiv)	Rr = 221 1%, Iref = 5mA	I_{OH} = 6*Iref	0.75V @ 20
1	0	30 (DC equiv)	Rr = 221 1%, Iref = 5mA	I_{OH} = 4*Iref	0.60V @ 30
1	0	25 (DC equiv)	Rr = 221 1%, Iref = 5mA	I_{OH} = 4*Iref	0.5V @ 20
1	1	30 (DC equiv)	Rr = 221 1%, Iref = 5mA	I_{OH} = 7*Iref	1.05V @ 30
1	1	25 (DC equiv)	Rr = 221 1%, Iref = 5mA	I_{OH} = 7*Iref	0.84V @ 20

Notes:
The entries in boldface are the primary system configurations of interest. The outputs should be optimized for these configurations.

48-pin TSSOP Packaging Mechanical (A)



48-pin SSOP Packaging Mechanical (V)



Ordering Information

P/N	Description
PI6C210A	48-pin TSSOP
PI6C210V	48-pin SSOP