NEC

NPN SILICON HIGH SPEED SWITCHING TRANSISTOR

NE327 SERIES

FEATURES

- **ULTRA-HIGH SWITCHING SPEED :** t_{ON} 0.7 ns TYP, t_{OFF} 0.5 ns TYP
- **HIGH f_T:** 3 GHz TYP
- **HIGH MAG:** 13 dB at 1 GHz
- **LOW NOISE :** 1 dB at 70 MHz
- **HIGH RELIABILITY GOLD METALLIZATION**

DESCRIPTION

The NE327 series of NPN silicon transistors is designed for use in ultrahigh speed current mode switching applications and for use in microwave amplifiers up to 1 GHz. Transistors in this series are available in chip form and in several reliable ceramic-metal stripline packages, including a dual-chip package (NE32740). The NE32740 is available in two lead configurations which offer the engineer a large degree of design flexibility. Reliability is assured by NEC's stringent production controls and platinum, titanium, and gold metallization system.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER EIAJ[1] REGISTERED NUMBER PACKAGE OUTLINE			NE32700 00 (CHIP)			NE32708 08			NE32740A/B 2SC1924 2SC1925 40A/B		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
f_T	Gain Bandwidth Product at V_{CE} = 5V, I_C = 15 mA	GHz	2.5	3			2.5	3		2.5	3
NF_{OPT}	Optimum Noise Figure[2] at V_{CE} = 5V, I_C = 3 mA, f = 70 MHz f = 0.5 GHz f = 1 GHz	 dB dB dB		 1 1.8 3.4			 1 1.8 3.4	 4.5			
MAG	Maximum Available Gain[3] at V_{CE} = 5 V, I_C = 15 mA, f = 1 GHz	 dB		 13		 10	 13				
$\|S_{21E}\|^2$	Insertion Power Gain at V_{CE} = 5 V, I_C = 15 mA, f = 0.5 GHz f = 1 GHz f = 2 GHz	 dB dB dB				 8	 15 10 4				
t_{ON}	Switching Time[7] at V_{CE} = 5 V, I_E = 30 mA	ns		0.7			0.7			0.7	
t_{OFF}	Switching Time[7] at V_{CE} = 5 V, I_E = 30 mA	ns		0.5			0.5			0.5	
h_{FE}	Forward Current Gain[3] Ratio at V_{CE} = 5 V, I_C = 10 mA		30	100	300	30	100	300	30	100	300
h_{FE1} h_{FE2}	Forward Current Gain Ratio[4] at V_{CE} = 5 V, I_C = 10 mA					0.8		1			
I_{CBO}	Collector Cutoff Current at V_{CB} = 10V, I_E = 0	μA			0.5			0.5			0.1
I_{EBO}	Emitter Cutoff Current at V_{EB} = 2 V, I_C = 0	μA			0.5			0.5			0.1
C_{CB}	Collector to Base Capacitance[5] at V_{CB} = 5V, I_C = 0, f = 1 MHz	pF		0.9	1.5		0.9	1.5		1.1	1.5
C_{EB}	Emitter to Base Capacitance at V_{EB} = 0.5 V, I_C = 0, f = 1 MHz	pF		0.9	1.5		0.9	1.5		1.1	1.5
ΔV_{BE}	Base Emitter Voltage Difference at V_{CE} = 5V, I_C = 10 mA	mV									10
$R_{E(HIE)}$	Input Resistance at V_{CE} = 5 V, I_C = 15 mA, f = 1 GHz	Ω		30			30	50			
$R_{TH(J-C)}$	Thermal Resistance (Junction to Case)	°C/W			50			70			50
P_T	Total Power Dissipation	mW			250			250			300[6]

Notes:
1. Electronic Industrial Association of Japan.
2. Input and output are tuned for optimum noise figure.
3. Pulse Width ≤ μs, Duty Cycle ≤ 2%/pulsed.
4. h_{FE2} is the smallest of the two.
5. C_{CB} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter terminal shall be connected to the guard terminal.
6. P_T is limited to 200 mW/chip in the dual chip configuration (NE32740).
7. See Test Circuit.

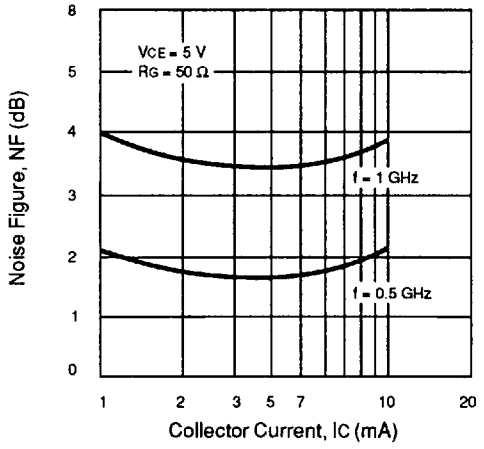
ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CBO}	Collector to Base Voltage	V	20
V_{CEO}	Collector to Emitter Voltage	V	12
V_{EBO}	Emitter to Base Voltage	V	3
I_C	Collector Current	mA	50
T_J	Junction Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to +200

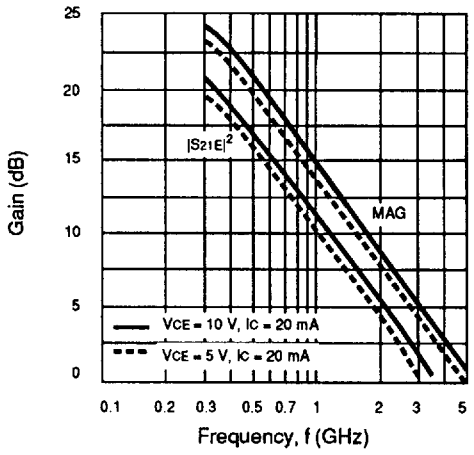
Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

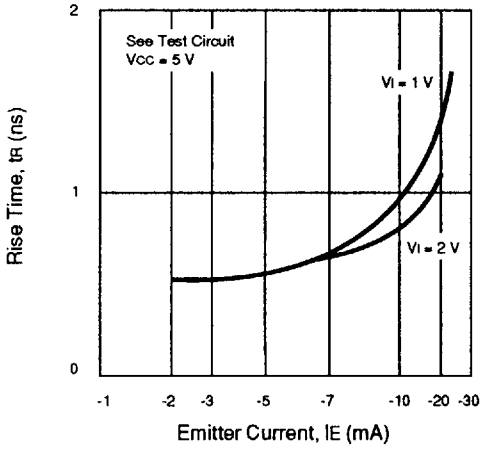
NOISE FIGURE vs. COLLECTOR CURRENT



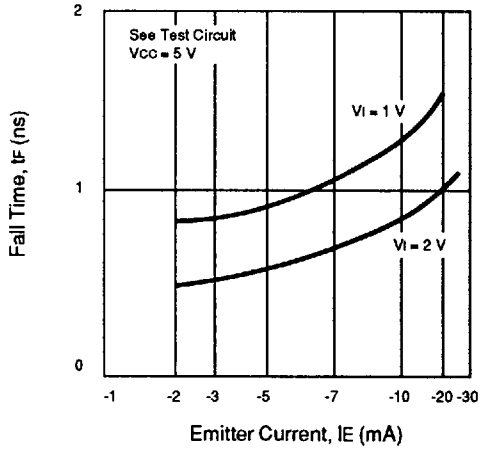
NE32708 GAIN vs. FREQUENCY



RISE TIME vs. EMITTER CURRENT

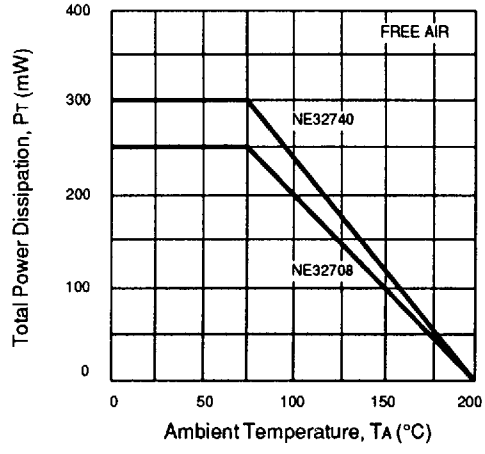


FALL TIME vs. EMITTER CURRENT

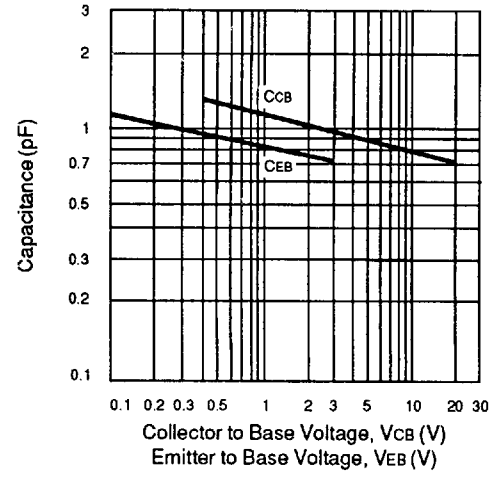


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

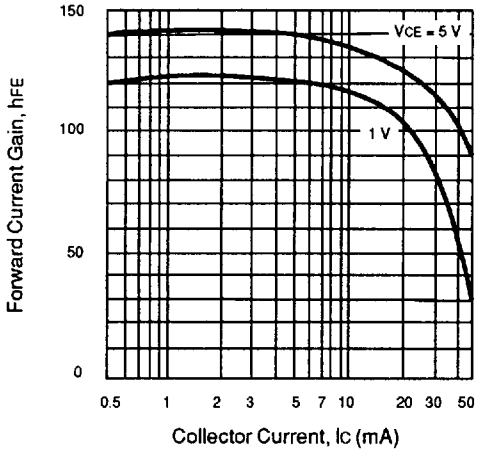
DC POWER DERATING CURVE



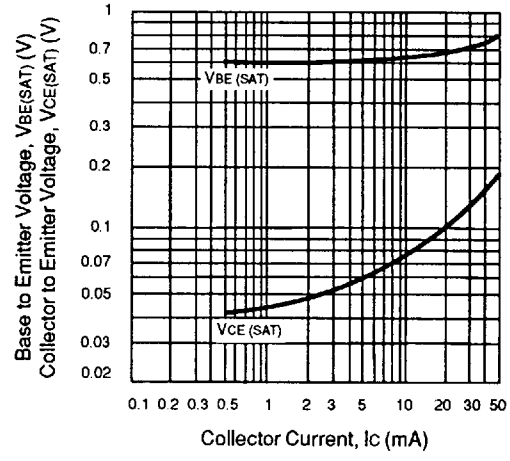
DEVICE CAPACITANCE



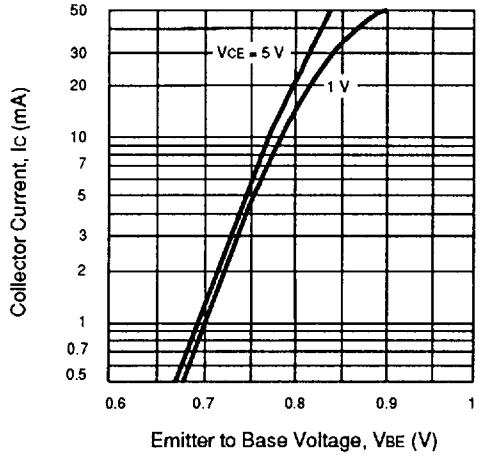
FORWARD CURRENT GAIN vs. COLLECTOR CURRENT



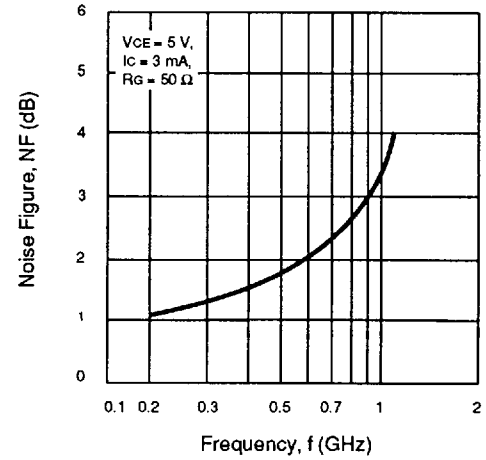
SATURATION VOLTAGE vs. COLLECTOR CURRENT



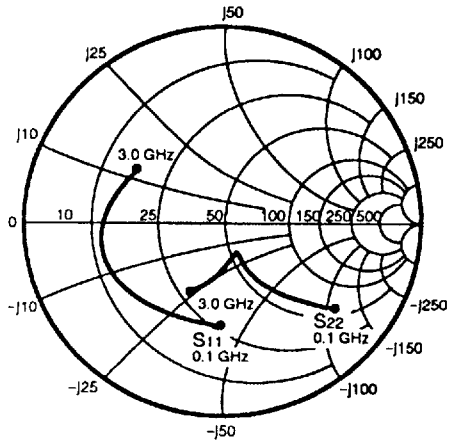
COLLECTOR CURRENT vs. EMITTER TO BASE VOLTAGE FOR TWO VALUES OF VCE

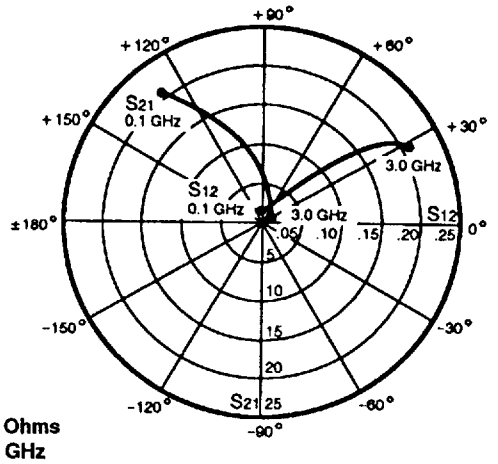


NOISE FIGURE vs. FREQUENCY



TYPICAL COMMON EMITTER SCATTERING PARAMETERS (T_A = 25°C)





Coordinates in Ohms
Frequency in GHz
(V_{CE} = 5 V, I_C = 15 mA)

NE32708

V_{CE} = 5 V, I_C = 3 mA

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}		K	MAG[1]
(MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG		
100	.80	-35	8.45	148	.02	75	.93	-17	0.16	26.3
500	.60	-123	4.19	99	.12	37	.49	-50	0.55	15.4
1000	.54	-154	2.34	75	.15	31	.37	-65	0.88	11.9
1500	.50	-167	1.65	56	.18	27	.38	-76	1.07	8.0
2000	.48	175	1.29	38	.21	22	.40	-90	1.15	5.5
2500	.47	168	1.06	27	.23	17	.43	-99	1.24	3.7
3000	.47	163	0.93	15	.25	13	.48	-109	1.2	3.0

V_{CE} = 5 V, I_C = 15 mA

100	.54	-93	20.27	128	.01	63	.70	-38	0.69	33.1
500	.60	-163	5.74	87	.04	49	.21	-65	1.32	18.2
1000	.60	-180	3.00	70	.09	50	.18	-75	1.18	12.7
1500	.55	174	2.04	55	.13	44	.22	-85	1.26	8.9
2000	.56	161	1.57	40	.16	36	.28	-98	1.23	7.0
2500	.56	154	1.26	31	.19	33	.33	-106	1.22	5.4
3000	.55	149	1.09	20	.21	28	.39	-114	1.2	4.4

V_{CE} = 10 V, I_C = 3 mA

100	.83	-31	8.60	150	.01	77	.94	-13	0.24	29.3
500	.59	-113	4.54	102	.10	41	.56	-41	0.57	16.6
1000	.52	-146	2.57	77	.14	35	.44	-53	0.85	12.6
1500	.47	-160	1.80	58	.17	29	.45	-63	1.03	9.2
2000	.45	-178	1.42	40	.20	24	.45	-78	1.11	6.5
2500	.44	175	1.15	29	.22	19	.47	-87	1.21	4.4
3000	.44	170	1.00	17	.24	14	.52	-97	1.18	3.6

V_{CE} = 10 V, I_C = 15 mA

100	.55	-79	21.22	131	.01	65	.75	-30	0.59	33.3
500	.55	-157	6.37	89	.04	50	.29	-45	1.23	19.1
1000	.55	-174	3.31	71	.08	51	.25	-53	1.23	13.3
1500	.53	178	2.26	57	.12	44	.29	-65	1.2	10.0
2000	.53	165	1.71	41	.16	38	.33	-81	1.13	8.1
2500	.52	158	1.38	31	.18	33	.37	-91	1.2	6.1
3000	.52	153	1.19	21	.20	29	.43	-101	1.14	5.5

Note:

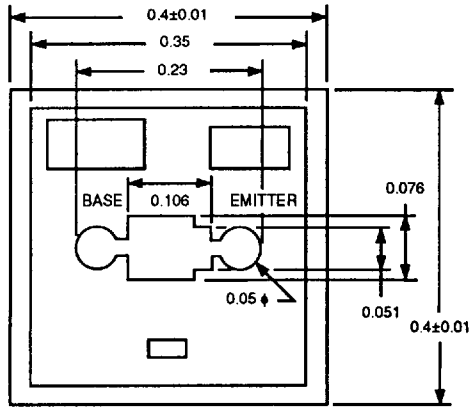
1. Gain Calculations:

$MAG = \frac{|S_{21}|}{|S_{12}|}\left(K \pm \sqrt{K^2 - 1}\right)$. When $K \leq 1$, MAG is undefined and MSG values are used. $MSG = \frac{|S_{21}|}{|S_{12}|}$, $K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}S_{21}|}$ $\Delta = S_{11}S_{22} - S_{21}S_{12}$

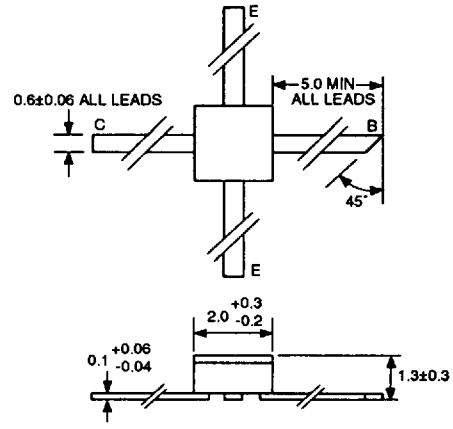
MAG = Maximum Available Gain
MSG = Maximum Stable Gain

OUTLINE DIMENSIONS (Units in mm)

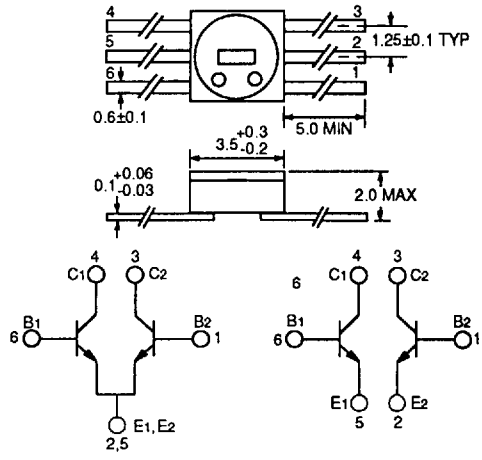
NE32700 (CHIP)



PACKAGE OUTLINE 08



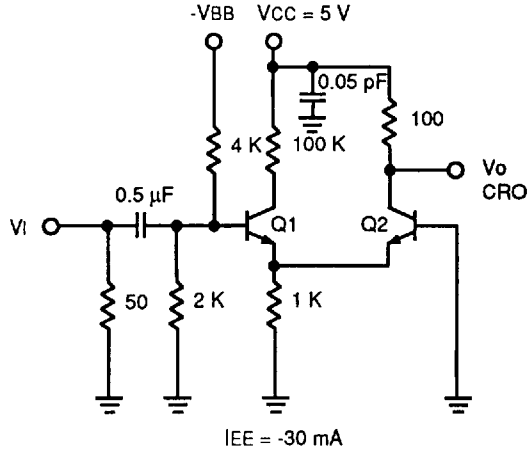
PACKAGE OUTLINE 40A/B



40A Internal Connection

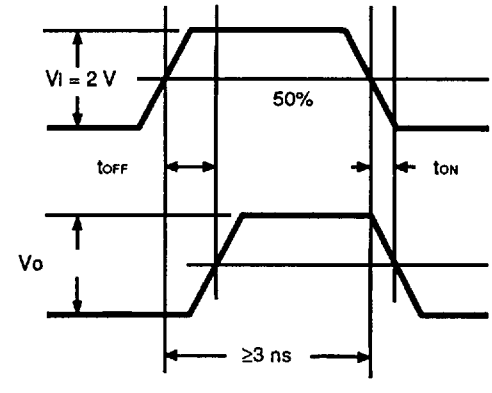
40B Internal Connection

TEST CIRCUITS



ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS

t_{ON} 0.7 ns TYP
t_{OFF} 0.5 ns TYP



INPUT AND OUTPUT WAVEFORMS AND DEFINITION TO t_{ON} and t_{OFF}

Notes:
1. Base voltage V_{BB} is adjusted so that Ic of Tr1 is zero when V_I is zero.
2. Ic variation range is between zero and about 30 mA.