F10168 • F10568

F10K VOLTAGE COMPENSATED ECL

QUAD LATCH/GATED OUTPUTS

DESCRIPTION – The F10168 and F10568 contains four D type latches with a Common Enable (E_C). When E_C is HIGH, outputs will follow the D inputs. Information is latched on the negative-going edge of E_C. Each latch output is combined with a separate gate control (G_n), allowing the final output (Q_n) to be forced LOW for wired-OR data bus applications.

PIN NAMES

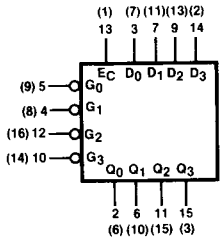
C_n	Data Inputs
$\overline{G}_n$	Output Gate Controls (Active LOW)
E_C	Common Enable (Active HIGH)
Q_n	Outputs

TRUTH TABLE

$\overline{G}$	E_C	D	Q_{t+1}
H	X	X	L
L	L	X	Q_t
L	H	L	L
L	H	H	H

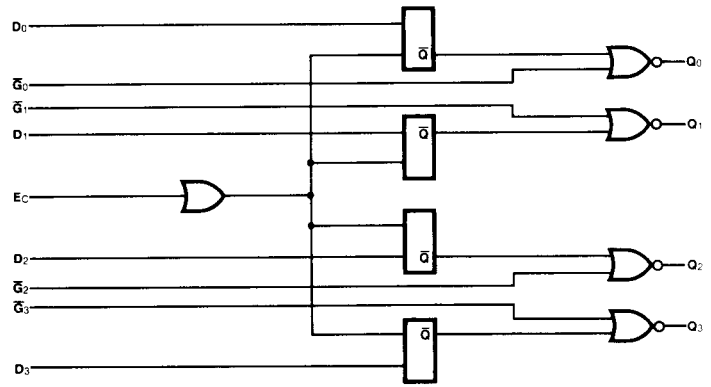
t, t + 1 = time before and after E_C negative transition.

LOGIC SYMBOL

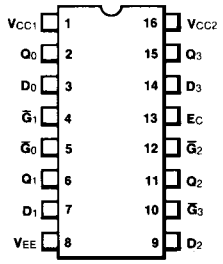


V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



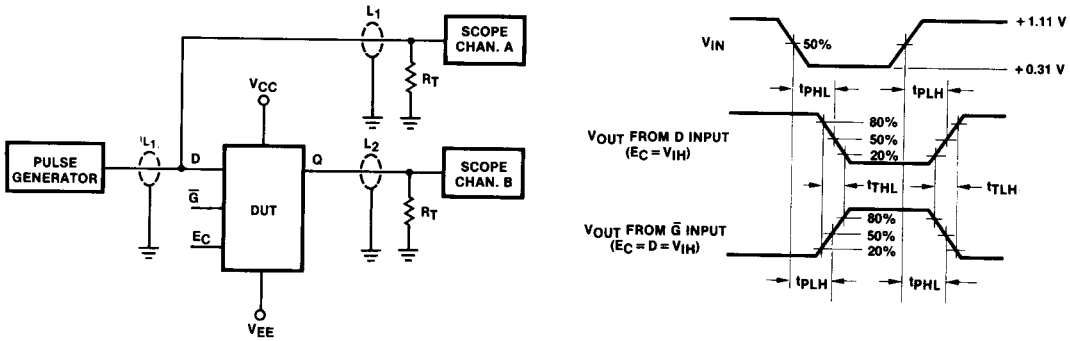
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS
I_{IH}	Input Current HIGH Data Enable Gate			 245 290 265	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Supply Current	−75	−60		mA	25°C	Inputs and Outputs Open

AC CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay, Enable and Data Gate	 1.0 1.0	 4.0 2.0	 5.4 3.5	ns ns	See Figure 1
t_{TLH}, t_{THL}	Transition Time, (20% to 80%) (80% to 20%)	1.5	2.0	3.5	ns	
t_s	Set-Up Time	2.5	−0.1		ns	
t_h	Hold Time	1.5	+0.1		ns	

SWITCHING CIRCUIT AND WAVEFORMS



L_1 and L_1 = equal length 50 Ω impedance lines
$R_T = 50$ Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 uF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Figure 1