PROGRAMMABLE, HIGH PERFORMANCE MULTI-PHASE, PWM CONTROLLER

SC1144

Preliminary - March 22, 1999

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1144 is a high performance, multi-phase (PWM) controller designed for high power microprocessors requiring ultra fast transient response, such as the Pentium® II and beyond. Utilizing a novel and unique design, the controller distributes the output load across (up to) four converter channels by digitally phase shifting the PWM outputs. This approach greatly reduces the stress and heat on the output stage components while lowering input ripple current by as much as 80%. Accurate current sharing among the four phases is achieved by precision design techniques and trimming of critical elements.

The high speed transconductance error amplifier is externally initialized using a soft-start capacitor allowing the controller to "wake-up" without overshoot, thus protecting the low voltage microprocessor loads. The output drive voltage to the power MOSFETs is programmable to minimize switching losses in the drive circuitry.

The output voltage is digitally programmable by means of a 5 bit DAC. A single resistor programs the master clock frequency (8MHz max) or the clock can be supplied by an external source where exact frequency control is desired. The number of operating phases is programmed independently of the external clock. The parts features under-voltage lock-out with hysteresis and over-current protection.

FEATURES

- Allows use of small surface mount components
- Ultra fast transient recovery time
- Wide, High frequency operating range
- Selectable 2, 3, 4 phase operation
- 5-bit DAC programmable output
- Precision load current sharing
- Selectable internal or external clock
- Soft start, Over current protection

APPLICATIONS

- High end servers and workstations
- High current/Ultra-fast transient microprocessors

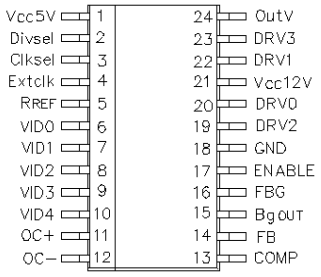
ORDERING INFORMATION

DEVICE (1)	PACKAGE	TEMP. (T_J)
SC1144ABCSW	SO-24	0 - 85°C

Note:
(1) Add suffix 'TR' for tape and reel.

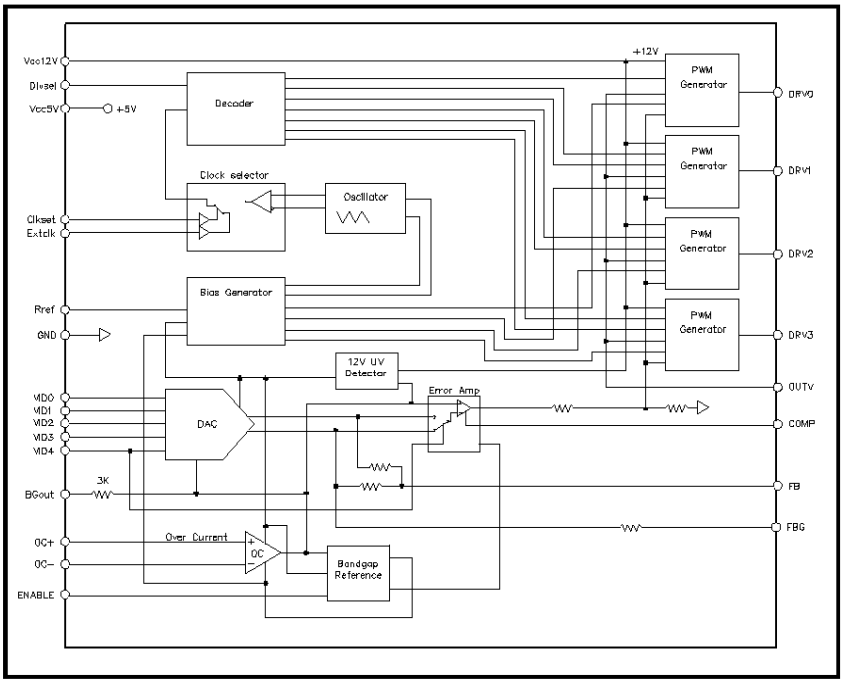
PIN CONFIGURATION

Top View



(24-Pin SOIC)

BLOCK DIAGRAM



The SC1144 is patent pending

Pentium is a registered trademark of Intel Corporation

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits	Units
V_{CC5V} to GND	V_{cc5v}	-0.3 to + 12	V
FBG to GND	FBG	± 1	V
V_{CC12V} to GND	V_{cc12v}	-0.3 to +20	V
Operating Temperature Range	T_A	0 to +70	°C
Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
Thermal Resistance Junction to Case	θ_{JC}	25	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	80	°C/W
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: T_A = 25°C, $V_{CC\ 5V}$ = 5V, $V_{CC\ 12V}$ = 12V, 4-Phase operation.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC12V}		10.0	12.0	14.0	V
UVLO Range	V_{CC5V}			3.9		V
UVLO Hystersis	V_{CC5V}			50		mV
UVLO Range	V_{CC12V}			9.0		V
UVLO Hystersis	V_{CC12V}			100		mV
Supply Voltage Range	V_{CC5V}		4.5	5.0	5.5	V
Supply Current	V_{CC12V}	DRV Outputs open		12	20	mA
Supply Current	V_{CC5V}	V_{OUT} = 2.00V, I_O = 0			40	mA
Reference Current Pin Voltage	V_{REF}	Iref = 250µA		2.05		V
Vid0-4 Clock Select & Divide	V_{INL}	Logic Low			0.8	V
Select Logic Threshold	V_{INH}	Logic High	2			V
Vid0-4 Clock Select & Divide	I_{INL}	Vid0-4=0V			-20	µA
Select Input Bias Current	I_{INH}	Vid0-4=4.5V			+50	µA
Enable Pin	V_{INL}				.8	V
	V_{INH}		2			V
Maximum Duty Cycle	D_{MAX}	FB = 0V		75		%
DRV0-3 Output Voltage	V_{OL}	I_{sink} = 1mA			.3	V
	V_{OH}	I_{source}=1ma,OUTV=V_{cc12}	V_{CC12} -1			V
DRV0-3 Source Current	I_{SRC}	V_{OUT} = 2.00V		40		mA
DRV0-3 Sink Current	I_{SNK}	V_{OUT} = 2.00V		20		mA

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ELECTRICAL CHARACTERISTICS (Cont.)

Unless otherwise noted: T_A = 25°C, V_{CC5V} = 5V, V_{CC12V} = 12V, 4-Phase operation.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bgout Voltage	V_{Bgout}	Vid = 00000	2.03	2.05	2.08	V
Bgout Impedance	R_{O_Bg}			3		KΩ
External Clock Freq. Range	F_{ext_CK}		.80	8.0	8.5	MHz
Oscillator Frequency	F_{OSC}	Iref = 250µA	7.6	8.0	8.4	MHz
Internal Clock Freq. Range	F_{int_CK}		.80	8.0	8.5	MHz
Match DRV0-3	Δ_D	Duty cycle (Avg) = 50%	-1		+1	%
PWM Off Time	Toff			25		%
Drive Voltage Range	OutV	Output Freq. = 2MHz/Phase V_O = 2.000V		10		V
Overcurrent Comparator, Comparator, Common Mode Range	OCC_CMR		3		15	V
OC+I/P bias Current	IB_OC+	Vin = 5V	+75		+250	µA
OC-I/P bias Current	IB_OC-	Vin = 5V	+75		+250	µA
Input Offset Voltage	VOS_OCC	Vin = 5V		10		mV
Feedback Input Impedance	Ri_FB	V_O = 2.00V		12		KΩ
Duty Cycle Range	D				75	%
CONVERTER SPECIFICATIONS, Reference Application Circuit						
Output Accuracy Over Set Range	V_{OUT}	VID 0-4 = 0000-1111 V_{CC5V} = 5.0V	-1		+1	%
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_O}$	V_O = 2.000V I_O = 3A - 20A		.025	.05	%/A
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{CC5V} = 5V, V_O = 2.000V V_{IN} = 4-6V, (vin separated from Vcc5v) I_O = 5A , Clk = external		.15		%/V

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PIN DESCRIPTION

Pin #	Pin Name	Pin Function
1	$V_{CC\ 5V}$	Supply voltage input (5V nominal)
2	Divsel	Connect to Gnd for four phase operation and to logic High for three Phase operation.
3	Clksel	Clock Select: Logic high selects internal clock. Logic low selects external clock.
4	Extclk	External Clock Input. The output frequency is determined by (Clock Input Freq.)/4. Output freq.= (Clock Input)/4. Pull up to Vcc5v to select internal clock.
5	R_{REF}	Connects to external reference resistor. Sets the operating frequency of the internal clock and the ramp time for the PWM. Reference voltage at this pin is 2.05V. Trimmed to set 250µA at 8MHz.
6	VID0(1)	Programming Input (LSB)
7	VID1(1)	Programming Input
8	VID2(1)	Programming Input
9	VID3(1)	Programming Input
10	VID4(1)	Programming Input (MSB)
11	OC+	Over current comparator. Non-Inverting input.
12	OC-	Over current comparator. Inverting input.
13	COMP	Compensation Pin. Compensation is acheived by connecting a capacitor in series with a resistor between this pin and FBG. A 300k ohm resistor must also be directly connected between this pin and FBG.
14	FB	Feedback input connected to supply output.
15	B_{GOUT}	Bandgap Reference Output. Output resistance=3kohm. Must be bypassed with 4.7nf -100nf capacitor to FBG. This capacitor programs the soft start time.
16	FBG	Feedback Ground. This pin must be connected to return side of output caps.
17	ENABLE	Connects to 5V to enable. Connect to GND to disable entire device.
18	GND	Ground Pin
19	DRV2	Phase 2 output
20	DRV0	Phase 0 output
21	V_{CC12V}	Supply voltage for the FET Drivers/DRV0-3
22	DRV1	Phase 1 output
23	DRV3	Phase 3 output
24	OutV	Sets the maximum DRV0-3 drive voltage in order to reduce switching losses in the external MOSFETs.

NOTE: (1) All logic inputs and outputs are open collector TTL compatible.

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OUTPUT VOLTAGE

Unless specified: 0 = GND; 1 = High (or Floating).
T_A = 25°C, V_{CC5V} = 5V, V_{CC12V} = 12V, 4-Phase operation.

PARAMETER	VID 43210	MIN	TYP	MAX
Output Voltage	01111	1.287	1.300	1.313
	01110	1.336	1.350	1.364
	01101	1.386	1.400	1.414
	01100	1.435	1.450	1.465
	01011	1.485	1.500	1.515
	01010	1.534	1.550	1.566
	01001	1.584	1.600	1.616
	01000	1.633	1.650	1.667
	00111	1.683	1.700	1.717
	00110	1.732	1.750	1.768
	00101	1.782	1.800	1.818
	00100	1.831	1.850	1.869
	00011	1.881	1.900	1.919
	00010	1.930	1.950	1.970
	00001	1.980	2.000	2.020
	00000	2.029	2.050	2.071
	11111	1.980	2.000	2.020
	11110	2.079	2.100	2.121
	11101	2.178	2.200	2.222
	11100	2.277	2.300	2.323
	11011	2.376	2.400	2.424
	11010	2.475	2.500	2.525
	11001	2.574	2.600	2.626
	11000	2.673	2.700	2.727
	10111	2.772	2.800	2.828
	10110	2.871	2.900	2.929
	10101	2.970	3.000	3.030
	10100	3.069	3.100	3.131
	10011	3.168	3.200	3.232
	10010	3.267	3.300	3.333
	10001	3.366	3.400	3.434
	10000	3.465	3.500	3.535

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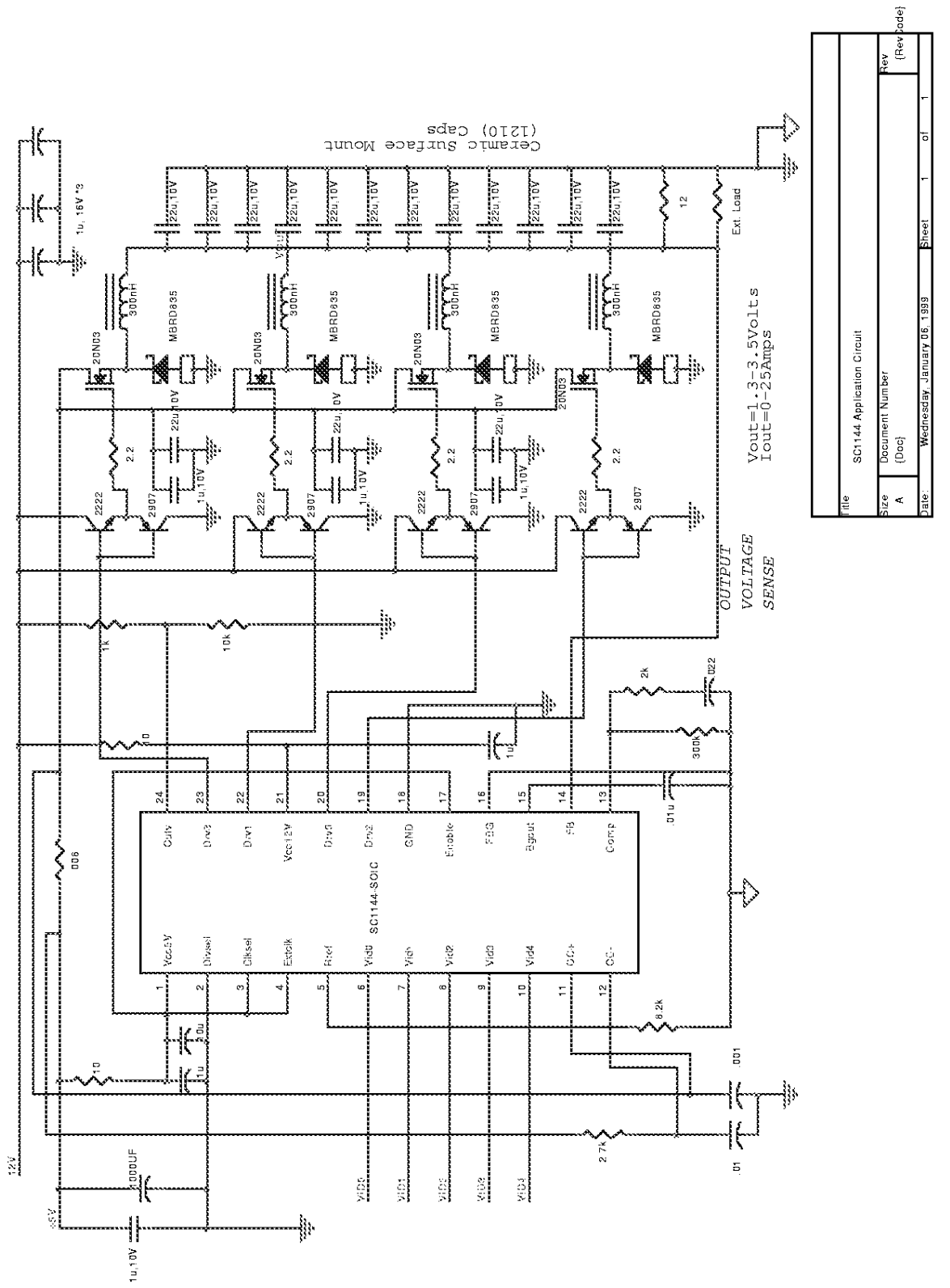
TYPICAL APPLICATION CIRCUIT



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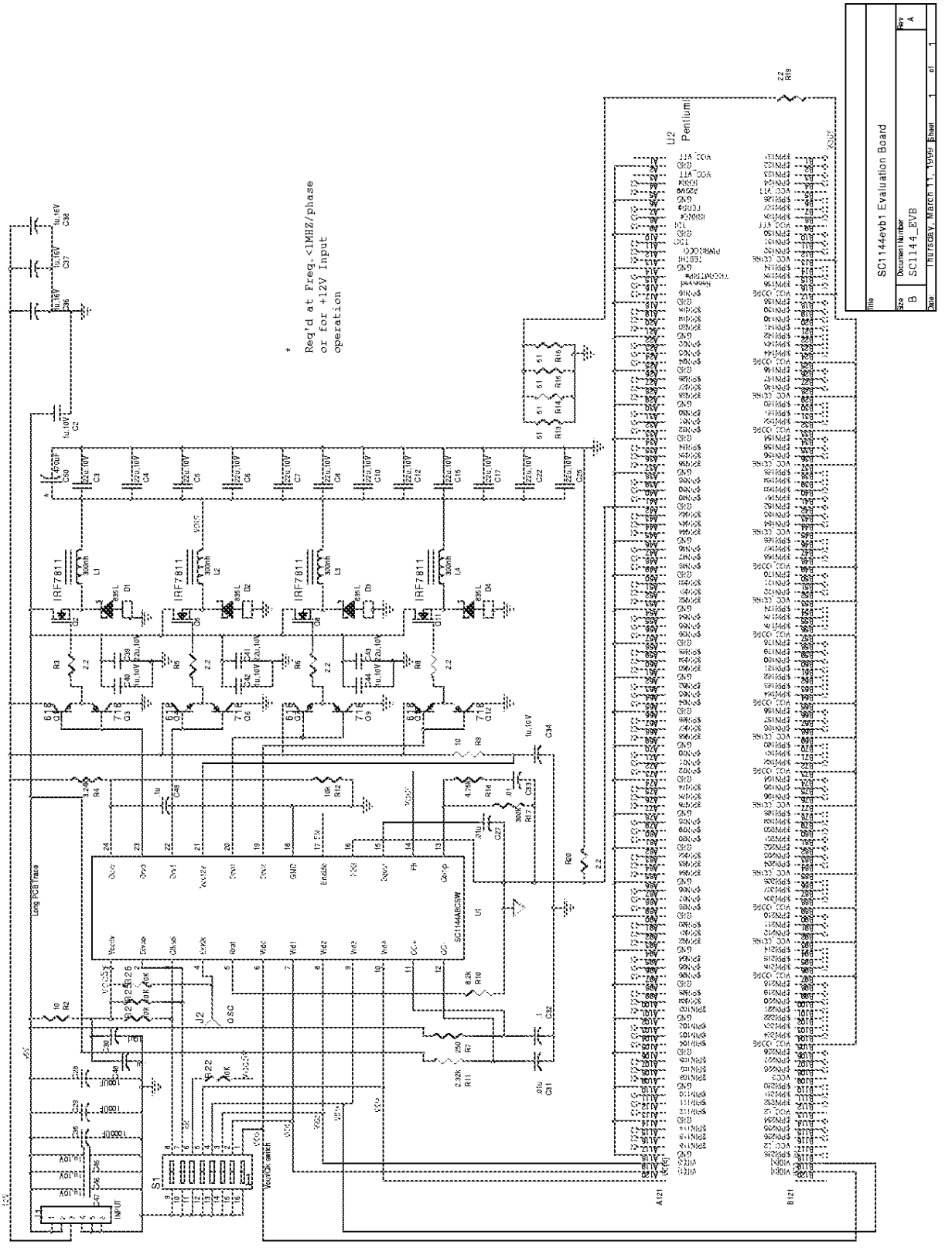
EVALUATION BOARD SCHEMATIC



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BILL OF MATERIAL

Item	Qty	Reference	Value	Manufacturer
1	11	C2,C34,C36,C37,C38,C40,C42,C44,C45,C46,C47	1u,10V	AVX (818)883-7606 X7R
2	15	C3,C4,C5,C6,C7,C8,C10,C12,C15,C17,C22,C25,C39,C41, C43	22u,10V	Murata (512)250-5082 PN #GRM235Y5V226Z010
3	2	C27,C31	.01u	AVX,Murata,Nichicon
4	2	C29,C28	100UF, 6.3v	Murata,Al. Elec.
5	1	C30	10uf, 6.3v	Murata,Al. Elec.
6	1	C32	.001	Murata
7	1	C33	.01u	Murata
8	1	C35	1000UF, 6.3v	Murata,Al. Elec.
9	1	C48	.1u	Murata,X7R
10	4	D1,D2,D3,D4	835L	Motorola
11	1	J1	INPUT	
12	1	J2	osc	
13	4	L1,L2,L3,L4	300nH, 8Amp or 450nH, 8Amp	Falco (305)662-7276 PN #T025A2 or TO25O2
14	4	Q1,Q4,Q7,Q10	FMMT618	Zetex
15	4	Q2,Q5,Q8,Q11	20N03HL	Motorola
16	4	Q3,Q6,Q9,Q12	FMMT718	Zetex
19	2	R2,R9	10	Dale,any
20	6	R3,R5,R6,R8,R19,R20	2.2	Dale
21	1	R4	680	any
22	1	R7	250	any
23	1	R10	8.2k	any
24	1	R11	2.32k	any
25	1	R12	3k	any
26	4	R13,R14,R15,R16	51, 1/4W, 1206	Dale
27	1	R17	300k	any
28	1	R18	4.75k	any
29	4	R21,R22,R25,R26	10K	any
30	1	S1	Vout/Clk switch C&K	(800)cal-swch
31	1	U1	SC1144ABCSW	Semtech (805)498-2111
32	1	U2	PentiumII conn.	Foxconn (714)256-1880

Unless otherwise noted, all resistors are 1/10W, 5%, 0805 and all capacitors are 20%, 50v, 0805.

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THEORY OF OPERATION

FUNCTIONAL DESCRIPTION

The SC1144 is a programmable, high performance, multi-phase controller designed for the most demanding DC/DC converter applications in which transient response, space, input ripple current and component form factor and cost are paramount. The SC1144 based dc/dc converter consists of four asynchronous converters. The gate drives to the converters are alternated sequentially by the SC1144 allowing equal sharing of the load current among the stages. The high clock frequency allows for smaller inductor value and miniature surface mount, low inductance output capacitors. Since each stage has ¼ the output current, the conduction losses in each stage is reduced by a factor of 1/16. Precision active trimming ensures 1% matching of duty cycles among phases, thus ensuring the heat and component stress is shared equally. This allows use of lower cost components in each phase and virtual elimination of heat sinks.

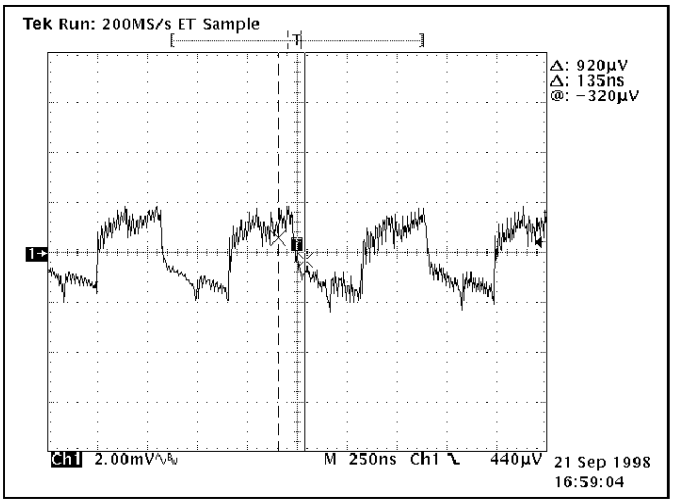

Fig. 4: V_{OUT} Ripple, V_{OUT} = 2.0V, I_{OUT} = 30A

DECODER/BIAS GENERATOR/PWM CONTROLLER

The 8 MHz clock is divided down to 2 MHz for four phase operation by the clock decoder. The start of the output pulses are time shifted 90 degrees by the decoder with respect to each other. The Bias Generator generates the ramps to each phase by a precision trimmed current source and on-chip capacitors. The decoder, which is synchronized to the bias generator via the master clock, phase shifts the ramps and enables the PWM controller sequentially. A resistor from R_{REF} pin to FBG programs the frequency and ramp time. The ramps are then compared to the error amplifier output at the high speed PWM comparator inputs. The controller outputs are buffered versions of the comparator outputs.

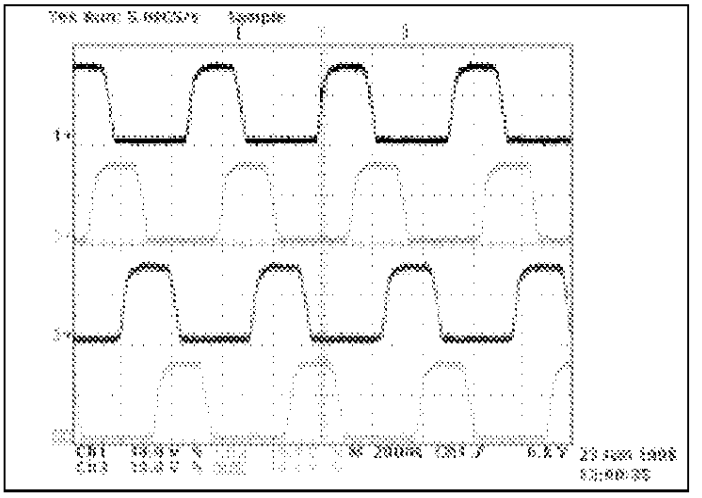

Fig. 1: The four Gate Drives firing 90° out of phase. V_{OUT} = 2.0V, I_{OUT} = 10A

ERROR AMPLIFIER

At the heart of the controller is an ultra-fast, transconductance error amplifier. Since the output inductor values can be selected to be a minimum, usually less than a micro-Henry, the delays due to inductor ramp time are minimized during transient load recovery. The higher frequency of operation also allows use of much smaller capacitance on the output. This means that the dc/dc converter output capacitors "hold Time" is less. The error amplifier must therefore respond extremely fast "Recover the Fort" after a transient. The SC1144 error amplifier recovers to its normal duty cycle after application of a full load transient within 2 usec maximum, (largely dependant on supply quality) and usually within 1usec. This minimizes undershoot and overshoot during application of a transient.

The SC1144 is patent pending

ERROR AMPLIFIER CONT.

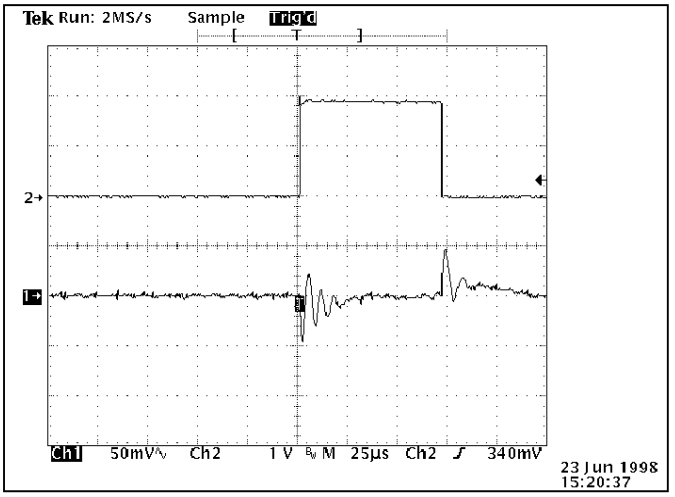

Fig. 2: Transient response, Top trace, Current sense 8A/div @ 30A/usec. Bottom trace, V_{OUT}.

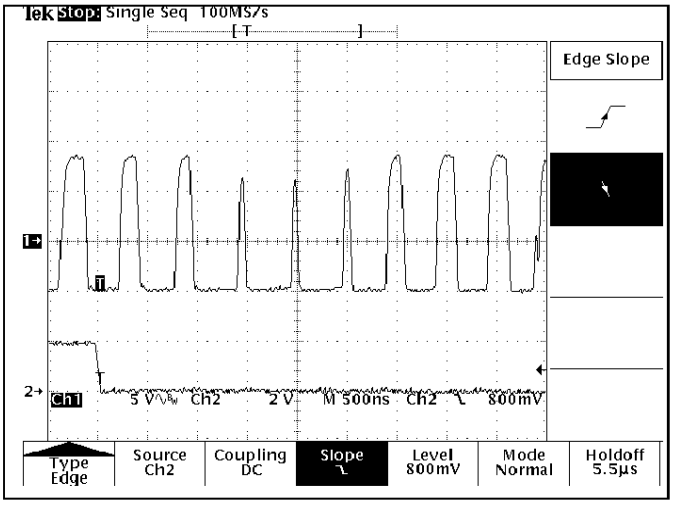

Fig. 3: Top Trace, Gate drive responding to removal of transient load. Bottom trace, Load current transient 16A/div.

The error amplifier has two inverting inputs, one for the High Range, (VID4 set to logic high) and one input for the Low Range. The effective gain of the error amplifier stays constant in both ranges keeping the loop gain constant regardless of output voltage range.

BANDGAP REFERENCE/SOFT START

The precision internal bandgap reference provides a stable, temperature compensated 2.05 V reference for the error amplifier's non-inverting input, the D_{ACREF} for the VID digital to analog converter, the under-voltage lock-out circuitry as well as the reference for the Bias generator current sources. The error amplifiers non-inverting input is connected to the bandgap reference through a 3 kohm resistor, which is also externally connected to a soft-start capacitor via the B_{GOUT} pin. Upon application of power, the non-inverting input of the error amplifier is held low for a short time allowing for the decoder and PWM controller to settle. This prevents any harmful output voltage overshoots upon start up or after a converter shut-down (as a result of over-current or the enable pin pulled low). For the preliminary version, the undervoltage lock-out circuit, depicted by * in the application schematic, is required to keep the output low for the duration of time when the Vcc5v is transitioning between 0V and 3V. This circuit will be implemented internally and will not be required for the production version. The non-inverting input then ramps up according to the RC time constant allowing gradual rise of output voltage.

OVER-CURRENT COMPARATOR

The SC1144 has an internal over-current comparator designed to sense current in the input supply path. The comparator inputs have a high common voltage range thus allowing operation under all possible voltage/current combinations. The output of the comparator pulls the B_{GOUT} (soft start) pin low thus disabling the error amplifier and causing the PWM outputs to enter minimum duty cycle mode.

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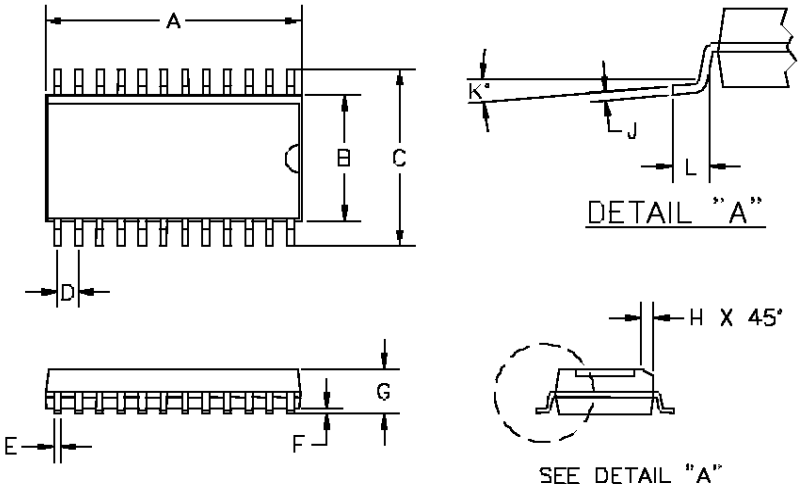
An evaluation board is available which may be ordered directly from the factory. SC1144EVB is a DC/DC converter utilizing the SC1144 four-phase controller. The evaluation board is intended as a guideline for board design, layout and to assess key performance parameters, such as transient response, thermal stress management and input and output ripple considerations. The SC1144EVB includes a SLOT1 connector for Pentium II, a DIP switch for mode/voltage selection as well as qualified selection of components for the SC1144 operation. The SC1144EVB user manual contains useful applications information and may be accessed from our website at semtech.com.

OUTLINE DRAWING - SO-24



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.5985	.6141	15.20	15.60	(2)
B	.2914	.2992	7.40	7.60	(2)
C	.394	.419	10.00	10.64	—
D	.050	BSC	1.27	BSC	—
E	.013	.020	.33	.51	—
F	.004	0.118	.10	.30	—
G	.0926	.1043	2.35	2.64	—
H	.010	.029	.25	.74	—
J	.0091	.0125	.23	.32	—
K	0°	8°	0°	8°	—
L	.016	.050	.41	1.27	—

JEDEC MS-013AD

B17104B

(2) DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS
(1) CONTROLLING DIMENSION : MILLIMETERS.

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