

SRM20100LT85/10

CMOS 1M-BIT STATIC RAM

● Industrial Temperature Range

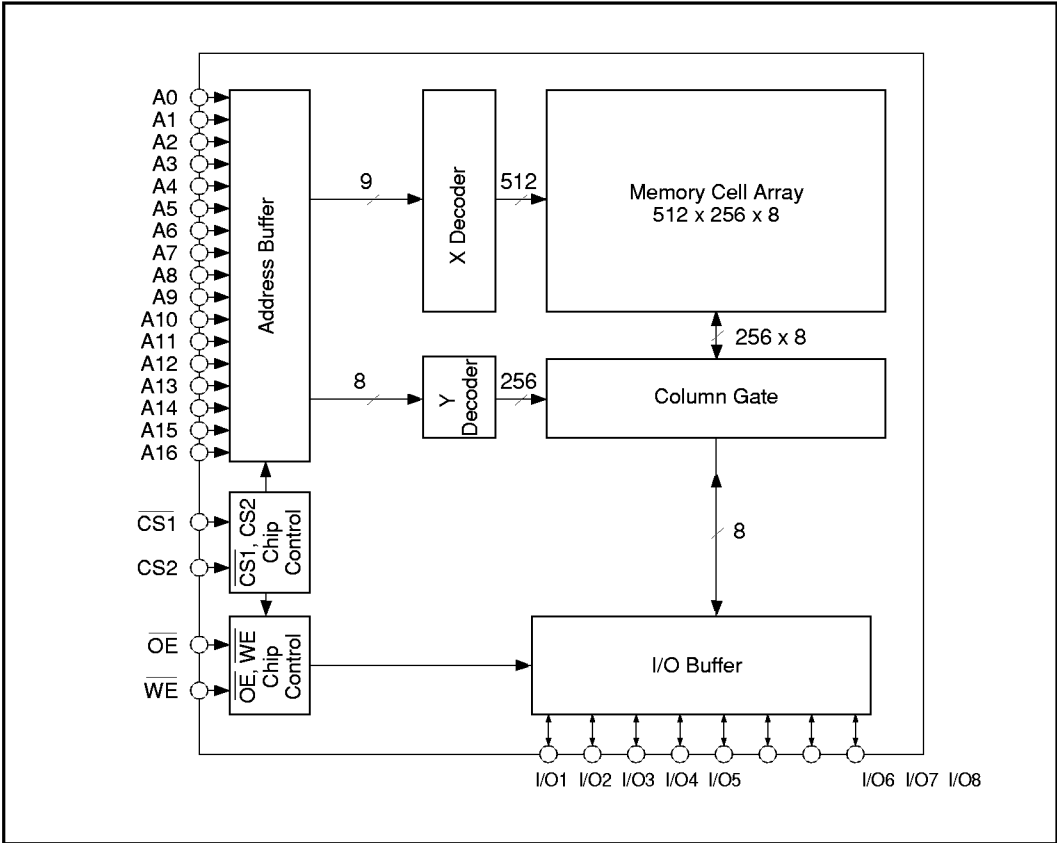
■ DESCRIPTION

The SRM20100LT85/10 is a 131,072 words x 8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

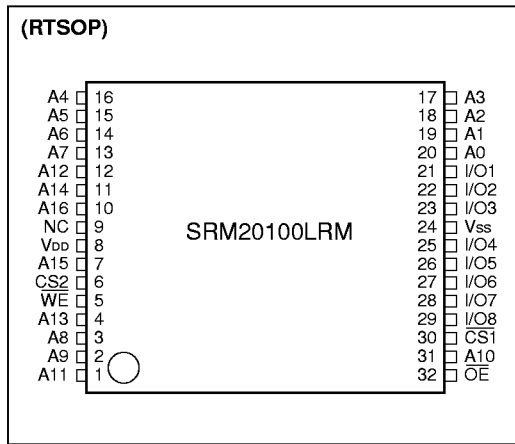
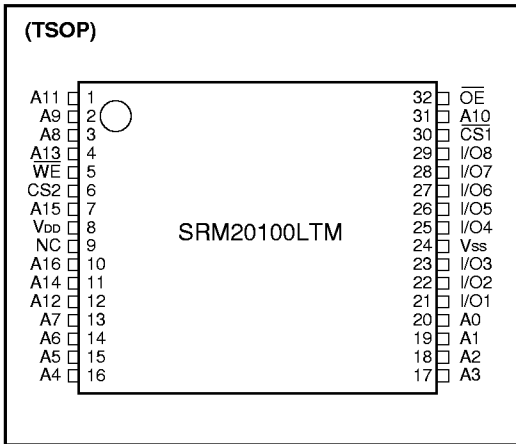
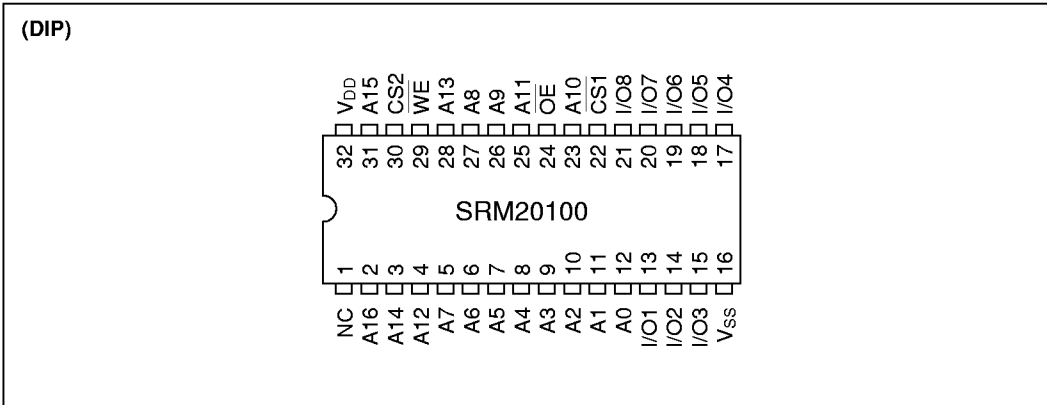
■ FEATURES

- Industrial temperature range . . . (-40 to 85°C)
- Access time SRM20100LT85 85ns (Max)
SRM20100LT10 100ns (Max)
- Low supply current Standby 2µA (Typ)
Operation 15mA/MHz (Typ)
- Completely static No clock required
- Single power supply 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capacity
- Non-volatile storage with battery back-up batteries
- Package SRM20100LCT85/10 32-pin DIP (plastic) (-40 to 85°C)
SRM20100LMT85/10 32-pin SOP (plastic) (-40 to 85°C)
SRM20100LTMT85/10 32-pin TSOP (plastic) (-40 to 85°C)
SRM20100LRMT85/10 32-pin RTSOP (plastic) (-40 to 85°C)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A16	Address Input
\overline{WE}	Write Enable
\overline{OE}	Output Enable
$\overline{CS1}$	Chip Select 1
CS2	Chip Select 2
I/O1 to 8	Data Input/Output
VDD	Power Supply (+5V)
VSS	Power Supply (0V)
NC	No Connection

■ ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage	V _{DD}	-0.5 to 7.0	V
Input voltage*	V _I	-0.5 to 7.0	V
Input/output voltage*	V _{I/O}	-0.5 to V _{DD} + 0.3	V
Power dissipation	P _D	1.0	W
Operating temperature	T _{OPR}	-40 to 85	°C
Storage temperature	T _{STG}	-65 to 150	°C
Soldering temperature and time	T _{SOL}	260°C, 10s (Lead only)	—

* V_I, V_{I/O} (Min.) = 3.0V (pulse width is 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD}	—	4.5	5.0	5.5	V
	V _{SS}	—	0	0	0	V
Input voltage	V _{IH}	—	2.2	3.5	V _{DD} + 0.3	V
	V _{IL}	—	-0.3*	—	0.8	V

* If pulse width is less than 50ns, it is -3.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

 $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -40$ to 85°C

Parameter	Symbol	Conditions	SRM20100L85/10			Unit
			Min	Typ*	Max	
Input leakage current	I _{LI}	$V_i = 0$ to V_{DD}	-1	—	1	μA
Standby supply current	I _{DDS}	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$	—	1	3.0	mA
	I _{DDS1}	$\overline{CS1} = CS2 \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V$	—	2	200	μA
Average operating current	I _{DDA}	$V_i = V_{IL}, V_{IH}$ $I_{I/O} = 0\text{mA}$, $t_{CYC} = \text{Min}$	—	45	70	mA
Operating supply current	I _{DDO}	$V_i = V_{IL}, V_{IH}$ $I_{I/O} = 0\text{mA}$	—	15	35	mA
Output leakage	I _{LO}	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{I/O} = 0$ to V_{DD}	-1	—	1	μA
High level output voltage	V _{OH}		2.4	$V_{DD} - 0.1$	—	V
Low level output voltage	V _{OL}		—	0.2	0.4	V

* Typical values are measured at $T_a = 25^\circ\text{C}$ and $V_{DD} = 5.0V$

● Terminal Capacitance

 $(f = 1\text{MHz}, T_a = 25^\circ\text{C})$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address capacitance	C _{ADD}	$V_{ADD} = 0V$	—	—	10	pF
Input capacitance	C _I	$V_i = 0V$	—	—	10	pF
I/O capacitance	C _{I/O}	$V_{I/O} = 0V$	—	—	10	pF

SRM20100LT85/10

● AC Electrical Characteristics

○ Read Cycle

$V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -40$ to $85^\circ C$

Parameter	Symbol	Conditions	SRM20100LT85		SRM20100LT10		Unit
			Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	*1	85	—	100	—	ns
Address access time	t _{ACC}		—	85	—	100	ns
$\overline{CS1}$ access time	t _{ACS1}		—	85	—	100	ns
CS2 access time	t _{ACS2}		—	85	—	100	ns
\overline{OE} access time	t _{OE}		—	45	—	50	ns
$\overline{CS1}$ output set time	t _{CLZ1}	*2	10	—	10	—	ns
$\overline{CS1}$ output floating	t _{CHZ1}		—	30	—	35	ns
CS2 output set time	t _{CLZ2}		10	—	10	—	ns
CS2 output floating	t _{CHZ2}		—	30	—	35	ns
\overline{OE} output set time	t _{OLZ}		5	—	5	—	ns
\overline{OE} output floating	t _{OHZ}		—	30	—	35	ns
Output hold time	t _{OH}	*1	10	—	10	—	ns

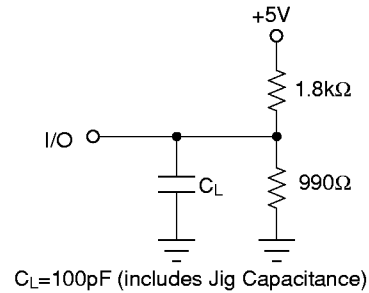
o Write Cycle

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = -40 to 85°C

Parameter	Symbol	Conditions	SRM20100LT85		SRM20100LT10		Unit
			Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	*1	85	—	100	—	ns
CS1 time	t _{CW1}		70	—	80	—	ns
CS2 time	t _{CW2}		70	—	80	—	ns
Address enable time	t _{AW}		70	—	80	—	ns
Address setup time	t _{AS}		0	—	0	—	ns
Write pulse width	t _{WP}		65	—	75	—	ns
Address hold time	t _{WR}		0	—	0	—	ns
Input data setup time	t _{DW}		35	—	40	—	ns
Input data hold time	t _{DH}		0	—	0	—	ns
\overline{WE} output floating	t _{WHZ}	*2	—	30	—	35	ns
\overline{WE} output setup time	t _{OW}		5	—	5	—	ns

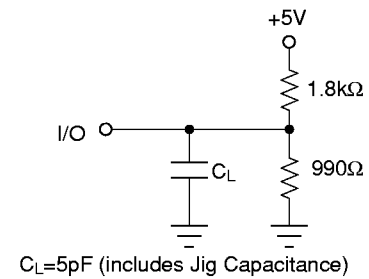
***1. Test Conditions**

1. Input pulse level: 0.6V to 2.4V
2. tr = tf = 5ns
3. Input and output timing reference levels : 1.5V
4. Output load C_L = 100pF



***2. Test Conditions**

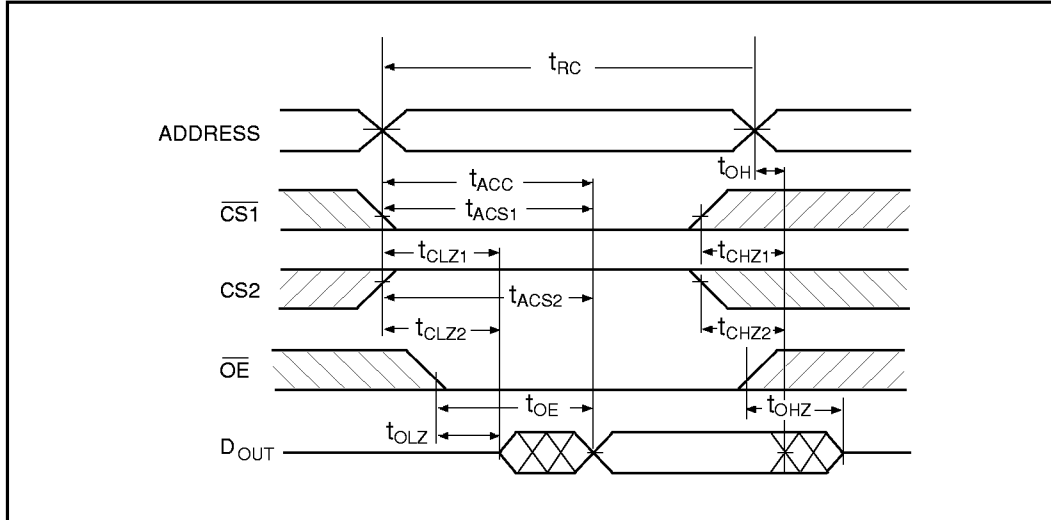
1. Input pulse level: 0.6V to 2.4V
2. tr = tf = 5ns
3. Input timing reference levels : 1.5V
4. Output timing reference levels: ± 200mV (the level displaced from stable output voltage level)
5. Output load C_L = 5pF



SRM20100LT85/10

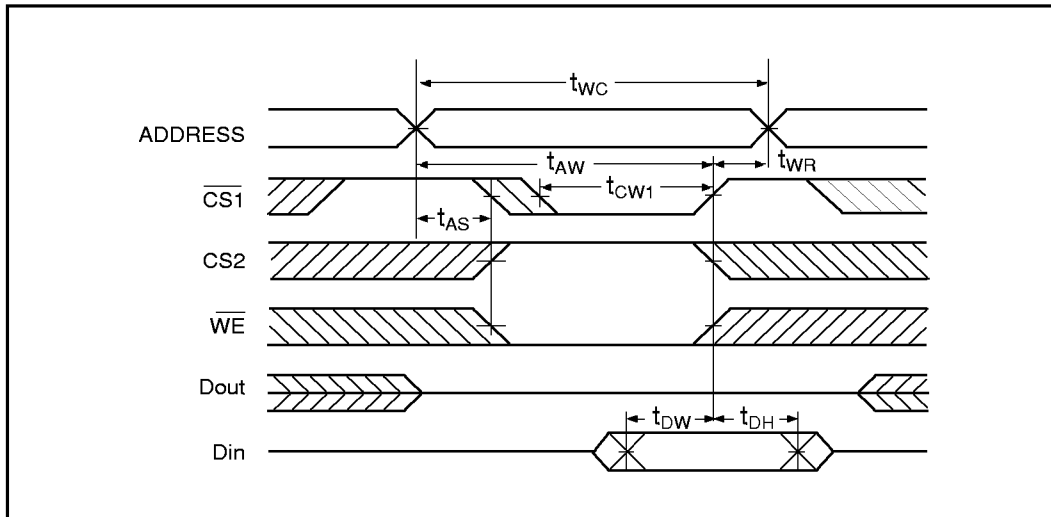
● **Timing Charts**

○ **Read Cycle*1**



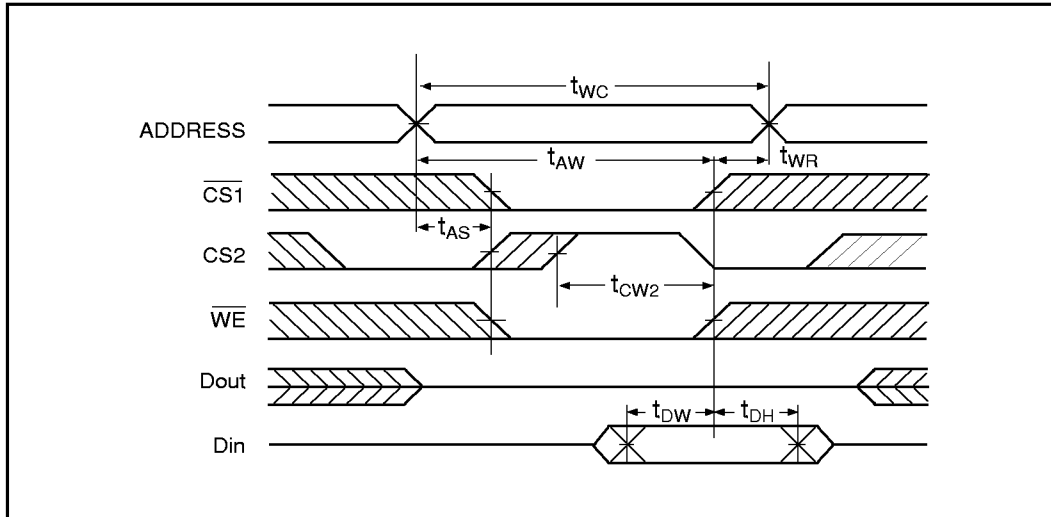
Note: *1. During read cycle time, \overline{WE} should be "H" level.

○ **Write Cycle (1) ($\overline{CS1}$ Control)*2**

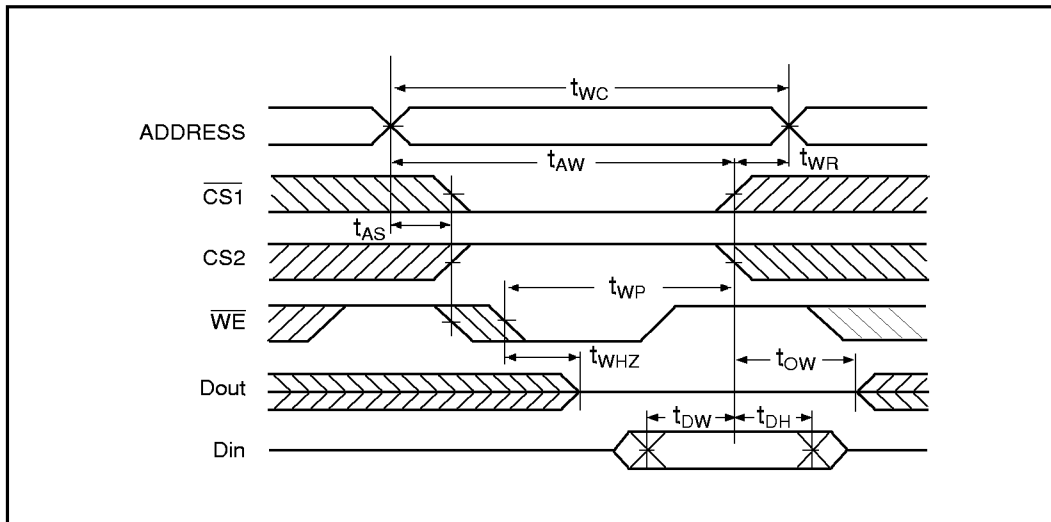


Note: *2. During write cycle time that is controlled by $\overline{CS1}$ or $\overline{CS2}$, the output buffer is in high impedance state, whether \overline{OE} level is "H" or "L".

o Write Cycle (2) (CS2 Control)



o Write Cycle (3) (\overline{WE} Control)*3, *4



Note: *3. During the write cycle that is controlled by \overline{WE} , the output buffer is in high impedance state if \overline{OE} is "H" level.
 *4. When I/O terminals are in output mode, be careful not to send conflicting (opposite) signals to the I/O terminals.

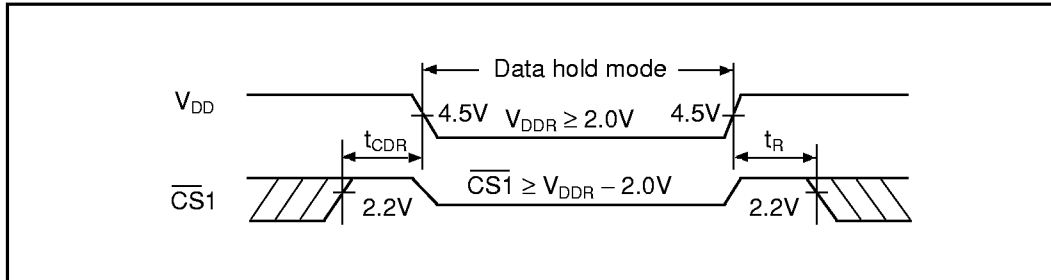
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

($T_a = -40$ to 85°C)

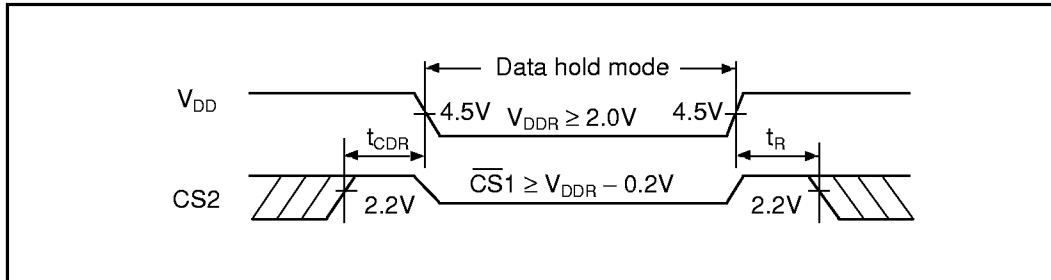
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	$V_{\text{DD}} = 3\text{V}$ $\overline{\text{CS}}1 = \text{CS}2 \geq V_{\text{DD}} - 0.2\text{V}$ or $\text{CS}2 < 0.2\text{V}$	—	1	100	μA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_{R}		t_{RC}^*	—	—	ms

* t_{RC} = Read cycle time

● Data Retention Timing ($\overline{\text{CS}}1$ Control)



● Data Retention Timing (CS2 Control)



■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	\overline{OE}	\overline{WE}	Data I/O	Mode	IDD
H	X	—	—	Hi-Z	Unselected	IDDs, IDDS1
—	L	—	—	Hi-Z	Unselected	IDDs, IDDS1
L	H	X	L	Input data	Write	IDDO
L	H	L	H	Output data	Read	IDDO
L	H	H	H	Hi-Z	Output disable	IDDO

X: "H" or "L"

—: "H", "L" or "Hi-Z"

● Reading Data

Data can be read by setting the addresses as follows:

$\overline{CS1}$ — low CS2 — high \overline{OE} — low \overline{WE} — high

Since data I/O terminals are in a high-impedance state when \overline{OE} is high, the data bus line can be used for other operations, reducing data access time.

● Writing Data

The four methods of writing data into memory are as follows:

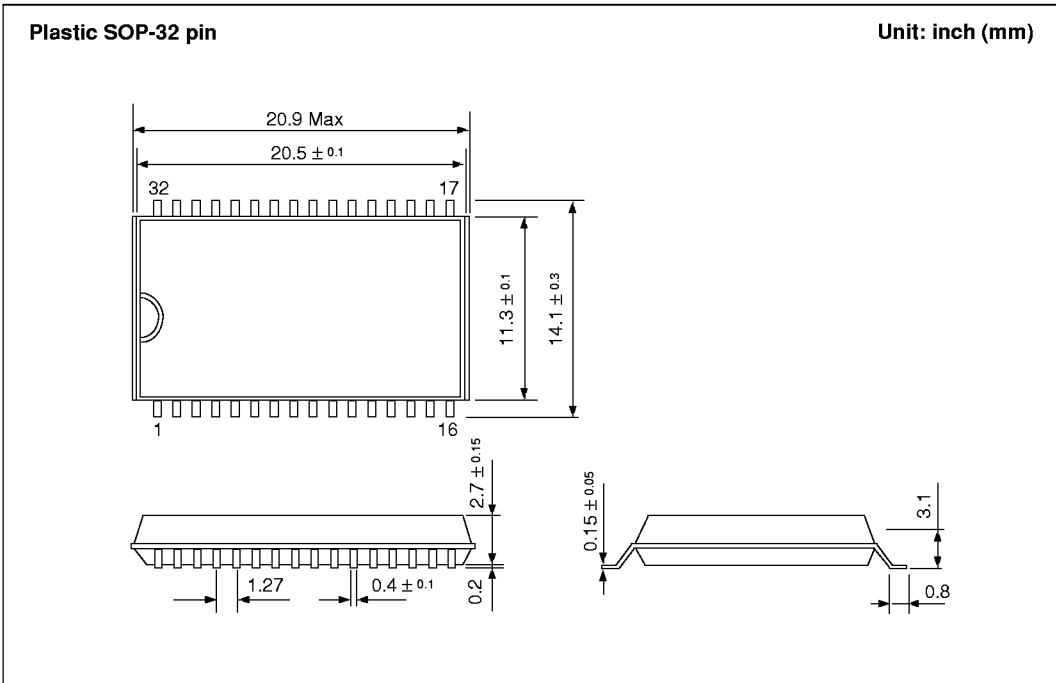
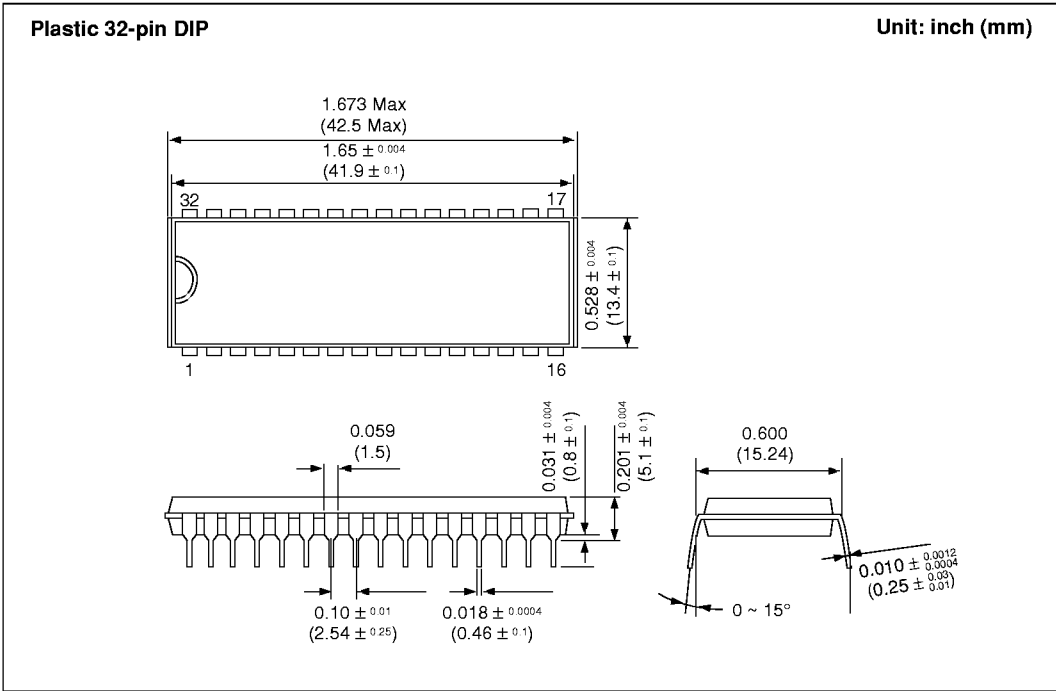
1. Set CS2 high, \overline{WE} low, set addresses and send a low pulse to $\overline{CS1}$.
2. Set $\overline{CS1}$ low, \overline{WE} low, set addresses and send a high pulse to CS2.
3. Set $\overline{CS1}$ low, CS2 high, set addresses and send a low pulse to \overline{WE} .
4. Set addresses, send a low pulse to $\overline{CS1}$ and \overline{WE} , and send a high pulse to CS2.

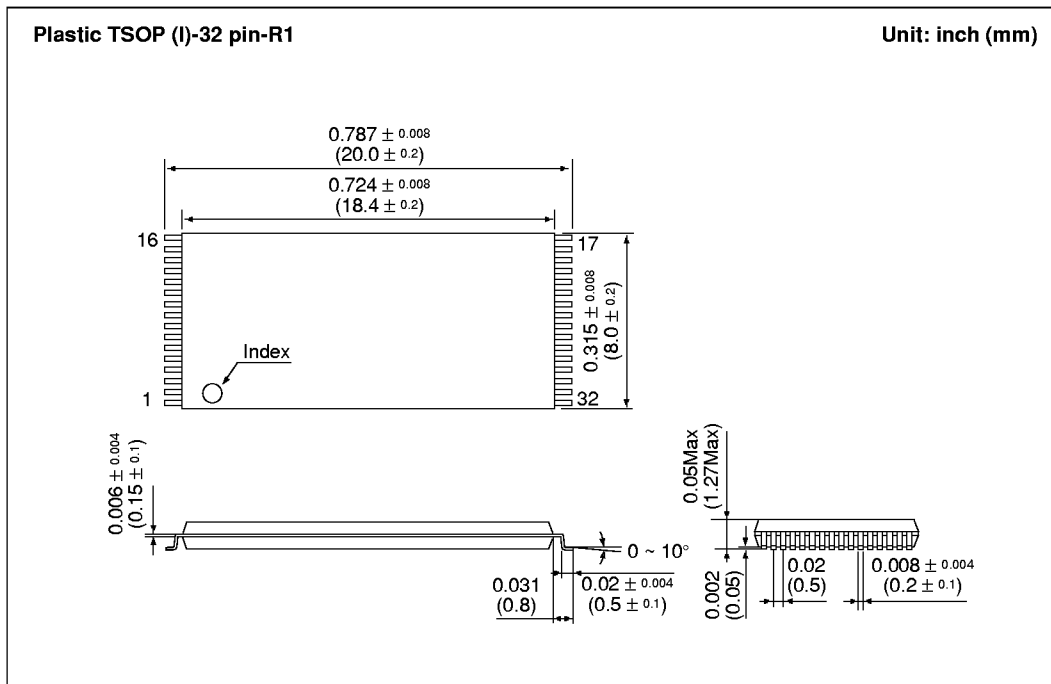
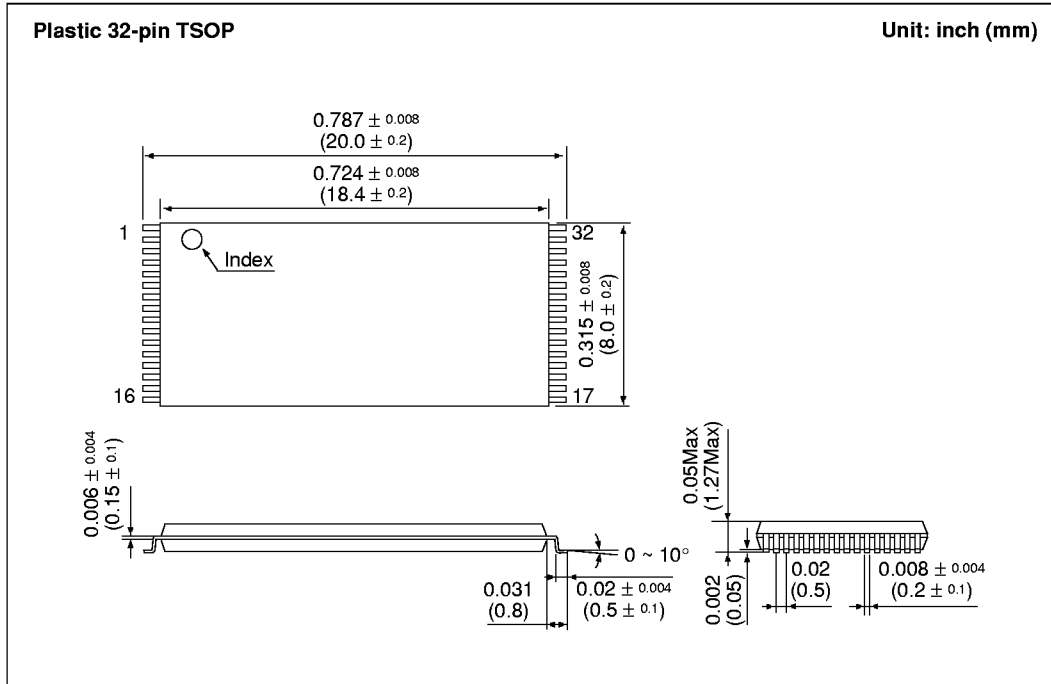
No matter which data writing configuration is used, data at the data I/O terminals are latched to the SRM20100LT85/10 at the end of the period that $\overline{CS1}$ and \overline{WE} are low, and CS2 is high. Since Data I/O terminals are always in a high-impedance state when $\overline{CS1}$ and \overline{OE} are high, and when CS2 is low, data bus contention is avoided.

● Standby Mode

When $\overline{CS1}$ is high, or CS2 is low, the SRM20100LT85/10 is in standby mode. During this state, data I/O terminals are Hi-Z, and all address inputs, data, and \overline{WE} can be either high or low. When $\overline{CS1}$ and CS2 are greater than $V_{DD}-0.2V$ or when CS2 is less than 0.2V, current flow in the SRM20100LT85/10 is negligible, except in high resistance areas.

■ PACKAGE DIMENSIONS





■ CHARACTERISTIC CURVES

