National Semiconductor Corporation

DM7556/DM8556 TRI-STATE® Programmable Binary Counters

General Description

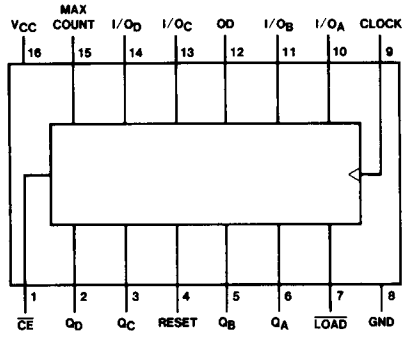
These circuits are synchronous, edge-sensitive, fully-programmable 4-bit counters. The counters feature both conventional totem-pole and TRI-STATE outputs; such that when the outputs are in the high impedance mode, they can be used to enter data from the bus lines. In addition, the clear input operates completely independent of all other inputs. During the programming operation, data is loaded into the flip-flops on the positive-going edge of the clock pulse. To facilitate cascading of these counters, the MAX COUNT output can be tied directly into the count enable input of the next counter.

Features

- Typical clock frequency 35 MHz
- TRI-STATE outputs
- Fully independent clear
- Synchronous loading
- Cascading circuitry provided internally

Connection Diagram

Dual-In-Line Package



TL/F/6588–1

Order Number DM7556J or DM8556N
See NS Package Number J16A or N16A

Function Table

Control Inputs					I/O Ports				Active Outputs			
$\overline{LOAD}$	$\overline{CE}$	CLK	OD	Reset	I/O_A	I/O_B	I/O_C	I/O_D	Q_A	Q_B	Q_C	Q_D
H	X	X	L	H	L	L	L	L	L	L	L	L
H	X	X	H	H	Z	Z	Z	Z	L	L	L	L
H	X	L	L	L	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	X	L	H	L	Z	Z	Z	Z	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	↑	L	L	a	b	c	d	A	B	C	D
H	L	↑	L	L		COUNT				COUNT		
H	L	↑	H	L	Z	Z	Z	Z		COUNT		

The I/O pins are used as inputs when they are TRI-STATED, and the $\overline{LOAD}$ input is Low. They are outputs and active when $\overline{LOAD}$ input is High and OD is Low.

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care including transitions

a, b, c, d = The level of the steady state input at inputs A, B, C, D respectively

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, Q_D respectively, before the indicated steady state input conditions were established.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM75	−55°C to +125°C
DM85	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM7556			DM8556			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−5.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
t_W	Pulse Width (Note 1)	Clock	25			25			ns
		Clear	20			20			
		Load	30			30			
$t_{\overline{CE}}$	Count Enable Time (Note 1)	Setup	30			30			ns
		Hold	−10			−10			
$t_{SETUP(1)}$	Setup Time High Logic Level (Note 1)	Data	25			25			ns
		Load	30			30			
$t_{HOLD(1)}$	Hold Time High Logic Level (Note 1)	Data	5			5			ns
		Load	−10			−10			
$t_{SETUP(0)}$	Setup Time Low Logic Level (Note 1)	Data	30			30			ns
		Load	25			25			
$t_{HOLD(0)}$	Hold Time Low Logic Level (Note 1)	Data	5			5			ns
		Load	−10			−10			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−25		−70	mA
			DM85	−25		−70	
I_{CC}	Supply Current	V_{CC} = Max			75	100	mA

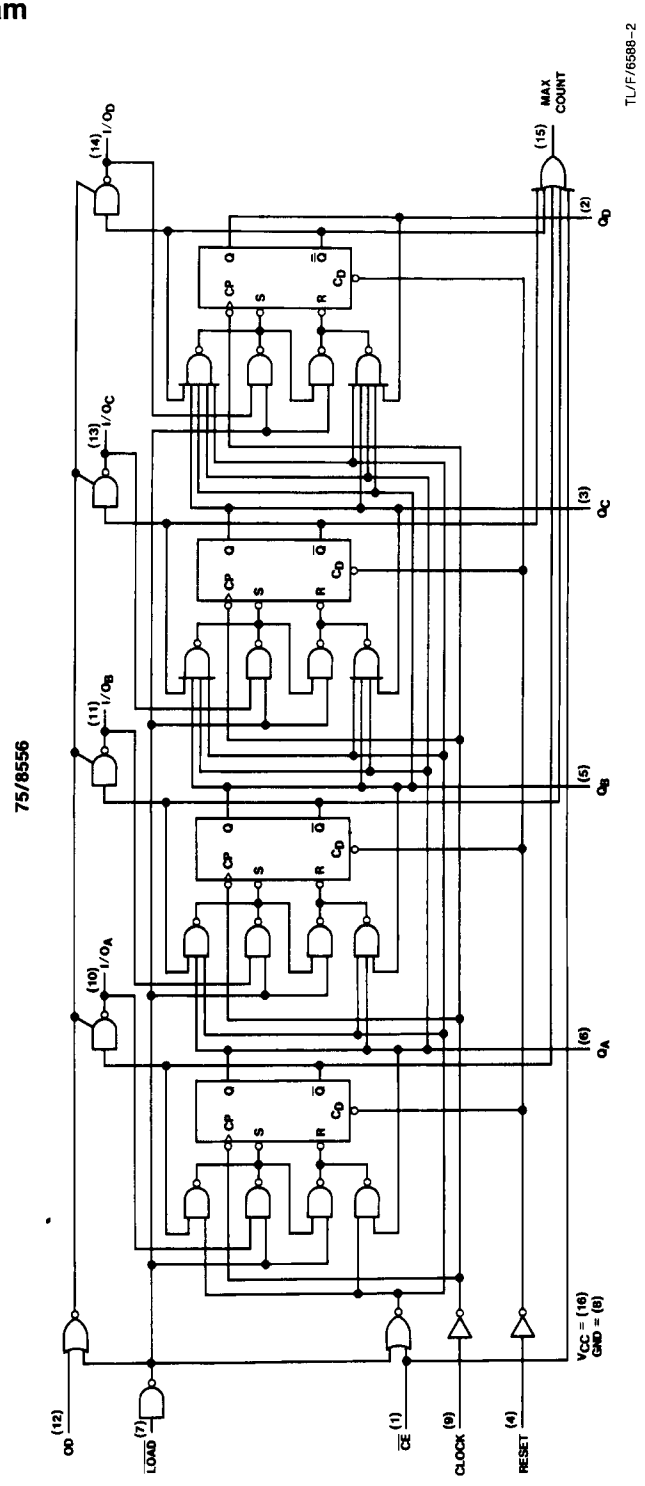
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

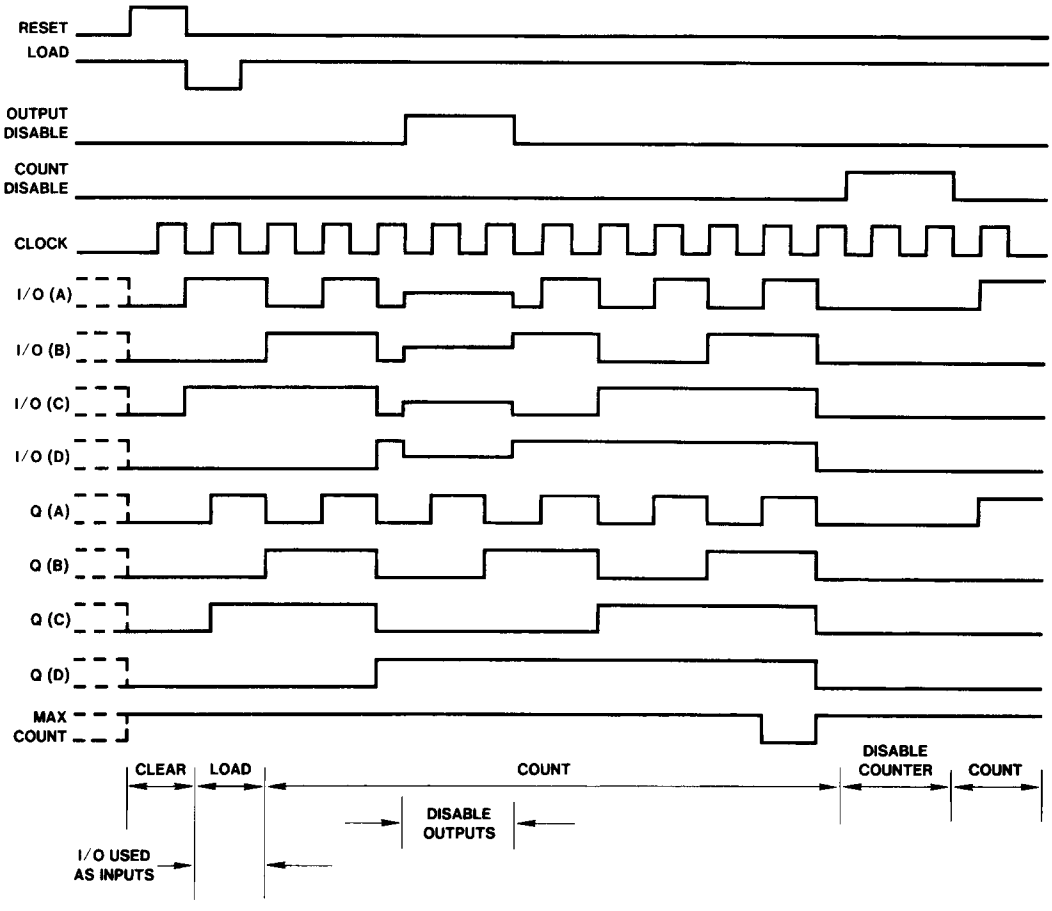
Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω				Units
			C_L = 5 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency				25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output				22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output				44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to MAX-CNT				33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to MAX-CNT				33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Reset to Output				44	ns
t_{PZH}	Output Enable Time to High Level Output	Output Disable to Q				20	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Disable to Q				20	ns
t_{PHZ}	Output Disable Time from High Level Output	Output Disable to Q		12			ns
t_{PLZ}	Output Disable Time from Low Level Output	Output Disable to Q		20			ns

Logic Diagram



Timing Diagram

75/8556 Typical Clear, Preset, Count, Inhibit Sequence



TL/F/6588–3

Sequence

(1) Clear to zero.

(2) Load binary five.

(3) Count six, seven, eight, nine, ten, eleven, twelve, thirteen, fourteen, fifteen, zero.

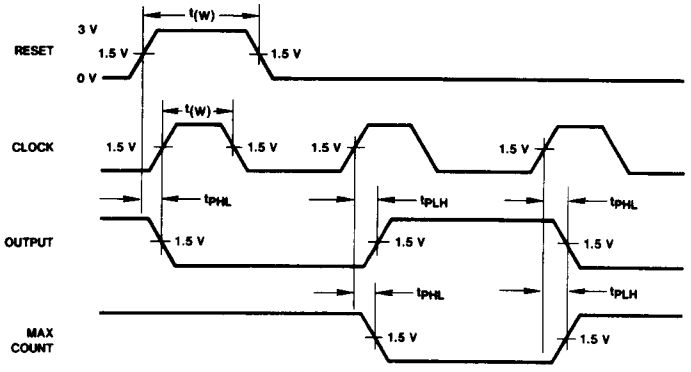
(4) Disable TRI-STATE outputs.

(5) Disable counter.

(6) Count to one.

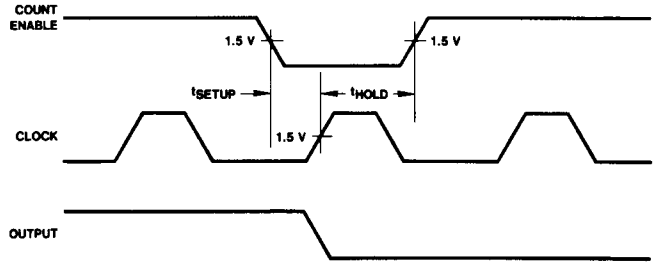
Switching Time Waveforms

Clock and Reset Voltage



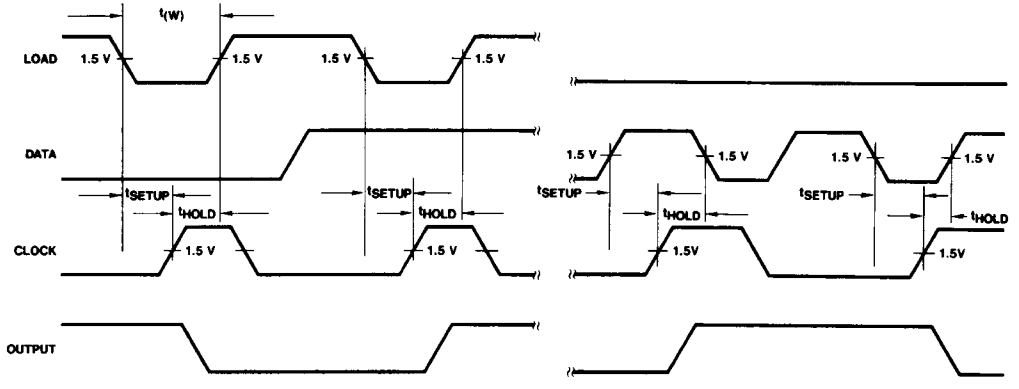
TL/F/6588–4

Count Enable and Clock



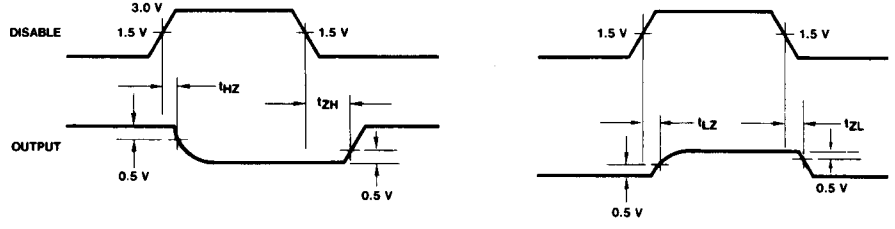
TL/F/6588–5

Load, Data and Clock



TL/F/6588–6

Output Disable



TL/F/6588–7