D2825, DECEMBER 1983

- **Similar to 'AS574 and 'AS576 with Clock Enable, Clear, and Multiple Output Controls**
- **Improved I_{OH} Specifications**
- **Multiple Output Enables Allow Multiuser Control of the Interface**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Buffered Control Inputs to Reduce DC Loading Effect**
- **Dependable Texas Instruments Quality and Reliability**

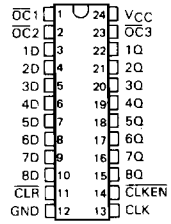
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

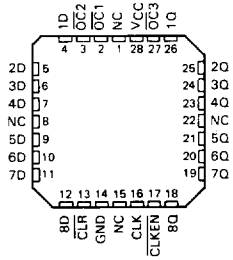
With the clock enable ($\overline{CLKEN}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS825 has noninverting D inputs and the 'AS826 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the eight Q outputs to go low independently of the clock.

A multiuser buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

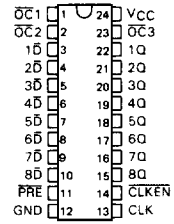
SN54AS825 . . . JT PACKAGE
SN74AS825 . . . NT PACKAGE
(TOP VIEW)



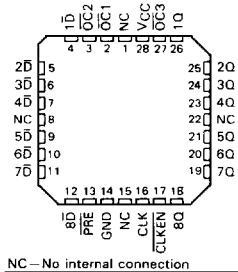
SN54AS825 . . . FH PACKAGE
SN74AS825 . . . FN PACKAGE
(TOP VIEW)



SN54AS826 . . . JT PACKAGE
SN74AS826 . . . NT PACKAGE
(TOP VIEW)



SN54AS826 . . . FH PACKAGE
SN74AS826 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

The output controls ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS825 and SN54AS826 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS825 and SN74AS826 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'AS825

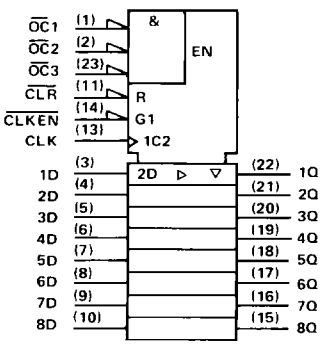
INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS826

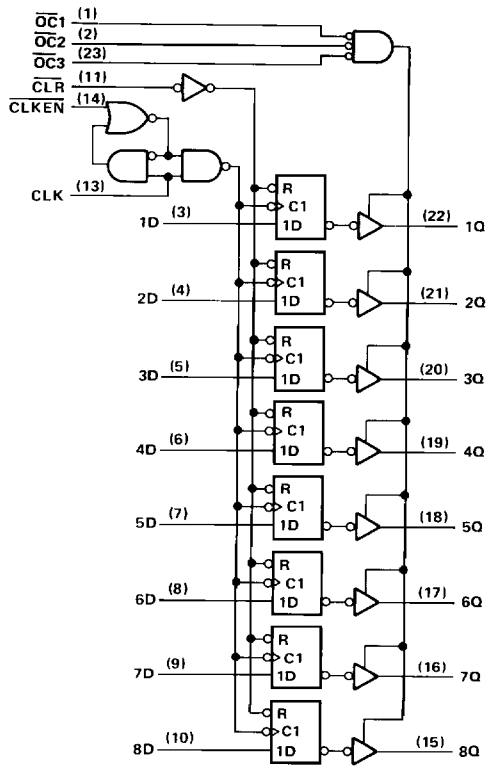
INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$\overline{OC}^* = \overline{OC}1 \cdot \overline{OC}2 \cdot \overline{OC}3$

'AS825 logic symbol

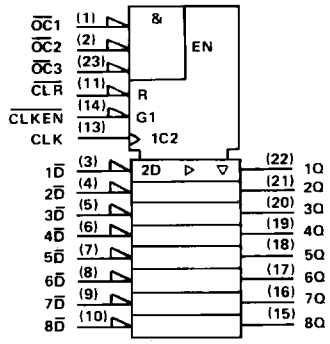


'AS825 logic diagram (positive logic)

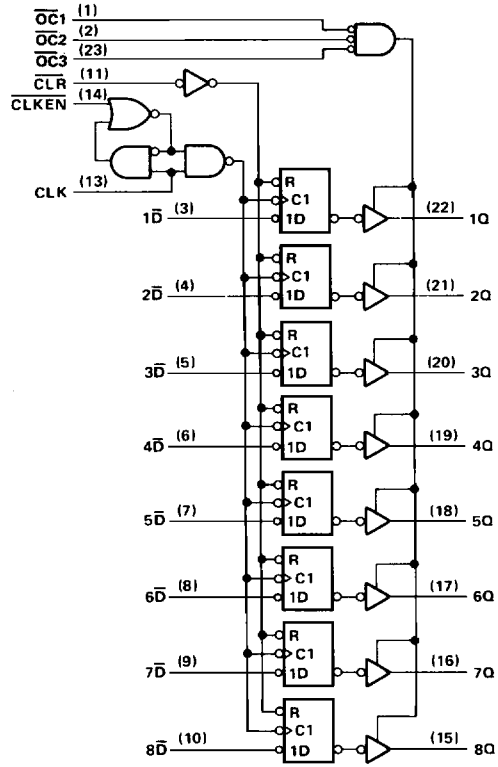


Pin numbers shown are for JT and NT packages.

'AS826 logic symbol



'AS826 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS825, SN54AS826 . . . . . −55°C to 125°C
SN74AS825, SN74AS826 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65 to 150°C

recommended operating conditions

			SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{CLR}$ low							ns
		CLK high							
		CLK low							
		$\overline{CLKEN}$							
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive							ns
		Data							
		$\overline{CLKEN}$							
t_h	Hold time, data after CLK↑								ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.25	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V							mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V							μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V							mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS825	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		58			58		
	'AS826	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		58			58		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS825 SN54AS826			SN74AS825 SN74AS826			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CLK	Any Q		7.5			7.5		ns
t_{PHL}				9.5			9.5		
t_{PHL}	$\overline{CLR}$	Any Q		11			11		ns
t_{PZH}	$\overline{OC}$	Any Q		6			6		ns
t_{PZL}				7			7		
t_{PHZ}	$\overline{OC}$	Any Q		6			6		ns
t_{PLZ}				7			7		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit $\overline{D}$ and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and $\overline{Q}$. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.