



# PROGRAMMABLE FLEXP CLOCK FOR P4 PROCESSOR

IDTCV152

## FEATURES:

- One high precision PLL for CPU, SSC, and N programming
- One high precision PLL for SRC/PCI, SSC, and N programming
- One high precision PLL for 48MHz
- Band-gap circuit for differential outputs
- Support spread spectrum modulation, down spread 0.5% and others
- Support SMBus block read/write, index read/write
- Selectable output strength for REF, 48MHz, PCI
- Allows for CPU frequency to change to a higher frequency for maximum system computing power
- Available in SSOP and TSSOP packages

## OUTPUTS:

- 5\*0.7V current –mode differential CPU CLK pair
- 4\*0.7V current –mode differential SRC CLK pair
- 7\*PCI, 3 free running, 33.3MHz
- 1\*48MHz
- 2\*REF

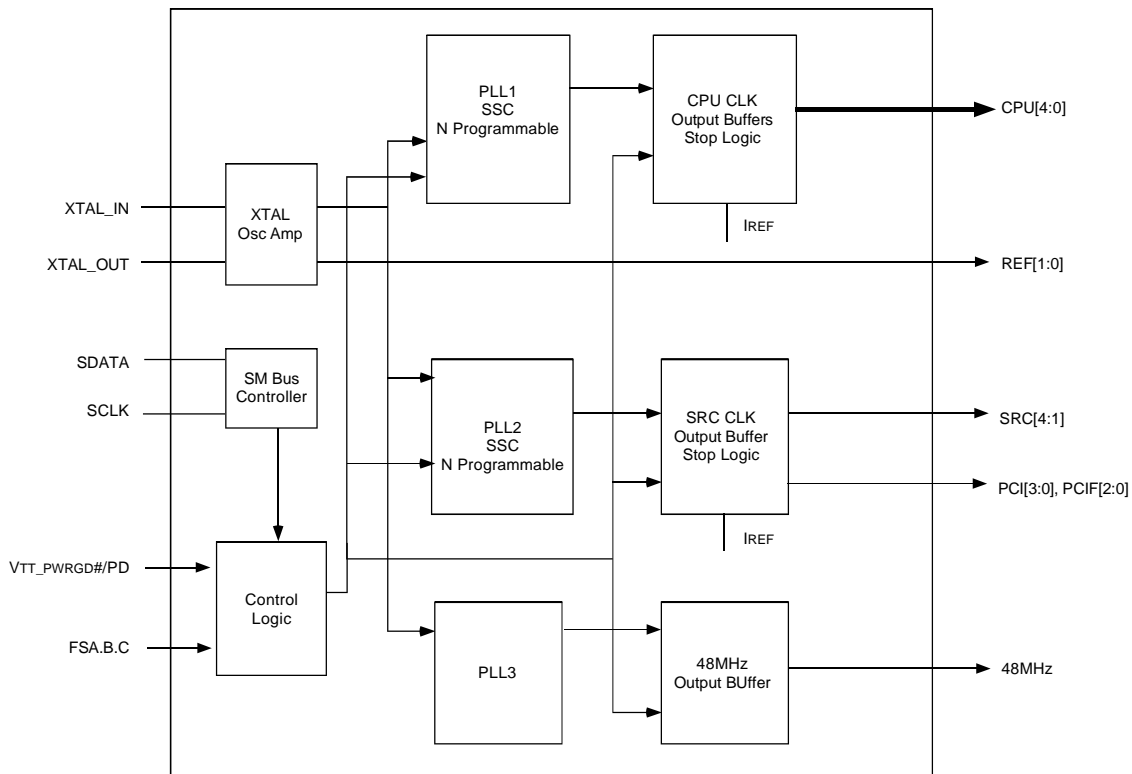
## DESCRIPTION:

IDTCV152 is a 56 pin clock device, compliant with Intel CK410B specification. The CPU output buffer is designed to support up to 400MHz processor. This chip has three PLLs inside for CPU, SRC/PCI, and 48MHz IO clocks. This device also implements Band-gap referenced IREF to reduce the impact of V<sub>DD</sub> variation on differential outputs, which can provide more robust system performance. Each CPU and SRC/PCI has its own Spread Spectrum selection, which allows for isolated changes instead of affecting other clock groups.

## KEY SPECIFICATION:

- CPU CLK cycle to cycle jitter < 85ps
- SRC CLK cycle to cycle jitter < 100ps
- PCI CLK cycle to cycle jitter < 250ps

## FUNCTIONAL BLOCK DIAGRAM

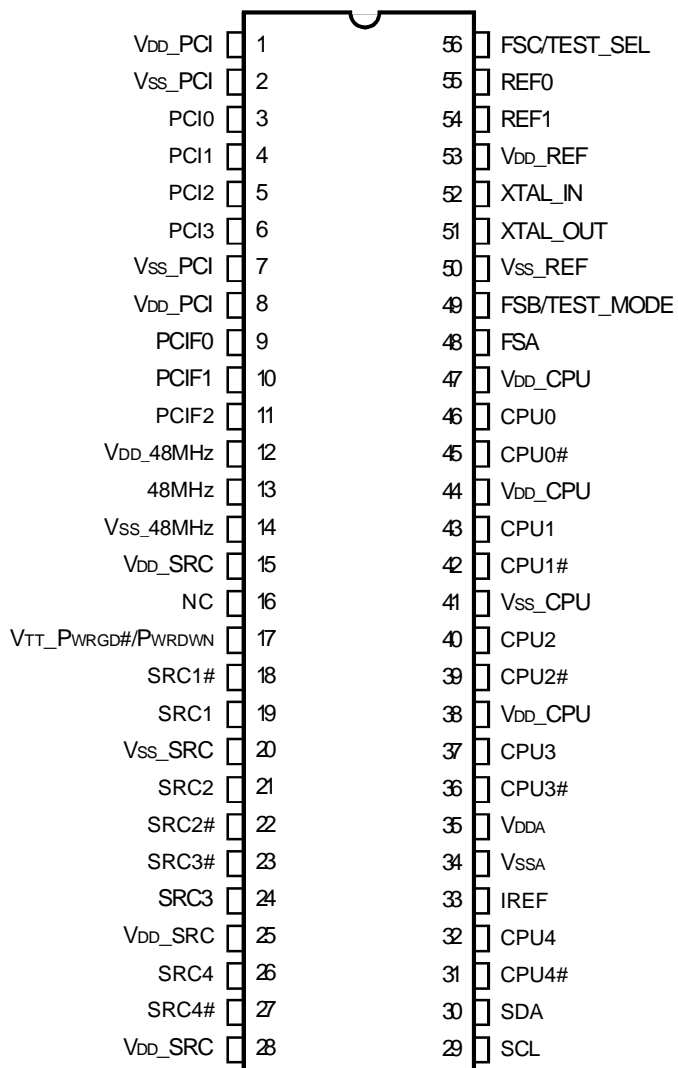


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**COMMERCIAL TEMPERATURE RANGE**

**MAY 2005**

## PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
VDDA	3.3V Core Supply Voltage		4.6	V
VDD	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
TSTG	Storage Temperature	-65	+150	°C
TAMBIENT	Ambient Operating Temperature	0	+70	°C
TCASE	Case Temperature		+115	°C
ESD Prot	Input ESD Protection Human Body Model	2000		V

### NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CPU AND SRC SPREAD SPECTRUM MAGNITUDE CONTROL

SMC[2:0]	%
000	-0.25
001	-0.5
010	-0.75
011	-1
100	±0.125
101	±0.25
110	±0.375
111	±0.5

## FREQUENCY SELECTION TABLE

FSC, B, A	CPU	SRC	PCI	USB	REF
101	100	100	33.3	48	14.318
001	133	100	33.3	48	14.318
011	166	100	33.3	48	14.318
010	200	100	33.3	48	14.318
000	266	100	33.3	48	14.318
100	333	100	33.3	48	14.318
110	400	100	33.3	48	14.318
111	Reserve	100	33.3	48	14.318

## PIN DESCRIPTION

Pin Name	Type	Pin #	Description
XTAL_IN	I	52	14.318XTALinput
XTAL_OUT	O	51	14.318XTALoutput
REF[1:0]	O	54, 55	14.318 MHz
PCI[3:0]	O	3, 4, 5, 6	33.33MHz PCI CLK
PCIF[2:0]	O	9, 10, 11	33.33MHz PCI free running CLK
USB48	O	13	48MHz
CPU[4:0], CPU#[4:0]	O	31, 32, 36, 37, 39, 40, 42, 43, 45, 46	CPU differential CLK
SRC[4:1], SRC#[4:1]	O	18, 19, 21-24, 26, 27	SRC differential clk
FSB/TEST_MODE	I	49	Frequency select. When in test mode, 0 = CLK Hi-Z, 1 = CLK REF/N
FSC/TEST_SEL	I	56	Frequency select. Select test mode if pulled to 2V and above when V <sub>TT_PWRGND#</sub> assertion.
FSA	I	48	Frequency select, sampled on V <sub>TT_PWRGND#</sub> assertion
IREF	I	33	Reference current for differential outputs
V <sub>TT_PWRGND#</sub> /PD	I	17	3.3V LVTTTL input, a level-sensitive strobe used to latch the FSA, FSB, FSC/TEST_SEL inputs. After V <sub>TT_PWRGND#</sub> assertion, becomes a real-time input for asserting power down (active HIGH).
SDA	I/O	30	SMBus data
SCL	I	29	SMBus clock

## RESOLUTION

CPU (MHz)	Resolution	N =
100	0.666667	150
133	0.666667	200
166	1.333333	125
200	1.333333	150
266	1.333333	200
333	2.666667	125
400	2.666667	150

## SE SIGNAL STRENGTH SELECTION

Str[1:0]	Strength
00	0.6x
01	0.8x
10	1x
11	1.2x

## INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N (0 is not valid)
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

## INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	D3h
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes), power on is 8
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

## INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

## INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

### BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	CPU[T/C]4	Output Enable	Tristate	Enable	RW	1
1	SRCT1, SRCC1	Output Enable	Tristate	Enable	RW	1
2	SRCT2, SRCC2	Output Enable	Tristate	Enable	RW	1
3	SRCT3, SRCC3	Output Enable	Tristate	Enable	RW	1
4	SRCT4, SRCC4	Output Enable	Tristate	Enable	RW	1
5	Reserved					1
6	Reserved					1
7	Reserved					1

### BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	Spread Spectrum Enable	Spread Spectrum mode Enable	Spread off	Spread on	RW	0
1	CPUT0, CPUC0	Output Enable	Tristate	Enable	RW	1
2	CPUT1, CPUC1	Output Enable	Tristate	Enable	RW	1
3	Reserved					1
4	CPUT2, CPUC2	Output Enable	Tristate	Enable	RW	1
5	CPUT3, CPUC3	Output Enable	Tristate	Enable	RW	1
6	REF0	Output Enable	Tristate	Enable	RW	1
7	REF1	Output Enable	Tristate	Enable	RW	1

### BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
0	USB_48	Output Enable	Disable	Enable	RW	1
1	PCIF0	Output Enable	Disable	Enable	RW	1
2	PCIF1	Output Enable	Disable	Enable	RW	1
3	PCIF2	Output Enable	Disable	Enable	RW	1
4	PCI0	Output Enable	Disable	Enable	RW	1
5	PCI1	Output Enable	Disable	Enable	RW	1
6	PCI2	Output Enable	Disable	Enable	RW	1
7	PCI3	Output Enable	Disable	Enable	RW	1

### BYTE 3

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPUCLK4	Allow controlled by SRC_STOP/CPU_Stop# assertion	Freerunning	Stoppable	RW	0
1	SRCT1, SRCC1	Allow controlled by PCI_STOP# assertion	Free running, not affected by PCI_STOP#	Stopped with PCI_STOP#	RW	0
2	SRCT2, SRCC2				RW	0
3	SRCT3, SRCC3				RW	0
4	SRCT4, SRCC4				RW	0
5	PCIF0				RW	0
6	PCIF1				RW	0
7	PCIF2				RW	0

## BYTE 4

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPUCLK0 Stop EN	Free-running control, Default: not affected by CPU_STOP	Free-running	Stoppable	RW	1
1	CPUCLK1 Stop EN				RW	1
2	CPUCLK2 Stop EN				RW	1
3	CPUCLK3 Stop EN				RW	1
4	CPUT0, CPUC0	CPU0 Pwrdown drive mode	Driven in power down	Tristate in power down	RW	0
5	CPUT1, CPUC1	CPU1 Pwrdown drive mode			RW	0
6	CPUT2, CPUC2	CPU2 Pwrdown drive mode			RW	0
7	CPUT3, CPUC3	CPU3 Pwrdown drive mode			RW	0

## BYTE 5

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPUCLK0	Stop Drive - Drive mode in Stop	Driven	Tri-state	RW	0
1	CPUCLK1				RW	0
2	CPUCLK2				RW	0
3	CPUCLK3				RW	0
4	CPUCLK4				RW	0
5	SRC	SRC Pwrdown drive mode	Driven in power down	Tristate in power down	RW	0
6	SRC	PCI_STOP drive mode	Driven in PCI_Stop	Tristate in power down	RW	0
7	CPUCLK4	CPU1 Pwrdown drive mode	Driven in power down	Tristate in power down	RW	0

## BYTE 6

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0		FSA latched value on power up			R	FSA
1		FSB latched value on power up			R	FSB
2		FSC latched value on power up			R	FSC
3	Software PCI_STOP function		Stop all PCI/F & SRC except PCIF[2:0] and SRC clocks set to free running	No stop	RW	1
4	REFstr1	REF drive strength , work with byte12 bit2, see strength table			RW	1
5	CPU	CPU_Stop control	Stop non-free running CPU clocks	Run	RW	1
6		Test Mode entry control	Normal operation	Test mode, controlled by byte 6 bit 7	RW	0
7		Only valid when Byte6 bit6 is HIGH	Hi-Z	REF/N mode	RW	0

### BYTE 7

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0		Vendor ID			R	1
1		Vendor ID			R	0
2		Vendor ID			R	1
3		Vendor ID			R	0
4		Revision ID			R	0
5		Revision ID			R	0
6		Revision ID			R	0
7		Revision ID			R	0

### BYTE 8 (BLOCK READ BYTE COUNT)

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0						0
1						1
2						1
3						1
4						0
5						0
6						0
7						0

### BYTE 9

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC SMC0	SSC control (see SMC table)			RW	1
1	SRC SMC1				RW	0
2	SRC SMC2				RW	0
3	Reserved				RW	0
4	CPU SMC0	SSC control (see SMC table)			RW	1
5	CPU SMC1				RW	0
6	CPU SMC2				RW	0
7	Reserved				RW	0

### BYTE 10

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	CPU_N0, LSB	CPU CLK = N* Resolution			RW	0
1	CPU_N1				RW	1
2	CPU_N2				RW	1
3	CPU_N3				RW	0
4	CPU_N4				RW	1
5	CPU_N5				RW	0
6	CPU_N6				RW	0
7	CPU_N7, MSB				RW	1

### BYTE 11

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	SRC_N0, LSB	CPU CLK = N* Resolution			RW	0
1	SRC_N1				RW	1
2	SRC_N2				RW	1
3	SRC_N3				RW	0
4	SRC_N4				RW	1
5	SRC_N5				RW	0
6	SRC_N6				RW	0
7	SRC_N7, MSB				RW	1

### BYTE 12

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	48MHzStr0				RW	1
1	48MHStr1	USB48MHz strength selection			RW	1
2	REFStr0	Work with Byte 6 Bit 4 REFstr1 (see strength table)			RW	1
3	Reserved				RW	0
4	PCIStrC0				RW	0
5	PCIStrC1	PCI strength selection			RW	1
6	PCIFStr0				RW	0
7	PCIFStr1	PCIF strength selection			RW	1

### BYTE 13

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
0	Test_scl	On chip test mode enable	Normal	SCLK=1, CLK outputs=1 SCLK=0, CLK outputs=0	RW	0
1		N Programming enable	Disable	enable	RW	0
2	Reserved				RW	0
3	Reserved				RW	0
4		USB PLL power down	Normal	Power down	RW	0
5		SRC PLL power down	Normal	Power down	RW	0
6		CPU PLL power down	Normal	Power down	RW	0
7	Reserved				RW	0

### BYTE 62 DEVICE ID + REV

**BIT[7:4] = 2h**

**BIT[3:0] = 0h**

### BYTE 63 = DEVICE ID

**BIT[7:4] = 1h**

**BIT[3:0] = 5h**



## ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = 0°C to +70°C, Supply Voltage: VDD = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	3.3V ± 5%	2	—	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage	3.3V ± 5%	V <sub>SS</sub> - 0.3	—	0.8	V
V <sub>IH_FS</sub>	LOW Voltage, HIGH Threshold	For FSA.B.C test_mode	0.7	—	V <sub>DD</sub> + 0.3	V
V <sub>IL_FS</sub>	LOW Voltage, LOW Threshold	For FSA.B.C test_mode	V <sub>SS</sub> - 0.3	—	0.35	V
I <sub>IL</sub>	Input Leakage Current	0 < V <sub>IN</sub> < V <sub>DD</sub> , no internal pull-up or pull-down	-5	—	+5	mA
I <sub>DD3.3OP</sub>	Operating Supply Current	Full active, C <sub>L</sub> = full load	—	—	400	mA
I <sub>DD3.3PD</sub>	Powerdown Current	All differential pairs driven	—	—	70	mA
		All differential pairs tri-stated	—	—	12	
F <sub>I</sub>	Input Frequency <sup>(1)</sup>	V <sub>DD</sub> = 3.3V	—	14.31818	—	MHz
L <sub>PIN</sub>	Pin Inductance <sup>(2)</sup>		—	—	7	nH
C <sub>IN</sub>	Input Capacitance <sup>(2)</sup>	Logic inputs	—	—	5	pF
C <sub>OUT</sub>		Output pin capacitance	—	—	6	
C <sub>INX</sub>		XTAL_IN and XTAL_OUT pins	—	—	5	
T <sub>STAB</sub>	Clock Stabilization <sup>(2,3)</sup>	From V <sub>DD</sub> power-up or de-assertion of PD to first clock	—	—	1.8	ms
	Modulation Frequency <sup>(2)</sup>	Triangular modulation	30	—	33	KHz
	T <sub>DRIVE_PD</sub> <sup>(2)</sup>	CPU output enable after PD de-assertion	—	—	300	us
	T <sub>FALL_PD</sub> <sup>(2)</sup>	Fall time of PD	—	—	5	ns
	T <sub>RISE_PD</sub> <sup>(2)</sup>	Rise time of PD	—	—	5	ns

### NOTES:

1. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
2. This parameter is guaranteed by design, but not 100% production tested.
3. See TIMING DIAGRAMS for timing requirements.

## ELECTRICAL CHARACTERISTICS - CPU AND SRC 0.7 CURRENT MODE DIFFERENTIAL PAIR<sup>(1)</sup>

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , Supply Voltage:  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 2\text{pF}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z <sub>O</sub>	Current Source Output Impedance <sup>(2)</sup>	$V_O = V_X$	3000	—	—	$\Omega$
V <sub>OH3</sub>	Output HIGH Voltage	$I_{OH} = -1\text{mA}$	2.4	—	—	V
V <sub>OL3</sub>	Output LOW Voltage	$I_{OL} = 1\text{mA}$	—	—	0.4	V
V <sub>HIGH</sub>	Voltage HIGH <sup>(2)</sup>	Statistical measurement on single-ended signal using oscilloscope math function	660	—	1150	mV
V <sub>LOW</sub>	Voltage LOW <sup>(2)</sup>		-300	—	150	
V <sub>OVS</sub>	Max Voltage <sup>(2)</sup>	Measurement on single-ended signal using absolute value	—	—	1150	mV
V <sub>UDS</sub>	Min Voltage <sup>(2)</sup>		-300	—	—	
V <sub>CROSS(ABS)</sub>	Crossing Voltage (abs) <sup>(2)</sup>		250	—	550	mV
d - V <sub>CROSS</sub>	Crossing Voltage (var) <sup>(2)</sup>	Variation of crossing over all edges	—	—	140	mV
ppm	Static Error <sup>(2,3)</sup>	See T <sub>PERIOD</sub> Min. - Max. values	—	—	0	ppm
T <sub>PERIOD</sub>	Average Period <sup>(3)</sup>	400MHz nominal / -0.5% spread	2.4993	—	2.5133	ns
		333.33MHz nominal / -0.5% spread	2.9991	—	3.016	
		266.66MHz nominal / -0.5% spread	3.7489	—	3.77	
		200MHz nominal / -0.5% spread	4.9985	—	5.0266	
		166.66MHz nominal / -0.5% spread	5.9982	—	6.032	
		133.33MHz nominal / -0.5% spread	7.4978	—	7.54	
		100MHz nominal / -0.5% spread	9.997	—	10.0533	
T <sub>ABSMIN</sub>	Absolute Min Period <sup>(2,3)</sup>	400MHz nominal / -0.5% spread	2.4143	—	—	ns
		333.33MHz nominal / -0.5% spread	2.9141	—	—	
		266.66MHz nominal / -0.5% spread	3.6639	—	—	
		200MHz nominal / -0.5% spread	4.9135	—	—	
		166.66MHz nominal / -0.5% spread	5.9132	—	—	
		133.33MHz nominal / -0.5% spread	7.4128	—	—	
		100MHz nominal / -0.5% spread	9.912	—	—	
t <sub>r</sub>	Rise Time <sup>(2)</sup>	$V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$	175	—	700	ps
t <sub>f</sub>	Fall Time <sup>(2)</sup>	$V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$	175	—	700	ps
d-t <sub>r</sub>	Rise Time Variation <sup>(2)</sup>		—	—	125	ps
d-t <sub>f</sub>	Fall Time Variation <sup>(2)</sup>		—	—	125	ps
dT <sub>3</sub>	Duty Cycle <sup>(2)</sup>	Measurement from differential waveform	45	—	55	%

### NOTES:

- SRC clock outputs run only at 100MHz.
- This parameter is guaranteed by design, but not 100% production tested.
- All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

## ELECTRICAL CHARACTERISTICS - CPU AND SRC 0.7 CURRENT MODE DIFFERENTIAL PAIR, CONTINUED<sup>(1)</sup>

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , Supply Voltage:  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 2\text{pF}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
tsk3	Skew, CPU <sup>(2)</sup>	$V_T = 50\%$	—	—	100	ps
	Skew, SRC <sup>(2)</sup>		—	—	250	
tjcyC-cyC	Jitter, Cycle to Cycle, CPU <sup>(2)</sup>	Measurement from differential waveform	—	—	85	ps
	Jitter, Cycle to Cycle, SRC <sup>(2)</sup>		—	—	125	

### NOTES:

1. SRC clock outputs run only at 100MHz.
2. This parameter is guaranteed by design, but not 100% production tested.

## ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK\_F

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , Supply Voltage:  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10 - 30\text{pF}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error <sup>(1,2)</sup>	See Tperiod Min. - Max. values	—	—	0	ppm
TPERIOD	Clock Period <sup>(2)</sup>	33.33MHz output nominal	29.991	—	30.009	ns
		33.33MHz output spread	29.991	—	30.1598	
VOH	Output HIGH Voltage	IOH = -1mA	2.4	—	—	V
VOL	Output LOW Voltage	IOL = 1mA	—	—	0.55	V
IOH	Output HIGH Current	VOH at Min. = 1V	-33	—	—	mA
		VOH at Max. = 3.135V	—	—	-33	
IOL	Output LOW Current	VOL at Min. = 1.95V	30	—	—	mA
		VOL at Max. = 0.4V	—	—	38	
	Edge Rate <sup>(1)</sup>	Rising edge rate	1	—	4	V/ns
	Edge Rate <sup>(1)</sup>	Falling edge rate	1	—	4	V/ns
tr1	Rise Time <sup>(1)</sup>	VOL = 0.8V, VOH = 2V	0.3	—	1.2	ns
tf1	Fall Time <sup>(1)</sup>	VOL = 0.8V, VOH = 2V	0.3	—	1.2	ns
dt1	Duty Cycle <sup>(1)</sup>	$V_T = 1.5\text{V}$	45	—	55	%
tsk1	Skew <sup>(1)</sup>	$V_T = 1.5\text{V}$	—	—	500	ps
tjcyC-cyC	Jitter, Cycle to Cycle <sup>(1)</sup>	$V_T = 1.5\text{V}$	—	—	500	ps

### NOTES:

1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

## ELECTRICAL CHARACTERISTICS, 48MHZ, USB

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , Supply Voltage:  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10 - 20\text{pF}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Static Error <sup>(1,2)</sup>	See Tperiod Min. - Max. values	—	—	0	ppm
TPERIOD	Clock Period <sup>(2)</sup>	48MHz output nominal	20.8257	—	20.834	ns
VOH	Output HIGH Voltage	IOH = -1mA	2.4	—	—	V
VOL	Output LOW Voltage	IOL = 1mA	—	—	0.55	V
IOH	Output HIGH Current	VOH at Min. = 1V	-29	—	—	mA
		VOH at Max. = 3.135V	—	—	-23	
IOL	Output LOW Current	VOL at Min. = 1.95V	29	—	—	mA
		VOL at Max. = 0.4V	—	—	27	
	Edge Rate <sup>(1)</sup>	Rising edge rate	1	—	2	V/ns
	Edge Rate <sup>(1)</sup>	Falling edge rate	1	—	2	V/ns
tR1	Rise Time <sup>(1)</sup>	VOL = 0.8V, VOH = 2V	0.5	—	1.2	ns
tF1	Fall Time <sup>(1)</sup>	VOL = 0.8V, VOH = 2V	0.5	—	1.2	ns
dT1	Duty Cycle <sup>(1)</sup>	VT = 1.5V	45	—	55	%
tCYC-CYC	Jitter, Cycle to Cycle		—	—	350	ps

### NOTES:

1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

## ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ , Supply Voltage:  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10 - 20\text{pF}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy <sup>(1)</sup>	See Tperiod Min. - Max. values	—	—	0	ppm
TPERIOD	Clock Period	14.318MHz output nominal	69.827	—	69.855	ns
VOH	Output HIGH Voltage <sup>(1)</sup>	IOH = -1mA	2.4	—	—	V
VOL	Output LOW Voltage <sup>(1)</sup>	IOL = 1mA	—	—	0.4	V
IOH	Output HIGH Current	VOH at Min. = 1V	-33	—	—	mA
		VOH at Max. = 3.135V	—	—	-33	
IOL	Output LOW Current	VOL at Min. = 1.95V	30	—	—	mA
		VOL at Max. = 0.4V	—	—	38	
	Edge Rate <sup>(1)</sup>	Rising edge rate	1	—	4	V/ns
	Edge Rate <sup>(1)</sup>	Falling edge rate	1	—	4	V/ns
tR1	Rise Time <sup>(1)</sup>	VOL = 0.8V, VOH = 2V	0.3	—	1.2	ns
tF1	Fall Time <sup>(1)</sup>	VOL = 0.8V, VOH = 2V	0.3	—	1.2	ns
dT1	Duty Cycle <sup>(1)</sup>	VT = 1.5V	45	—	55	%
tCYC-CYC	Jitter, Cycle to Cycle <sup>(1)</sup>	VT = 1.5V	—	—	1000	ps

### NOTE:

1. This parameter is guaranteed by design, but not 100% production tested.

## PCI STOP FUNCTIONALITY

If PCIF (2:0) and SRC clocks are set to be free-running through SMBus programming, they will ignore the PCI\_STOP register bit.

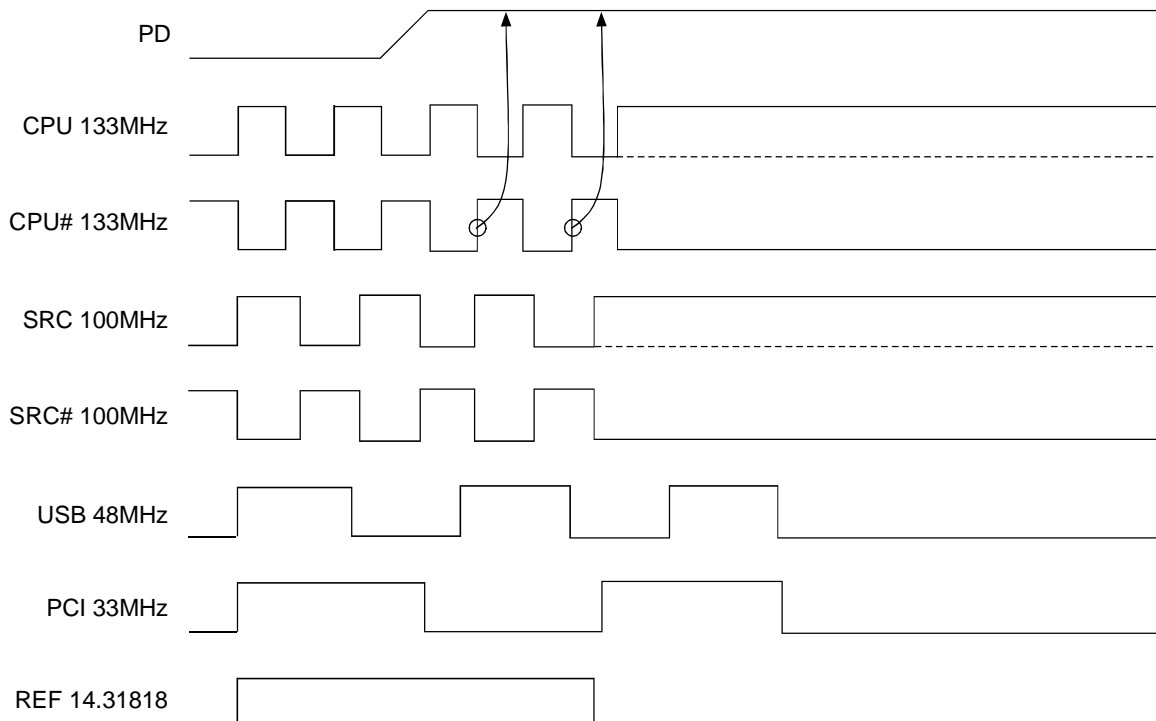
PCI_STOP (Byte 6 bit 3)	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	DOT96	DOT96#	REF
1	Normal	Normal	Normal	Normal	33MHz	48MHz	Normal	Normal	14.318MHz
0	Normal	Normal	IREF * 6 or float	Low	Low	48MHz	Normal	Normal	14.318MHz

## PD, POWER DOWN

PD is an asynchronous active high input used to shut off all clocks cleanly prior to clock power. When PD is asserted high all clocks will be driven low before turning off the VCO. In PD de-assertion all clocks will start without glitches.

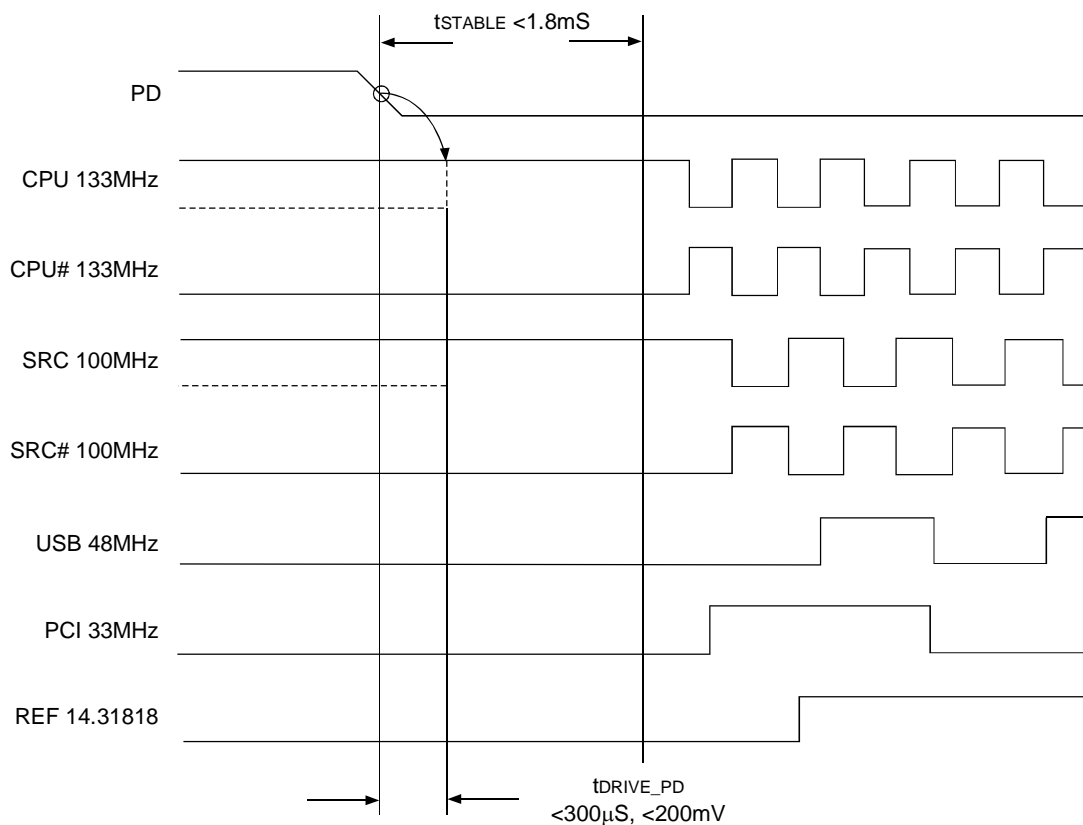
PD	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	REF
0	Normal	Normal	Normal	Normal	33MHz	48MHz	14.318MHz
1	IREF * 2 or float	Float	IREF * 2 or float	Float	Low	Low	Low

## PD ASSERTION

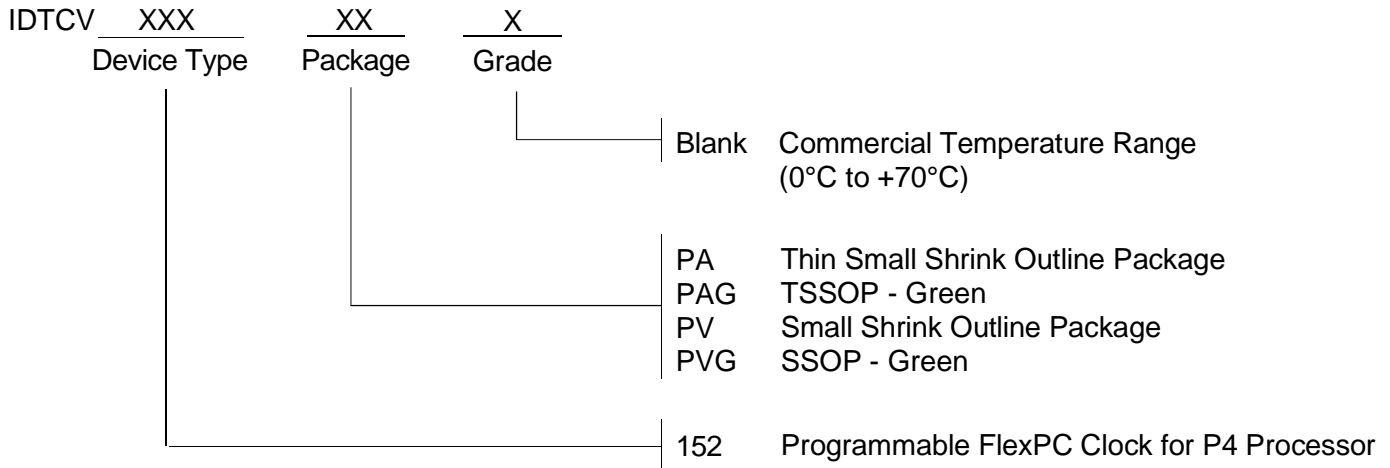


## PD DE-ASSERTION

The time from the de-assertion of PD or until power supply ramps to get stable clocks will be less than 1.8ms. If the drive mode control bit for PD tristate is programmed to '1' the stopped differential pair must first be driven high to a minimum of 200mV in less than 300µs of PD deassertion.



## ORDERING INFORMATION



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