

512Kx8 MONOLITHIC SRAM, SMD 5962-95613

FEATURES

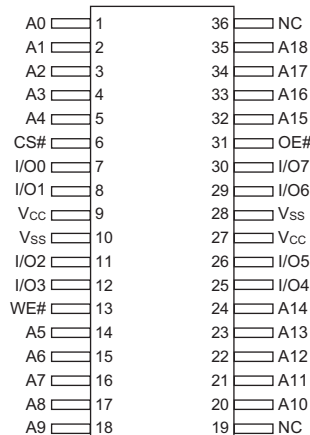
- Access Times 15, 17, 20, 25, 35, 45, 55ns
- MIL-STD-883 Compliant Devices Available
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
 - 36 lead Ceramic SOJ (Package 100)
 - 36 lead Ceramic Flat Pack (Package 226)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
 - 32 pin Ceramic DIP (Package 300)
 - 32 lead Ceramic SOJ (Package 101)
 - 32 lead Ceramic Thinpack™ Flat Pack (Package 321)
- 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
- Commercial, Industrial and Military Temperature Range
- 5V Power Supply
- Low Power CMOS
- Low Power Data Retention for Battery Back-up Operation
- TTL Compatible Inputs and Outputs

*This product is subject to change without notice.

REVOLUTIONARY PINOUT

36 FLAT PACK
36 CSOJ

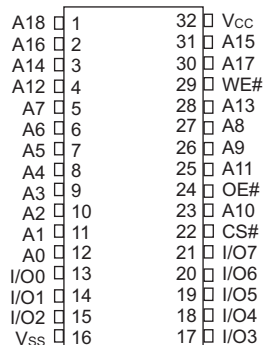
TOP VIEW



EVOLUTIONARY PINOUT

32 DIP
32 CSOJ (DE)
32 FLAT PACK (FF)

TOP VIEW

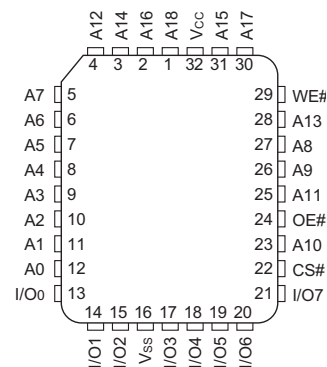


PIN DESCRIPTION

A0-18	Address Inputs
I/O 0-7	Data Input/Output
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
Vcc	+5.0V Power
GND	Ground

32 CLCC

TOP VIEW



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature Range	T_{STG}	-65	+150	°C
Signal Voltage Range to GND	V_G	-0.5	$V_{CC}+0.5$	V
Junction Temperature	T_J		150	°C
Supply Voltage Range (V_{CC})	V_{CC}	-0.5	7.0	V

Truth Table

CS#	OE#	WE#	MODE	DATA I/O	POWER
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil)	T_A	-55	+125	°C

Capacitance
 $(T_A = +25^\circ\text{C})$

Parameter	Symbol	Conditions	Package	Speed (ns)	Max	Unit
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}, f = 1.0\text{ MHz}$	32 pin CSOJ, DIP, Flat Pack Evolutionary	15 to 55	20	pF
			32 pin CLCC	15 to 55	15	pF
			36 pin CSOJ & Flat Pack Revolutionary	15 to 35	12	pF
				45 to 55	20	pF
Output capacitance	C_{OUT}	$V_{OUT} = 0\text{ V}, f = 1.0\text{ MHz}$	32 pin CSOJ, DIP, Flat Pack Revolutionary	15 to 55	20	pF
			36 pin CSOJ & Flat Pack Revolutionary	15 to 35	12	pF
				45 to 55	20	pF
					20	pF

This parameter is guaranteed by design but not tested.

DC Characteristics – CMOS Compatible
 $(V_{CC} = 5.0\text{V}, GND = 0\text{V}, -55^\circ\text{C} \leq T_A \leq 125^\circ\text{C})$

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{CC} = 5.5, V_{IN} = GND \text{ to } V_{CC}$		10	μA
Output Leakage Current	I_{LO}	$CS\# = V_{IH}, OE\# = V_{IH}, V_{OUT} = GND \text{ to } V_{CC}$		10	μA
Operating Supply Current*	I_{CC}	$CS\# = V_{IL}, OE\# = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5,$		160	mA
Standby Current	I_{SS}	$CS\# = V_{IH}, OE\# = V_{IH}, f = 5\text{MHz}, V_{CC} = 5.5$		0.45	mA
Output Low Voltage	V_{OL}	$I_{OL} = 6\text{mA}$ for 17 - 35ns, $I_{OL} = 2.1\text{mA}$ for 45 - 55ns, $V_{CC} = 4.5$		0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4.0\text{mA}$ for 17 - 35ns, $I_{OH} = 1.0\text{mA}$ for 45 - 55ns, $V_{CC} = 4.5$	2.4		V

Data retention characteristics for low power "I" version

Parameter	Symbol	Conditions	Min	Max	Unit
Data Retention Supply Voltage	V_{DR}	$CS\# V_{CC} - 0.2\text{V}$	2.0	5.5	V
Low Power Data Retention	I_{CCDR1}	$V_{CC} = 3\text{V}$		7	mA
Low Power Data Retention	I_{CCDR2}	$V_{CC} = 2\text{V}$		2	mA

AC Characteristics

 (V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C)

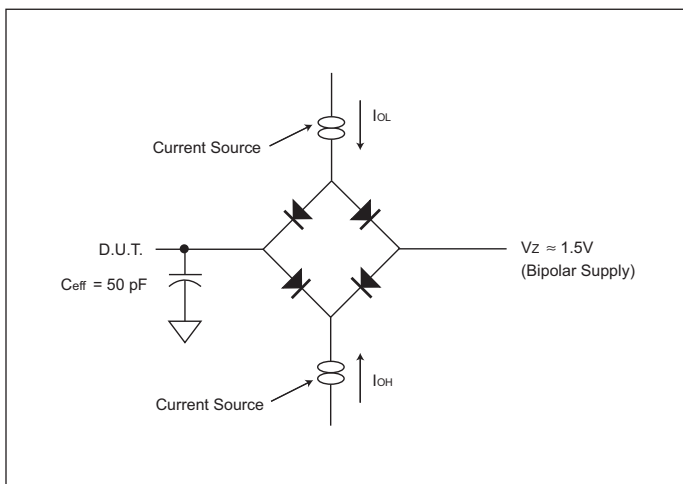
Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	15		17		20		25		35		45		55		ns
Address Access Time	t _{AA}		15		17		20		25		35		45		55	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		0		0		ns
Chip Select Access Time	t _{ACS}		15		17		20		25		35		45		55	ns
Output Enable to Output Valid	t _{OE}		8		9		10		12		25		25		25	ns
Chip Select to Output in Low Z	t _{CLZ1}	2		2		2		2		4		4		4		ns
Output Enable to Output in Low Z	t _{OLZ1}	0		0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ1}		8		9		10		12		15		20		20	ns
Output Disable to Output in High Z	t _{OHZ1}		8		9		10		12		15		20		20	ns

AC Characteristics

 (V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	15		17		20		25		35		45		55		ns
Chip Select to End of Write	t _{CW}	13		14		14		15		25		35		50		ns
Address Valid to End of Write	t _{AW}	13		14		14		15		25		35		50		ns
Data Valid to End of Write	t _{DW}	8		9		10		10		20		25		25		ns
Write Pulse Width	t _{WP}	13		14		14		15		25		35		40		ns
Address Setup Time	t _{AS}	2		2		2		2		2		2		2		ns
Address Hold Time	t _{AH}	0		0		0		0		0		5		5		ns
Output Active from End of Write	t _{OW1}	2		2		3		4		4		5		5		ns
Write Enable to Output in High Z	t _{WHZ1}		8		9		9		10		15		20		25	ns
Data Hold Time	t _{DH}	0		0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC Test Circuit

AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

 V_Z is programmable from -2V to +7V.

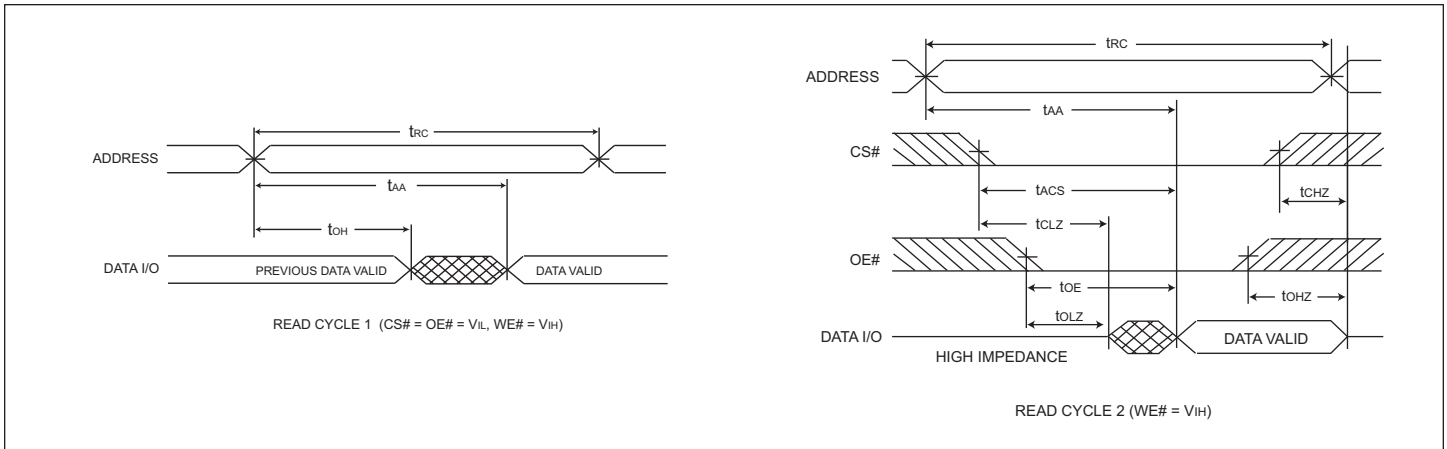
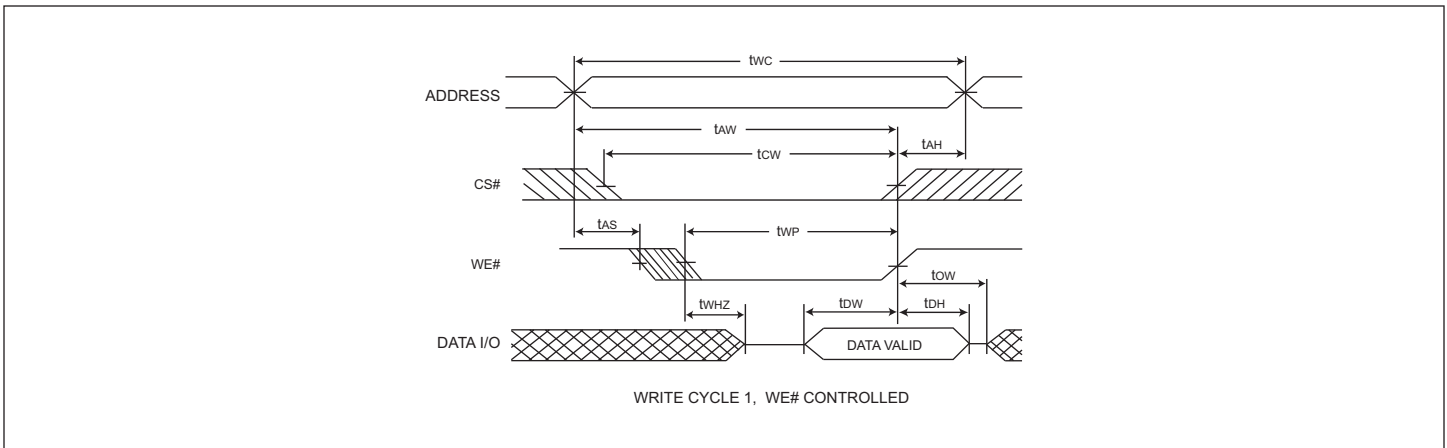
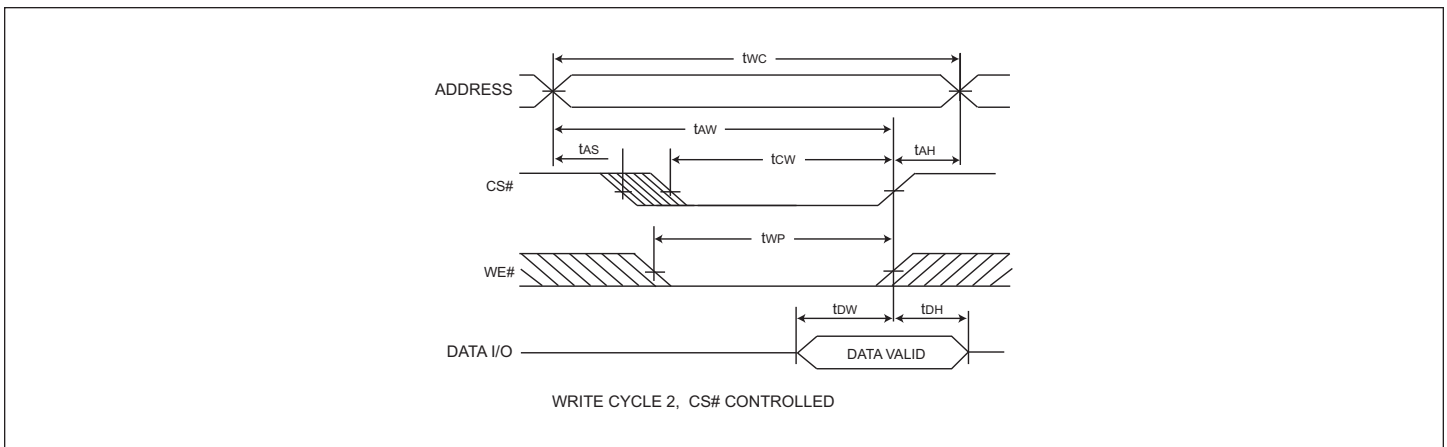
 I_{OL} & I_{OH} programmable from 0 to 16mA.

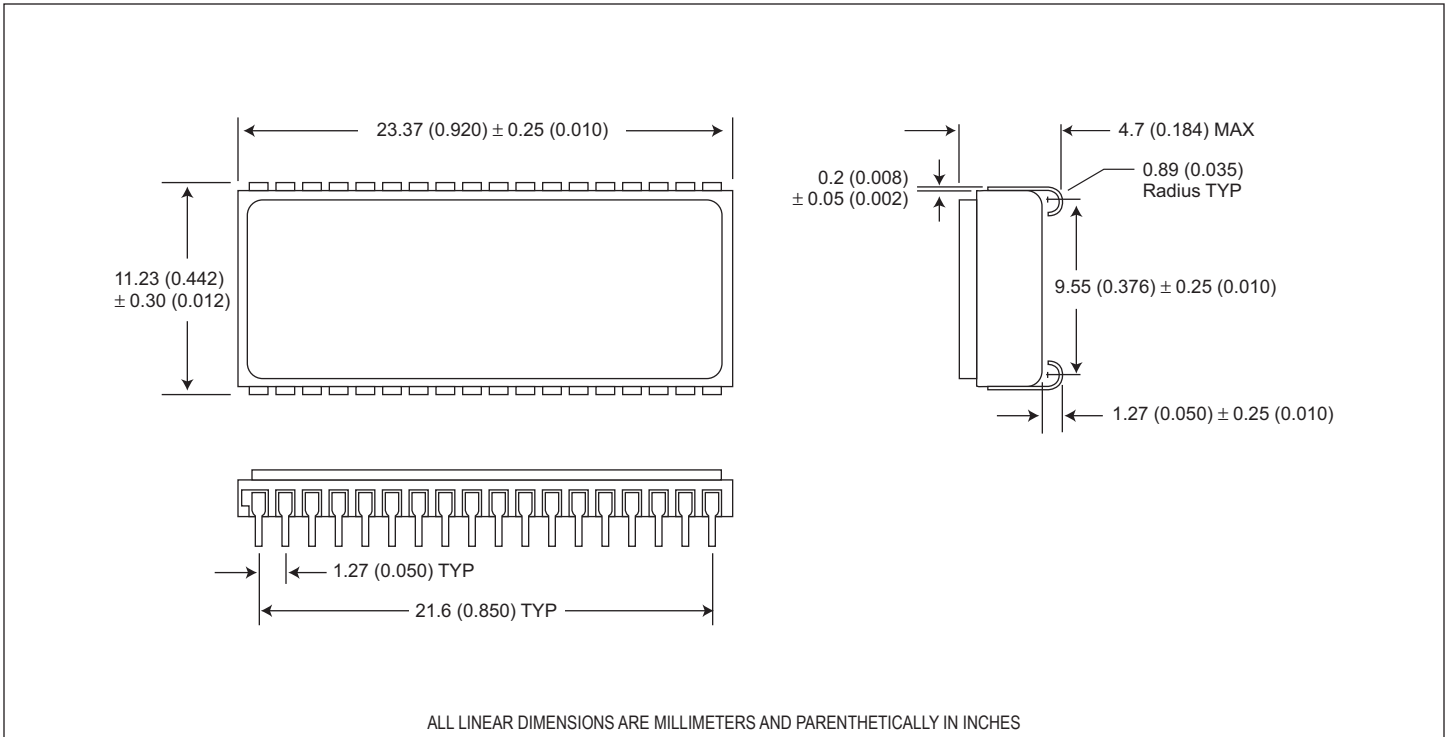
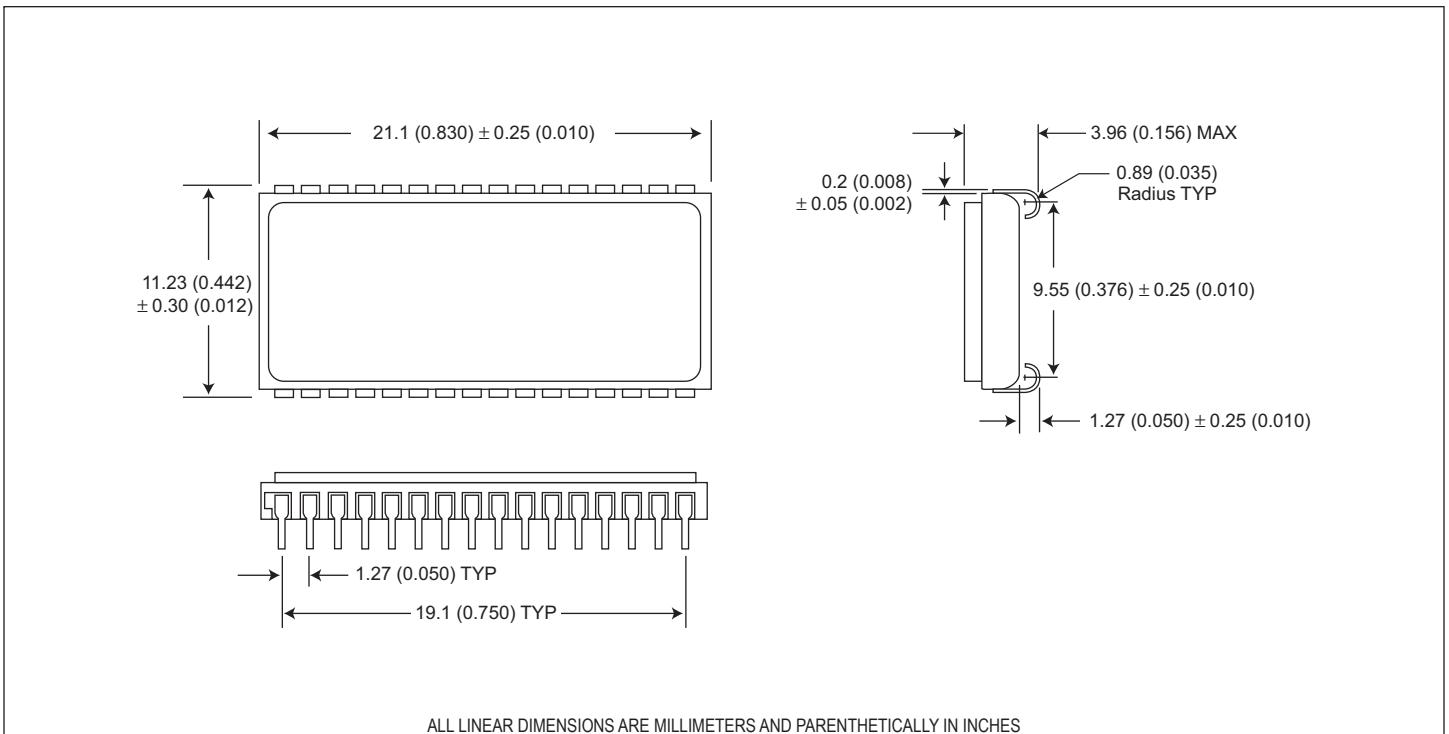
 Tester Impedance Z₀ = 75 Ω.

 V_Z is typically the midpoint of V_{OH} and V_{OL}.

 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

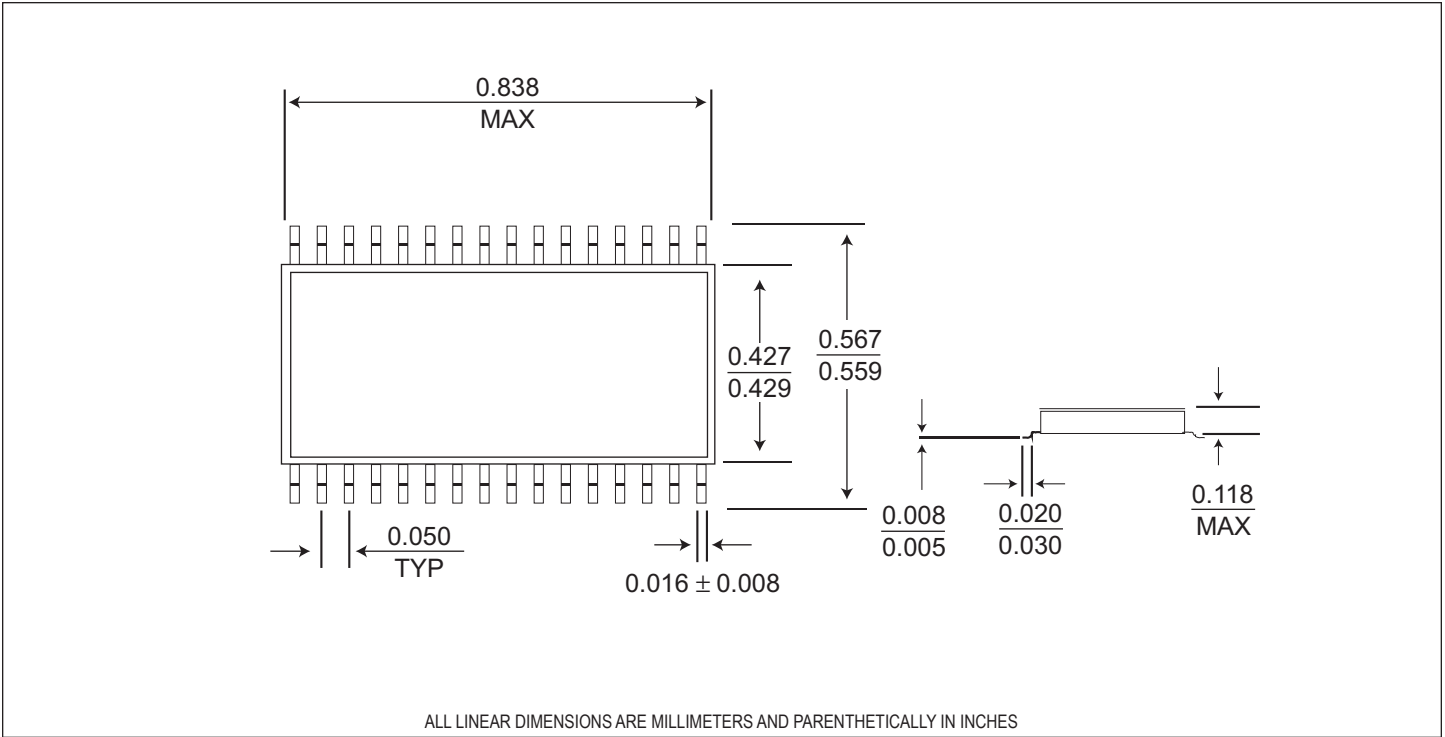
ATE tester includes jig capacitance.

TIMING WAVEFORM – READ CYCLE

WRITE CYCLE – WE# CONTROLLED

WRITE CYCLE – CS# CONTROLLED


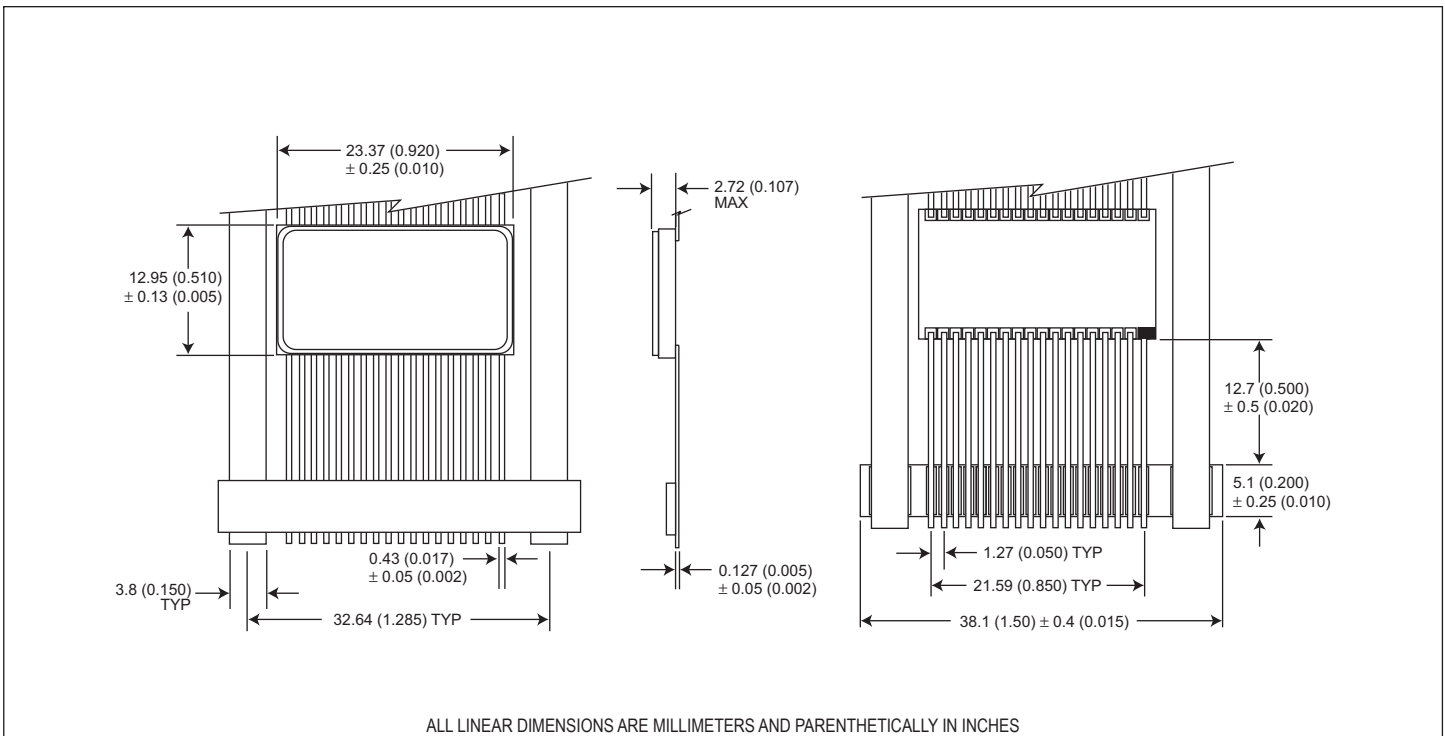
PACKAGE 100: 36 LEAD, CERAMIC SOJ

PACKAGE 101: 32 LEAD, CERAMIC SOJ


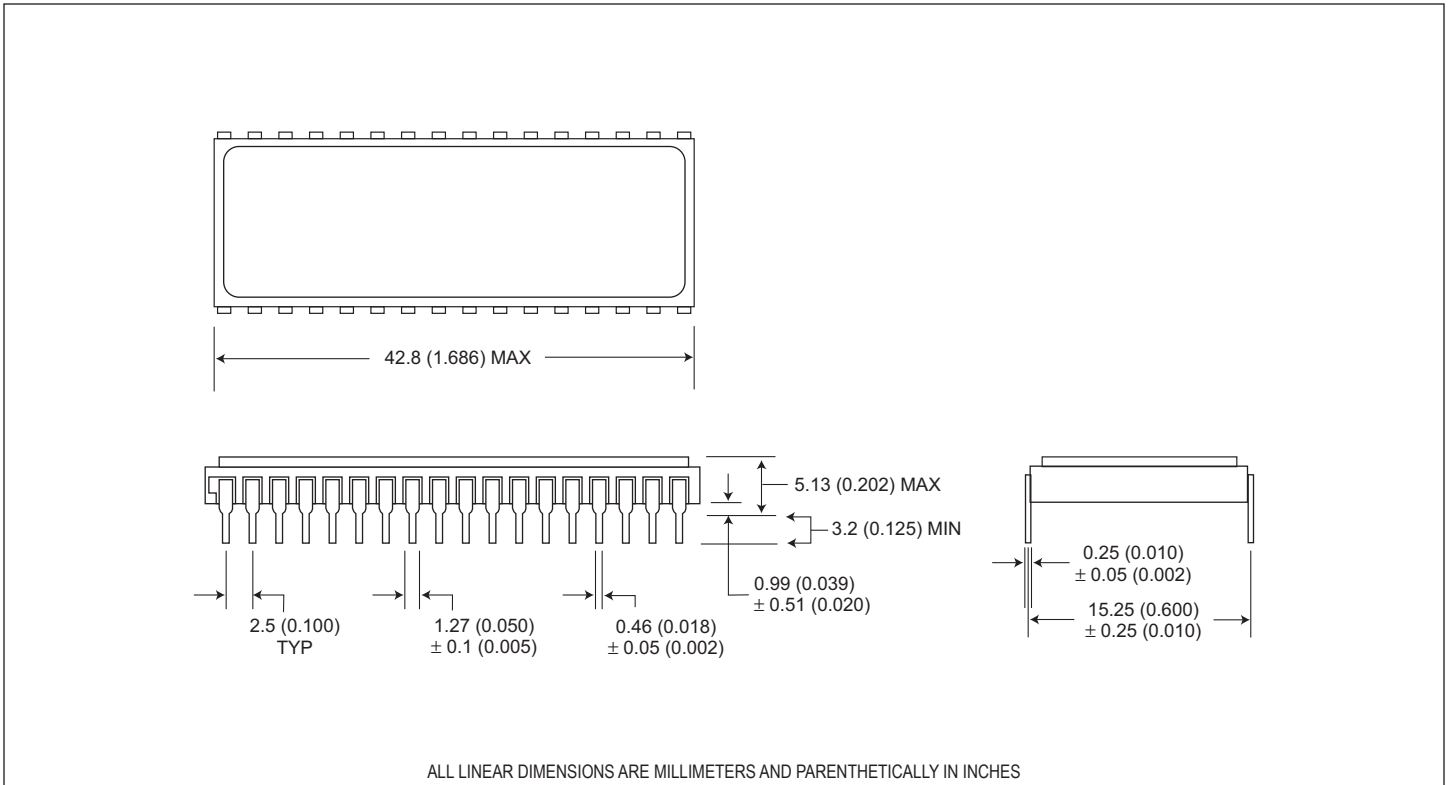


PACKAGE 321: 32 PIN CERAMIC THINPACK™ FLATPACK



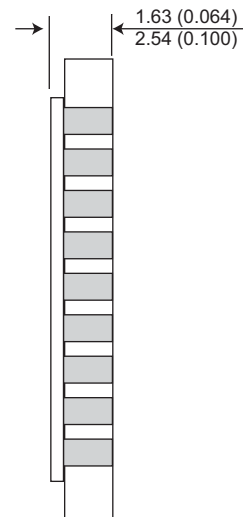
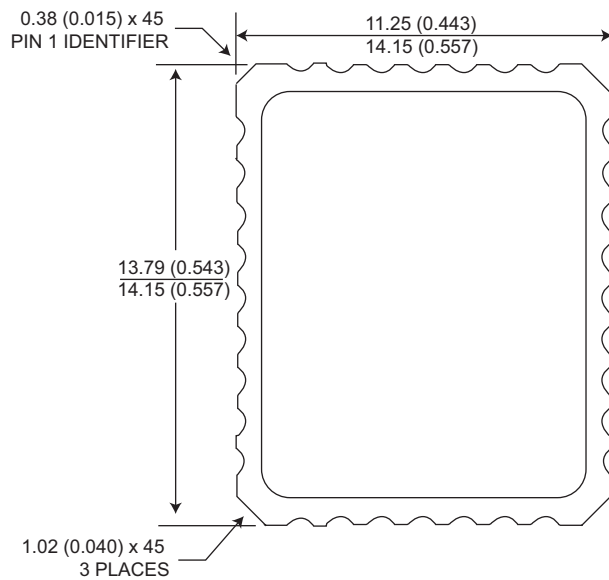
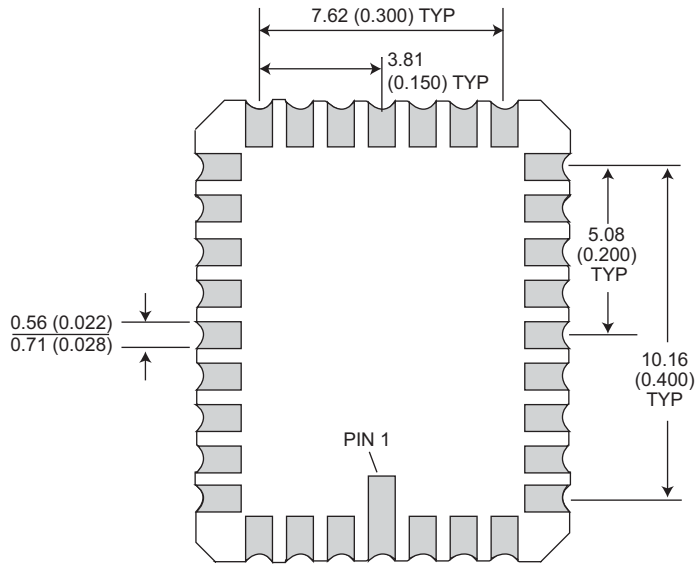
PACKAGE 226: 36 LEAD, CERAMIC FLAT PACK



PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED




PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W M S 512K 8 X - XXX X X X

MICROSEMI CORPORATION _____

MONOLITHIC _____

SRAM _____

ORGANIZATION, 512K x 8 _____

IMPROVEMENT MARK: _____

Blank = Standard

L = Low Power Data Retention

ACCESS TIME (ns) _____

PACKAGE: _____

C = 32 pin Ceramic 0.600" DIP (Package 300)

CL = 32 pin Rectangular Ceramic Leadless Chip Carrier (Package 601)

DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary

DJ = 36 Lead Ceramic SOJ (Package 100)

F = 36 Lead Ceramic Flat Pack (Package 226)

FF = 32 Lead Ceramic Thinpack™ Flat Pack (Package 321)

DEVICE GRADE: _____

Q = Military Grade*

M = Military Screened $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$

I = Industrial $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$

C = Commercial $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$

LEAD FINISH: _____

Blank = Gold plated leads

A = Solder dip leads

* This product is processed the same as the 5962-XXXXXHXX product but all test and mechanical requirements are per the Microsemi data sheet.

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 8 SRAM Monolithic	55ns	32 pin DIP (C)	5962-95613 05HYX
512K x 8 SRAM Monolithic	45ns	32 pin DIP (C)	5962-95613 06HYX
512K x 8 SRAM Monolithic	35ns	32 pin DIP (C)	5962-95613 07HYX
512K x 8 SRAM Monolithic	25ns	32 pin DIP (C)	5962-95613 08HYX
512K x 8 SRAM Monolithic	20ns	32 pin DIP (C)	5962-95613 09HYX
512K x 8 SRAM Monolithic	17ns	32 pin DIP (C)	5962-95613 10HYX
512K x 8 SRAM Monolithic	15ns	32 pin DIP (C)	5962-95613 14HYX
512K x 8 SRAM Monolithic	55ns	32 lead SOJ Evol (DE)	5962-95613 05HTX
512K x 8 SRAM Monolithic	45ns	32 lead SOJ Evol (DE)	5962-95613 06HTX
512K x 8 SRAM Monolithic	35ns	32 lead SOJ Evol (DE)	5962-95613 07HTX
512K x 8 SRAM Monolithic	25ns	32 lead SOJ Evol (DE)	5962-95613 08HTX
512K x 8 SRAM Monolithic	20ns	32 lead SOJ Evol (DE)	5962-95613 09HTX
512K x 8 SRAM Monolithic	17ns	32 lead SOJ Evol (DE)	5962-95613 10HTX
512K x 8 SRAM Monolithic	15ns	32 lead SOJ Evol (DE)	5962-95613 14HTX
512K x 8 SRAM Monolithic	55ns	36 lead SOJ (DJ)	5962-95613 05HZX
512K x 8 SRAM Monolithic	45ns	36 lead SOJ (DJ)	5962-95613 06HZX
512K x 8 SRAM Monolithic	35ns	36 lead SOJ (DJ)	5962-95613 07HZX
512K x 8 SRAM Monolithic	25ns	36 lead SOJ (DJ)	5962-95613 08HZX
512K x 8 SRAM Monolithic	20ns	36 lead SOJ (DJ)	5962-95613 09HZX
512K x 8 SRAM Monolithic	17ns	36 lead SOJ (DJ)	5962-95613 10HZX
512K x 8 SRAM Monolithic	15ns	36 lead SOJ (DJ)	5962-95613 14HZX
512K x 8 SRAM Monolithic	55ns	36 lead Flatpack (F)	5962-95613 05HXX
512K x 8 SRAM Monolithic	45ns	36 lead Flatpack (F)	5962-95613 06HXX
512K x 8 SRAM Monolithic	35ns	36 lead Flatpack (F)	5962-95613 07HXX
512K x 8 SRAM Monolithic	25ns	36 lead Flatpack (F)	5962-95613 08HXX
512K x 8 SRAM Monolithic	20ns	36 lead Flatpack (F)	5962-95613 09HXX
512K x 8 SRAM Monolithic	17ns	36 lead Flatpack (F)	5962-95613 10HXX
512K x 8 SRAM Monolithic	15ns	36 lead Flatpack (F)	5962-95613 14HXX

Document Title

512Kx8 MONOLITHIC SRAM, SMD 5962-95613

Revision History

Rev #	History	Release Date	Status
Rev 12	Changes (Pg. 1-11) 12.1 Change document layout from White Electronic Designs to Microsemi 12.2 Add document Revision History page	March 2011	Final
Rev 13	Changes (Pg. 2) 13.1 Correct typo in Absolute Maximum Ratings – Signal Voltage Range to Ground Max from $V_{CC}-0.5$ to $V_{CC}+0.5$ 13.1 Correct typo in DC Characteristics – CMOS Compatible - Operating Supply Current Conditions from $CS\# = V_{IH}$ to $CS\# = V_{IL}$	April 2012	Final
Rev 14	Change (Pg. 9) 14.1 Changed Device Grade "Q" description from "MIL-STD-883 Compliant" to "MIL-PRF-38534 Class H Compliant."	May 2014	Final
Rev 15	Change (Pg. 9) 15.1 Changed Device Grade "Q" description from "MIL-PRF-38534 Class H Compliant." to "Military Grade."	August 2014	Final