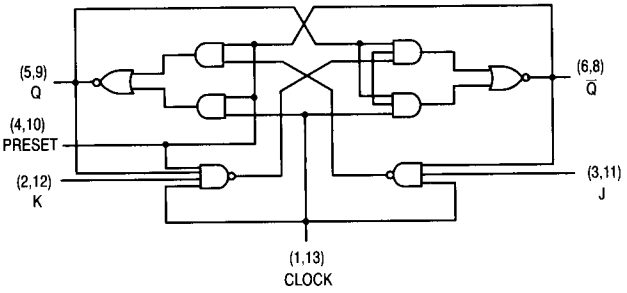
MOTOROLA

Dual J-K Flip-Flop With Preset

ELECTRICALLY TESTED PER:
MIL-M-38510/30104

The 54LS113A offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs			Outputs	
	$\overline{PR}$	J	K	Q	$\overline{Q}$
Set	L	X	X	H	L
Toggle	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	$\overline{q}$

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

Military 54LS113A

MPO

AVAILABLE AS:

1) JAN: JM38510/30104BXA
2) SMD: N/A
3) 883: 54LS113A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
CLK_1	1	1	2	V_{CC}
K_1	2	2	3	V_{CC}
J_1	3	3	4	V_{CC}
PR_1	4	4	6	GND
Q_1	5	5	8	V_{CC}
$\overline{Q}_1$	6	6	9	OPEN
GND	7	7	10	GND
$\overline{Q}_2$	8	8	12	OPEN
Q_2	9	9	13	V_{CC}
PR_2	10	10	14	GND
J_2	11	11	16	V_{CC}
K_2	12	12	18	V_{CC}
CLK_2	13	13	19	V_{CC}
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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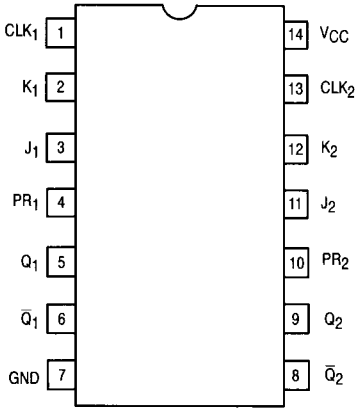
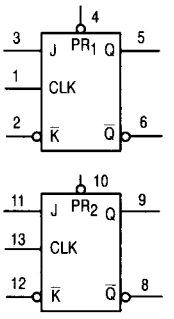
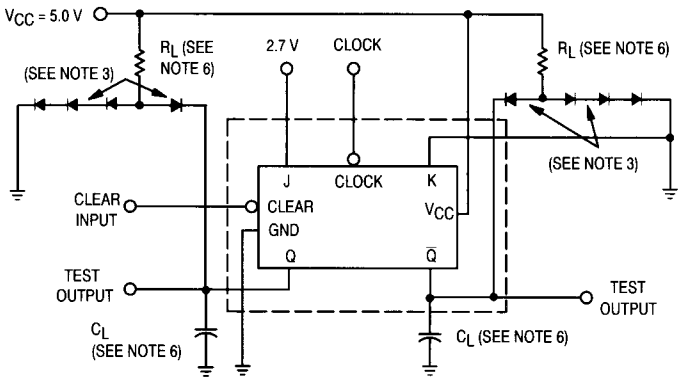
CONNECTION DIAGRAM



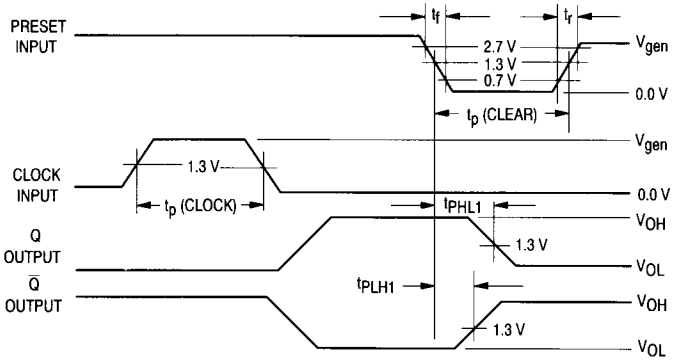
LOGIC SYMBOL



CLEAR SWITCHING TEST CIRCUIT



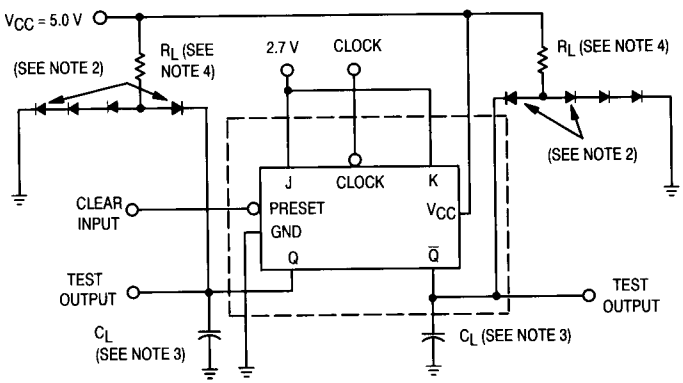
WAVEFORMS



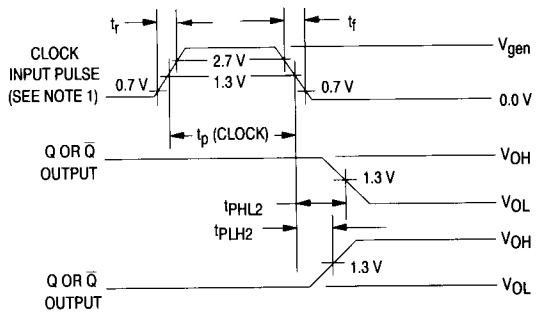
NOTES:

1. Preset inputs dominate regardless of the state of the clock or J-K inputs.
2. Preset input pulse characteristics: V_{gen} = 3.0 V, $t_f \leq 15$ ns, $t_r \leq 6.0$ ns, t_p (preset) = 30 ns, PRR ≤ 1.0 MHz.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. Voltage measurements are to be made with respect to network ground terminal.
6. R_L = 2.0 kΩ ± 5.0%.
7. Clock input pulse characteristics: V_{gen} = 3.0 V, t_p (clock) ≤ 25 ns, PRR ≤ 1.0 MHz.

SYNCHRONOUS SWITCHING TEST CIRCUIT



WAVEFORMS



NOTES:

1. Clock input characteristics for t_{PLH}, t_{PHL} (clock to output): V_{gen} = 3.0 V, $t_r \leq 15$ ns, t_f = 6.0 ns, t_p (clock) = 20 ns and PRR = ≤ 1.0 MHz. When testing f_{MAX} the clock input characteristics are: V_{gen} = 3.0 V, $t_r = t_f \leq 6.0$ ns, t_p (clock) ≤ 20 ns and PRR = (see table).
2. All diodes are 1N3064, or equivalent.
3. C_L = 50 pF ± 10% (including jig and probe capacitance).
4. R_L = 2.0 kΩ ± 5.0%.

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Symbol	Parameter		Limits						Unit	Test Condition (Unless Otherwise Specified)	
	Static Parameters:		+ 25°C		+ 125°C		− 55°C				
			Subgroup 1		Subgroup 2		Subgroup 3				
			Min	Max	Min	Max	Min	Max			
V_{OH}	Logical "1" Output Voltage		2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IN} = 2.0 V, V_{IL} = 0.7 V.	
V_{OL}	Logical "0" Output Voltage			0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.7 V.	
V_{IC}	Input Clamping Voltage			− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.	
I_{IH}	Logical "1" Input Current (J & K inputs)			20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other input = GND.	
I_{IHH}	Logical "1" Input Current (J & K inputs)			100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, PR = 4.5 V, K = GND, CLK = (see note 1).	
I_{IH}	Logical "1" Input Current (PR inputs)			60		60		60	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, J = 4.5 V, CLK & K = GND, Q = (see note 3).	
I_{IHH}	Logical "1" Input Current (PR inputs)			300		300		300	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, J = 4.5 V, CLK & K = GND, Q = (see note 3).	
I_{IH}	Logical "1" Input Current (CLK inputs)			80		80		80	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs = GND.	
I_{IHH}	Logical "1" Input Current (CLK inputs)			400		400		400	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs = GND.	
I_{IL}	Logical "0" Input Current (J & K inputs)		− 0.12	− 0.36	− 0.12	− 0.36	− 0.12	− 0.36	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, CLK = 4.5 V, J = 0 V, PR = (see note 2).	
I_{IL}	Logical "0" Input Current (CLK inputs)		− 0.24	− 0.72	− 0.24	− 0.72	− 0.24	− 0.72	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, J & K = 4.5 V, PR = (see note 2).	
I_{IL}	Logical "0" Input Current (PR inputs)		− 0.12	− 0.72	− 0.12	− 0.72	− 0.12	− 0.72	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs = 4.5 V.	
I_{OS}	Output Short Circuit Current	Q_1 & Q_2	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, Q = GND.	PR = GND, other inputs are open.
		$\overline{Q}_1$ & $\overline{Q}_2$	− 7.5	− 50	− 7.5	− 50	− 7.5	− 50			J = GND, V_{IN} = 4.5 V, CLK = (see note 1), V_{OUT} = 2.25 V.
I_{CC}	Power Supply Current			8.0		8.0		8.0	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, CLK = (see note 1), J = GND.	
										V_{CC} = 5.5 V, PR = GND, other inputs are 5.5 V.	
V_{IH}	Logical "1" Input Voltage		2.0		2.0		2.0		V	V_{CC} = 4.5 V.	
V_{IL}	Logical "0" Input Voltage			0.7		0.7		0.7	V	V_{CC} = 4.5 V.	
	Functional Tests		Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.	

NOTES: 1. = 0.0 V 2.5 V min/5.5 V max 2. = 0.0 V 2.5 V min/5.5 V max 3. Momentary GND, then open.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Output High-Low	5.0 —	28 20	5.0 —	40 35	5.0 —	40 35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Output Low-High	5.0 —	21 20	5.0 —	32 27	5.0 —	32 27	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output Output High-Low	5.0 —	30 20	5.0 —	42 37	5.0 —	42 37	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output Output Low-High	5.0 —	22 20	5.0 —	32 27	5.0 —	32 27	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	25		25		25		MHz	V_{CC} = 5.0 V, V_{IN} = 2.7 V, C_L = 50 pF, R_L = 2.0 kΩ ± 5.0%.
f_{MAX}	Maximum Clock Frequency	30						MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ ± 5.0%.

NOTES:

1. f_{MAX}, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C_L = 15 pF are guaranteed but not tested.

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