

RJM0306JSP

Silicon N / P Channel Power MOS FET
High Speed Power Switching

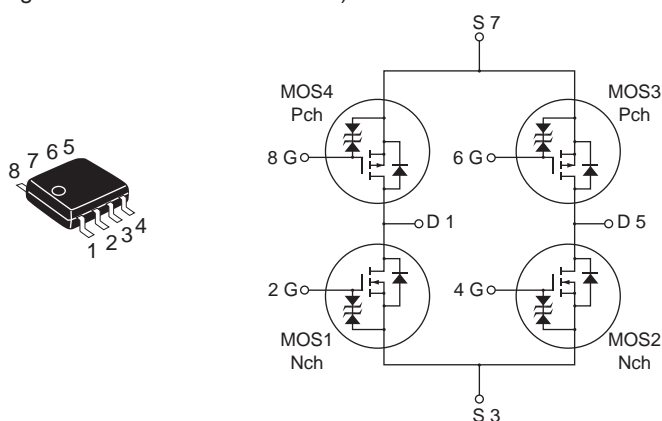
REJ03G1571-0101
Rev.1.01
May 28, 2010

Features

- Two elements each of N and P channels are incorporated (suitable for H-bridge circuit)
- High density mounting
- Low on-resistance
- Capable of 4 V gate drive
- High temperature D-S leakage guarantee
Avalanche rating

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8 <FP-8DAV>)



Pin No.	Element	Electrode
1	MOS1 (Nch)	Drain
	MOS4 (Pch)	
2	MOS1 (Nch)	Gate
3	MOS1 (Nch)	Source
	MOS2 (Nch)	
4	MOS2 (Nch)	Gate
5	MOS2 (Nch)	Drain
	MOS3 (Pch)	
6	MOS3 (Pch)	Gate
7	MOS3 (Pch)	Source
	MOS4 (Pch)	
8	MOS4 (Pch)	Gate

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value		Unit
		MOS1, 2 (Nch)	MOS3, 4 (Pch)	
Drain to source voltage	V _{DSS}	30	-30	V
Gate to source voltage	V _{GSS}	±20	±20	V
Drain current	I _D	3.5	-3.5	A
Drain peak current	I _D (pulse) ^{Note 1}	28	-28	A
Avalanche current	I _{AP} ^{Note 4}	3.5	-3.5	A
Avalanche energy	E _{AR} ^{Note 4}	1.22	1.22	mJ
Channel dissipation	P _{ch} ^{Note 2}	1.5		W
Channel dissipation	P _{ch} ^{Note 3}	2.2		W
Channel temperature	T _{ch}	150		°C
Storage temperature	T _{stg}	-55 to +150		°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. 1 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s

3. 2 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s

4. Value at T_{ch} = 25°C, R_g ≥ 50 Ω

Electrical Characteristics

MOS1, 2 (Nch)

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}, V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 24 \text{ V}, V_{GS} = 0,$ $T_A = 125^\circ\text{C}$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	50	65	$\text{m}\Omega$	$I_D = 2.0 \text{ A}^{\text{Note5}}, V_{GS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	70	105	$\text{m}\Omega$	$I_D = 2.0 \text{ A}^{\text{Note5}}, V_{GS} = 4.5 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	80	130	$\text{m}\Omega$	$I_D = 2.0 \text{ A}^{\text{Note5}}, V_{GS} = 4.0 \text{ V}$
Input capacitance	C_{iss}	—	290	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	85	—	pF	
Reverse transfer capacitance	C_{rss}	—	30	—	pF	
Total gate charge	Q_g	—	5.0	—	nC	$V_{DD} = 10 \text{ V}, V_{GS} = 10 \text{ V},$ $I_D = 3.5 \text{ A}$
Gate to source charge	Q_{gs}	—	1.2	—	nC	
Gate to drain charge	Q_{gd}	—	0.6	—	nC	
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	$V_{GS} = 10 \text{ V}, I_D = 2.0 \text{ A},$ $V_{DD} \cong 10 \text{ V}, R_L = 5 \text{ }\Omega,$ $R_G = 4.7 \text{ }\Omega$
Rise time	t_r	—	12	—	ns	
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	8	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.88	1.15	V	
Body-drain diode reverse recovery time	t_{rr}	—	25	—	ns	$I_F = 3.5 \text{ A}, V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Note: 5. Pulse test

MOS3, 4 (Pch)

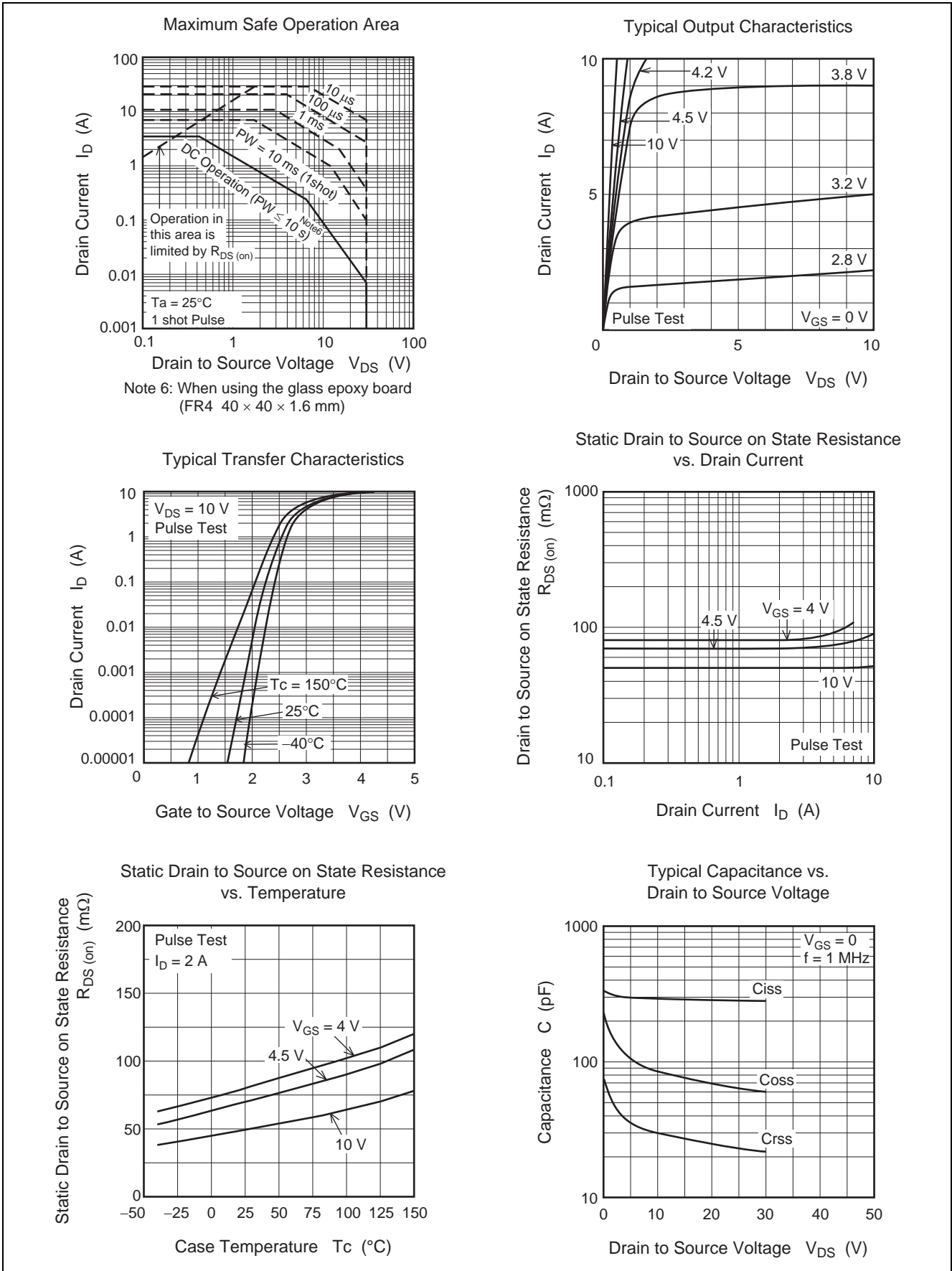
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -24 \text{ V}$, $V_{GS} = 0$, $T_a = 125^\circ\text{C}$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	90	120	$\text{m}\Omega$	$I_D = -2.0 \text{ A}^{\text{Note5}}$, $V_{GS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	140	210	$\text{m}\Omega$	$I_D = -2.0 \text{ A}^{\text{Note5}}$, $V_{GS} = -4.5 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	160	260	$\text{m}\Omega$	$I_D = -2.0 \text{ A}^{\text{Note5}}$, $V_{GS} = -4.0 \text{ V}$
Input capacitance	C_{iss}	—	320	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	85	—	pF	
Reverse transfer capacitance	C_{rss}	—	50	—	pF	
Total gate charge	Q_g	—	6.0	—	nC	$V_{DD} = -10 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -3.5 \text{ A}$
Gate to source charge	Q_{gs}	—	1.4	—	nC	
Gate to drain charge	Q_{gd}	—	1.0	—	nC	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$V_{GS} = -10 \text{ V}$, $I_D = -2.0 \text{ A}$, $V_{DD} \cong -10 \text{ V}$, $R_L = 5.0 \text{ }\Omega$, $R_G = 4.7 \text{ }\Omega$
Rise time	t_r	—	17	—	ns	
Turn-off delay time	$t_{d(off)}$	—	30	—	ns	
Fall time	t_f	—	7	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-0.92	-1.2	V	$I_F = -3.5 \text{ A}$, $V_{GS} = 0^{\text{Note5}}$
Body-drain diode reverse recovery time	t_{rr}	—	30	—	ns	$I_F = -3.5 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

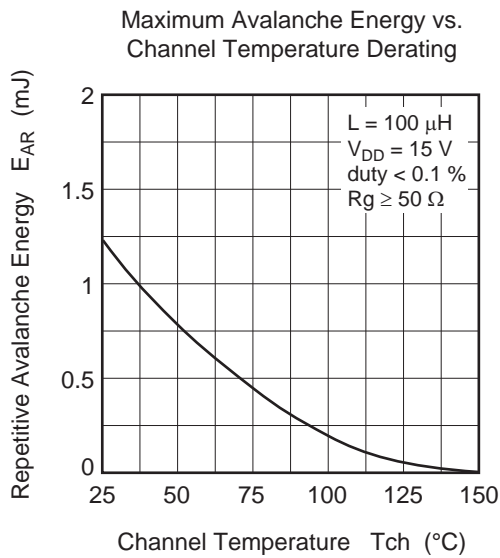
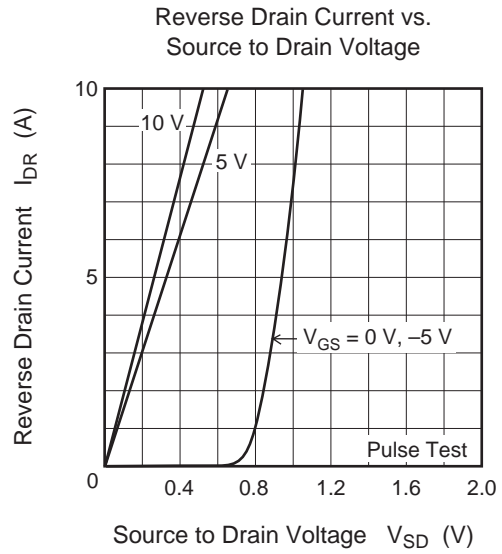
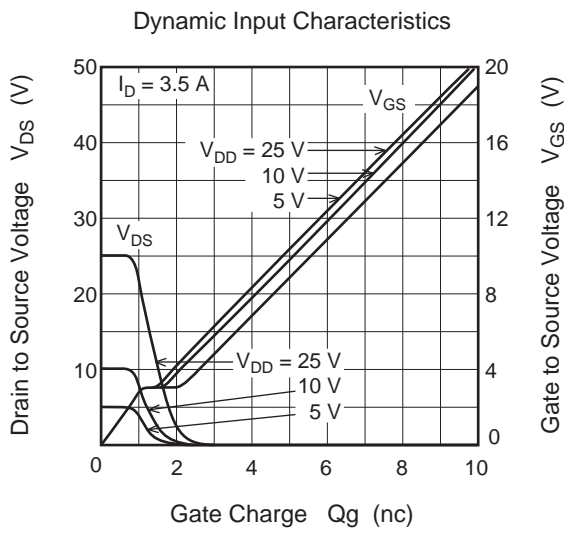
Note: 5. Pulse test

Main Characteristics

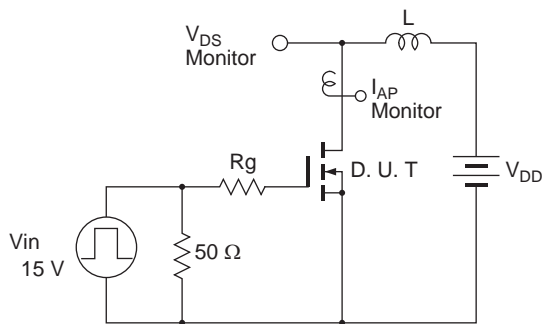
MOS1, 2 (Nch)



MOS1, 2 (Nch)

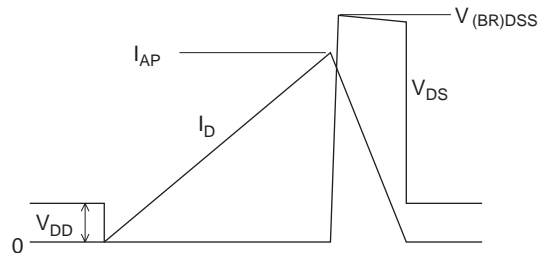


Avalanche Test Circuit

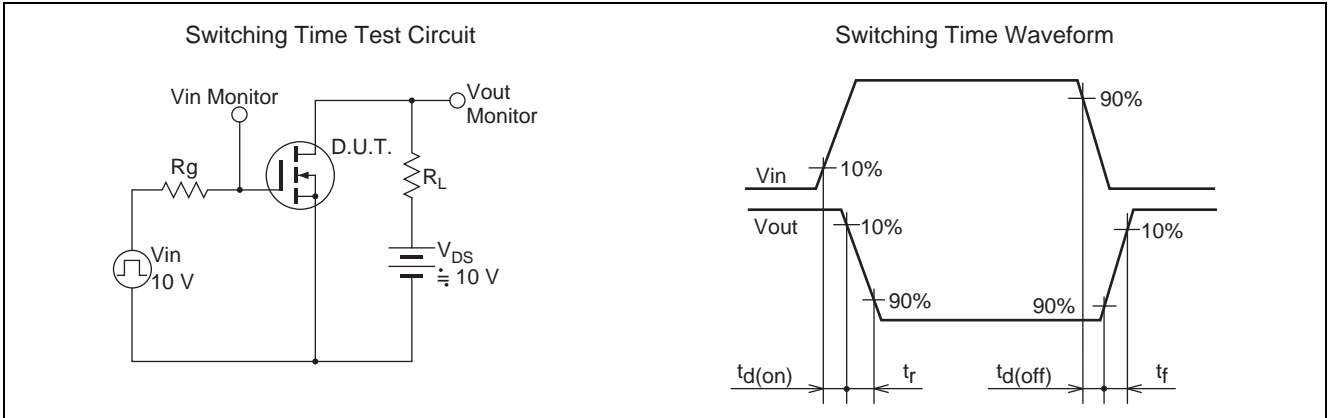


Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

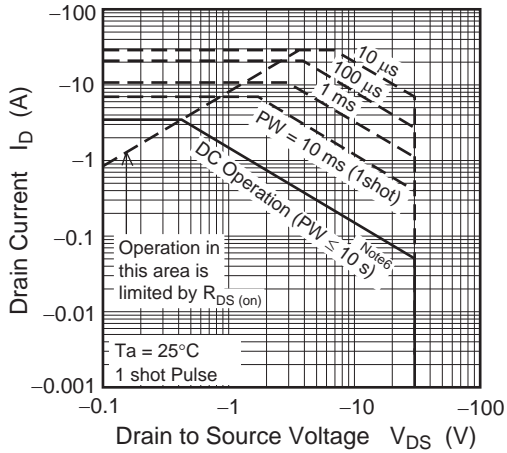


MOS1, 2 (Nch)

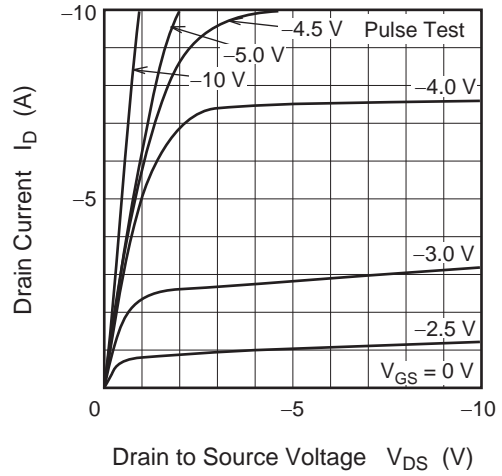


MOS3, 4 (Pch)

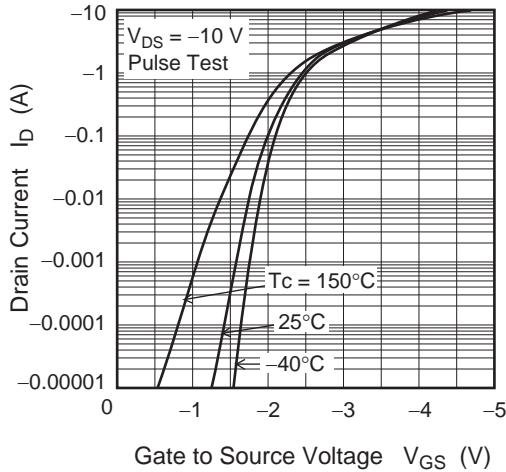
Maximum Safe Operation Area



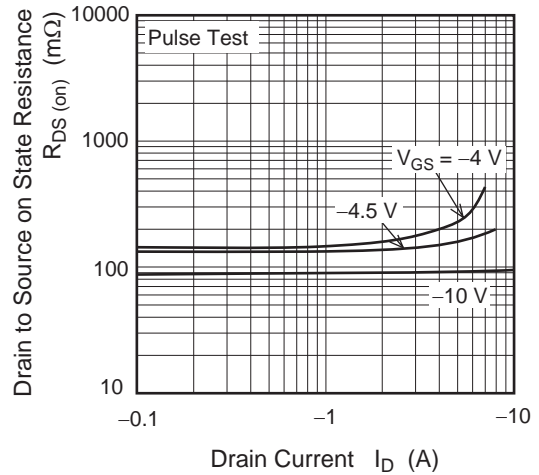
Typical Output Characteristics



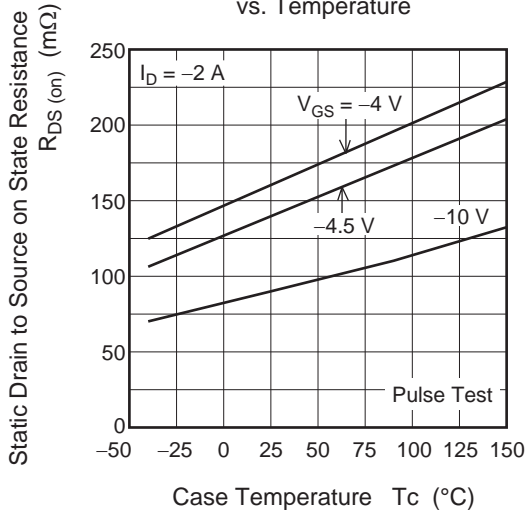
Typical Transfer Characteristics



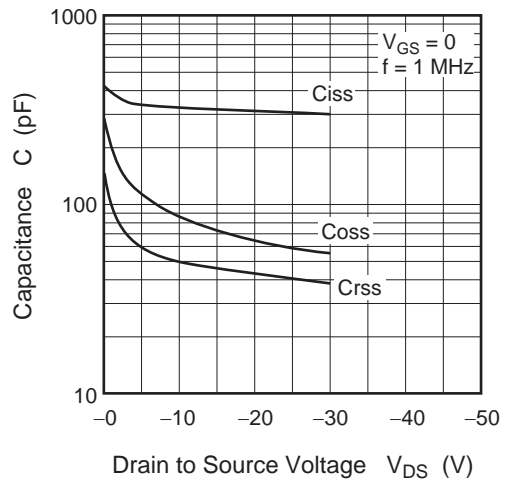
Static Drain to Source on State Resistance vs. Drain Current



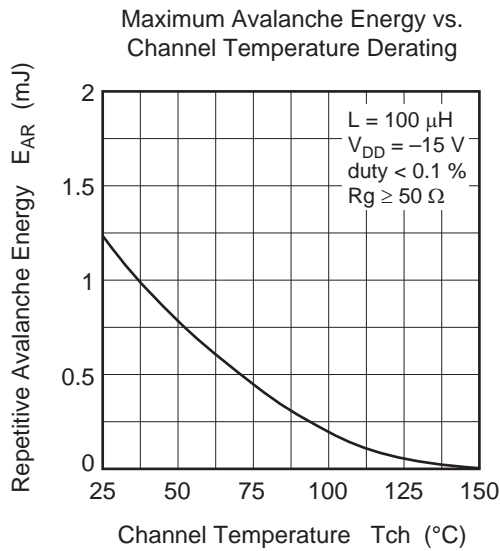
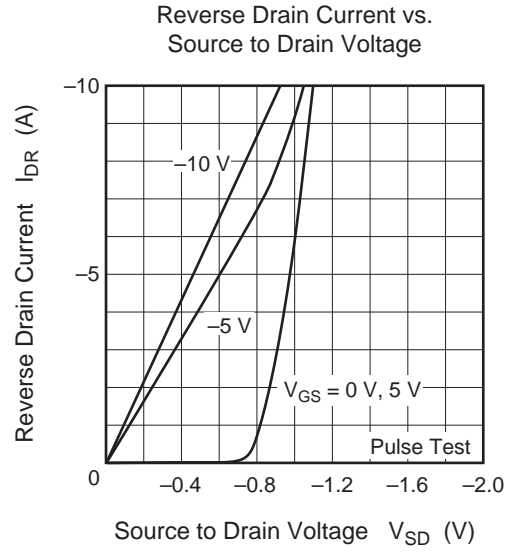
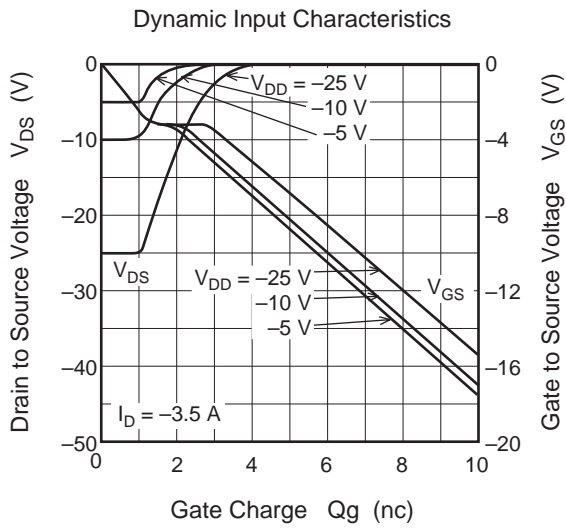
Static Drain to Source on State Resistance vs. Temperature



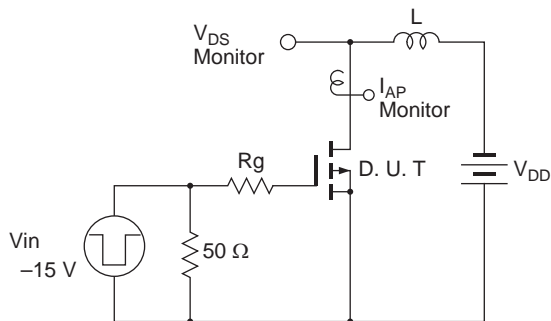
Typical Capacitance vs. Drain to Source Voltage



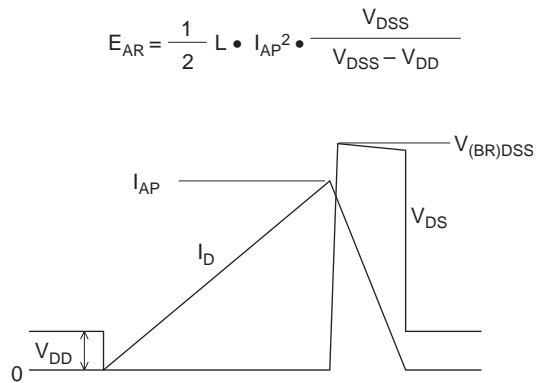
MOS3, 4 (Pch)



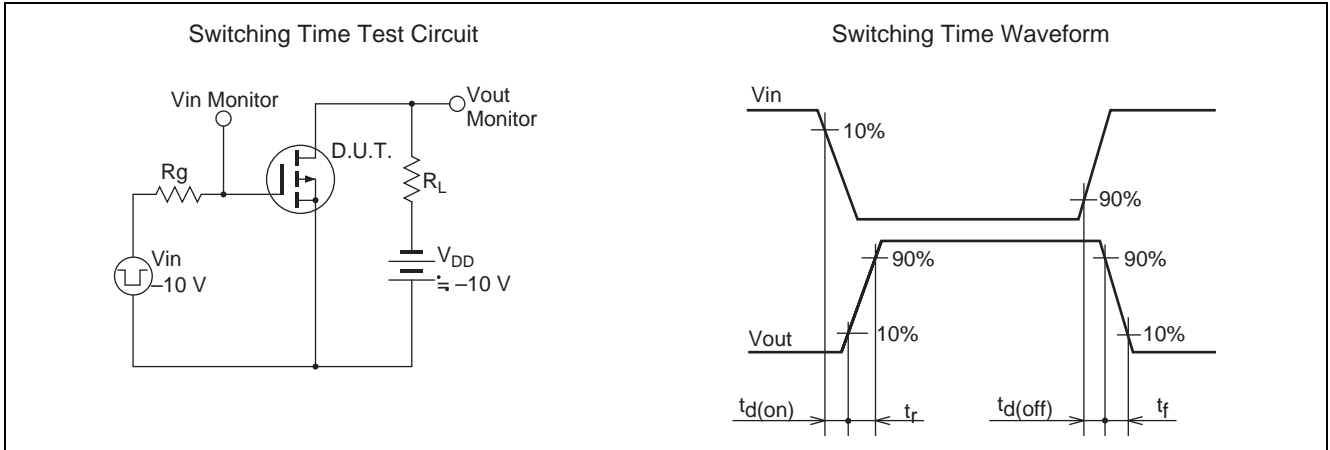
Avalanche Test Circuit



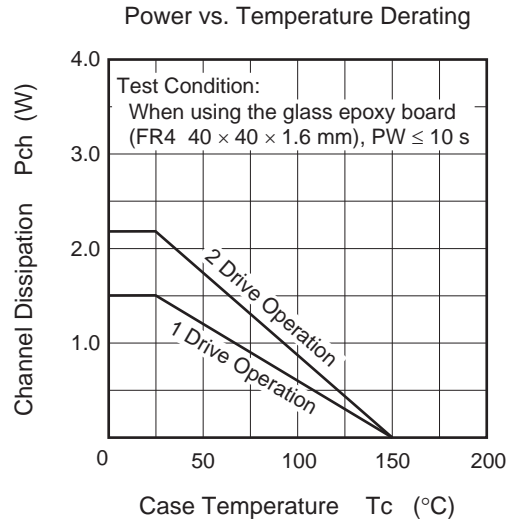
Avalanche Waveform



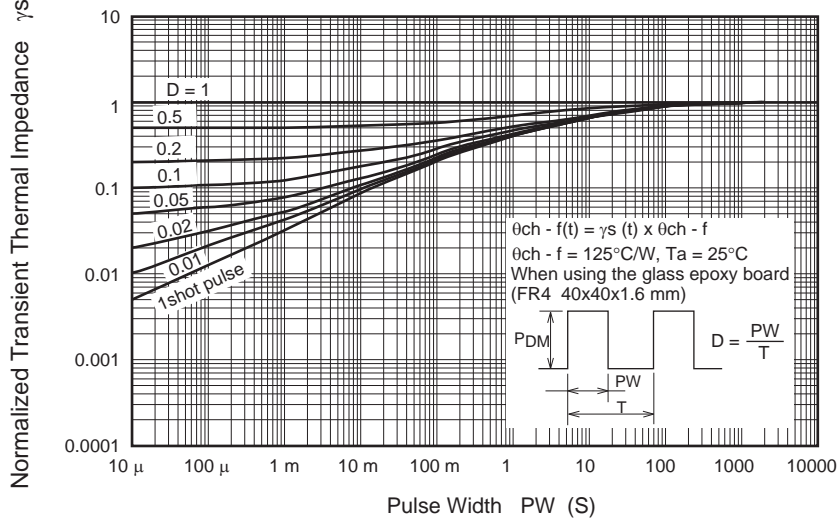
MOS3, 4 (Pch)



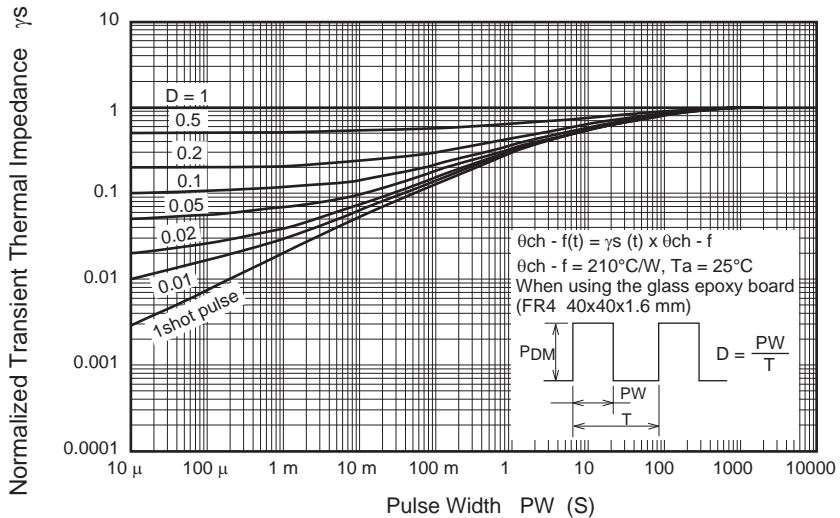
Common



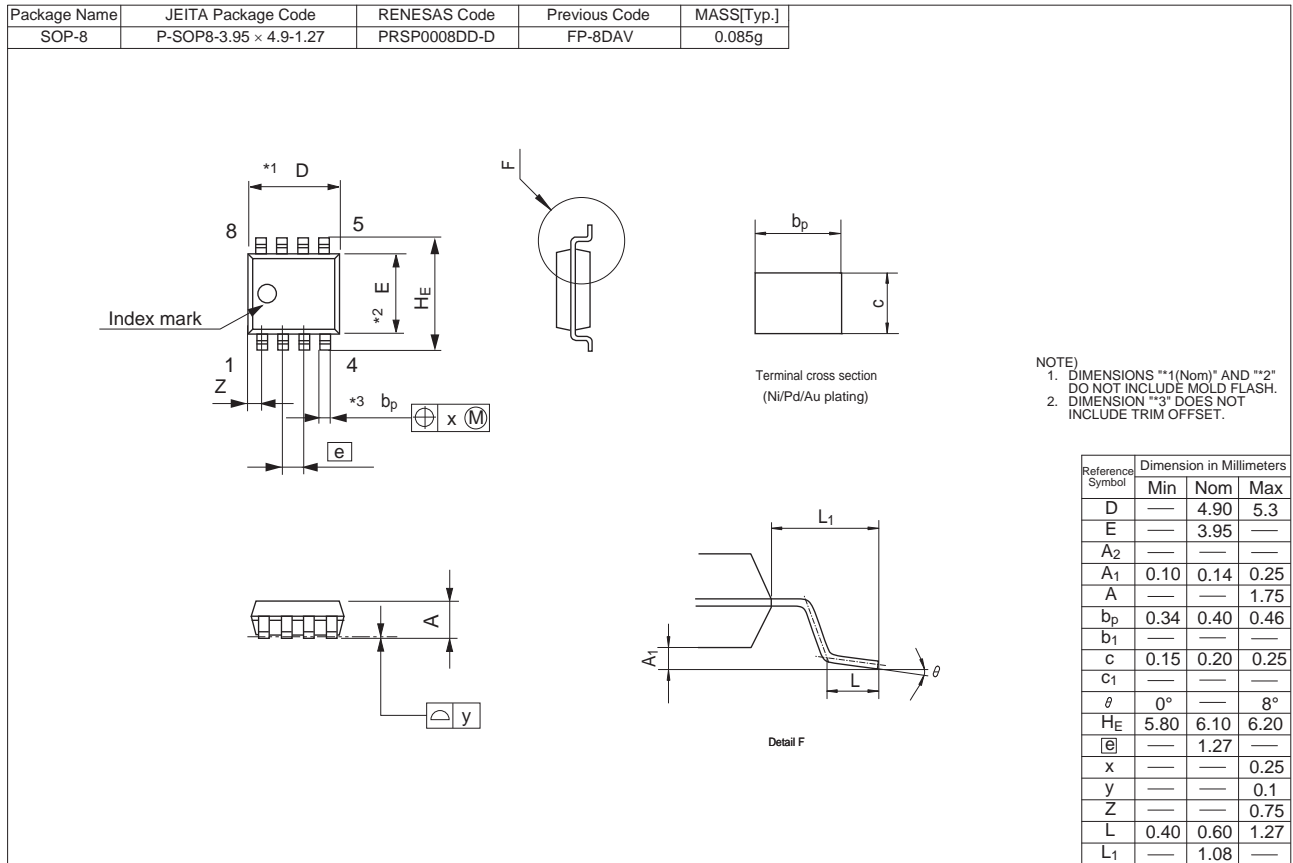
Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)



Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RJM0306JSP-00-J0	2500 pcs	Taping

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