RJM0306JSP

Silicon N / P Channel Power MOS FET
High Speed Power Switching

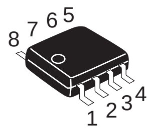
REJ03G1571-0101
Rev.1.01
May 28, 2010

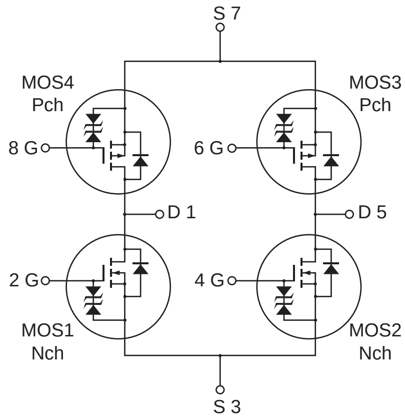
Features

- Two elements each of N and P channels are incorporated (suitable for H-bridge circuit)
- High density mounting
- Low on-resistance
- Capable of 4 V gate drive
- High temperature D-S leakage guarantee
  Avalanche rating

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8 <FP-8DAV>)





Pin No.	Element	Electrode
1	MOS1 (Nch)	Drain
	MOS4 (Pch)	
2	MOS1 (Nch)	Gate
3	MOS1 (Nch)	Source
	MOS2 (Nch)	
4	MOS2 (Nch)	Gate
5	MOS2 (Nch)	Drain
	MOS3 (Pch)	
6	MOS3 (Pch)	Gate
7	MOS3 (Pch)	Source
	MOS4 (Pch)	
8	MOS4 (Pch)	Gate

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value		Unit
		MOS1, 2 (Nch)	MOS3, 4 (Pch)	
Drain to source voltage	V_{DSS}	30	–30	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	3.5	–3.5	A
Drain peak current	I_D (pulse)[Note 1]	28	–28	A
Avalanche current	I_{AP}[Note 4]	3.5	–3.5	A
Avalanche energy	E_{AR}[Note 4]	1.22	1.22	mJ
Channel dissipation	Pch[Note 2]	1.5		W
Channel dissipation	Pch[Note 3]	2.2		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. 1 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
3. 2 Drive operation: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
4. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics

MOS1, 2 (Nch)

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 μA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 30 V, V_{GS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	V_{DS} = 24 V, V_{GS} = 0, Ta = 125°C
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	50	65	mΩ	I_D = 2.0 A[Note5], V_{GS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	70	105	mΩ	I_D = 2.0 A[Note5], V_{GS} = 4.5 V
Static drain to source on state resistance	$R_{DS(on)}$	—	80	130	mΩ	I_D = 2.0 A[Note5], V_{GS} = 4.0 V
Input capacitance	Ciss	—	290	—	pF	V_{DS} = 10 V, V_{GS} = 0 , f = 1 MHz
Output capacitance	Coss	—	85	—	pF	
Reverse transfer capacitance	Crss	—	30	—	pF	
Total gate charge	Qg	—	5.0	—	nC	V_{DD} = 10 V, V_{GS} = 10 V, I_D = 3.5 A
Gate to source charge	Qgs	—	1.2	—	nC	
Gate to drain charge	Qgd	—	0.6	—	nC	
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	V_{GS} = 10 V, I_D = 2.0 A, V_{DD} ≅ 10 V, R_L = 5 Ω, R_G = 4.7 Ω
Rise time	t_r	—	12	—	ns	
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	8	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.88	1.15	V	I_F = 3.5 A, V_{GS} = 0[Note5]
Body-drain diode reverse recovery time	t_{rr}	—	25	—	ns	I_F = 3.5A, V_{GS} = 0 di_F/dt = 100 A/μs

Note: 5. Pulse test

MOS3, 4 (Pch)

(Ta = 25°C)

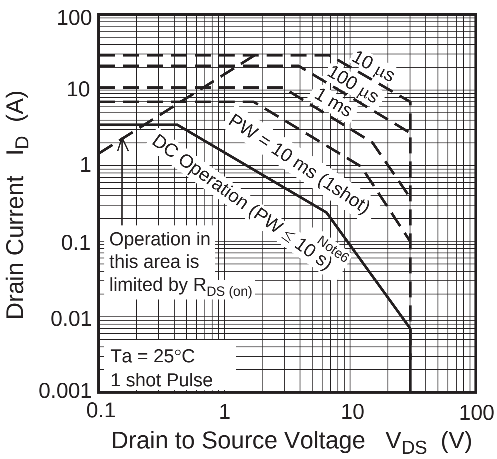
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 μA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	μA	V_{DS} = –30 V, V_{GS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	μA	V_{DS} = –24 V, V_{GS} = 0, Ta = 125°C
Gate to source leak current	I_{GSS}	—	—	±10	μA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	90	120	mΩ	I_D = –2.0 A[Note5], V_{GS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	140	210	mΩ	I_D = –2.0 A[Note5], V_{GS} = –4.5 V
Static drain to source on state resistance	$R_{DS(on)}$	—	160	260	mΩ	I_D = –2.0 A[Note5], V_{GS} = –4.0 V
Input capacitance	Ciss	—	320	—	pF	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	85	—	pF	
Reverse transfer capacitance	Crss	—	50	—	pF	
Total gate charge	Qg	—	6.0	—	nC	V_{DD} = –10 V, V_{GS} = –10 V, I_D = –3.5 A
Gate to source charge	Qgs	—	1.4	—	nC	
Gate to drain charge	Qgd	—	1.0	—	nC	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	V_{GS} = –10 V, I_D= –2.0 A, V_{DD} ≅ –10 V, R_L = 5.0 Ω, R_G = 4.7 Ω
Rise time	t_r	—	17	—	ns	
Turn-off delay time	$t_{d(off)}$	—	30	—	ns	
Fall time	t_f	—	7	—	ns	
Body-drain diode forward voltage	V_{DF}	—	–0.92	–1.2	V	I_F = –3.5 A, V_{GS} = 0[Note5]
Body-drain diode reverse recovery time	t_{rr}	—	30	—	ns	I_F = –3.5 A, V_{GS} = 0, di_F/dt = 100 A/μs

Note: 5. Pulse test

Main Characteristics

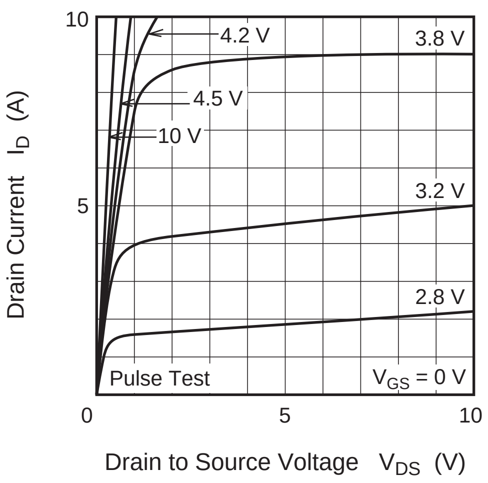
MOS1, 2 (Nch)

Maximum Safe Operation Area

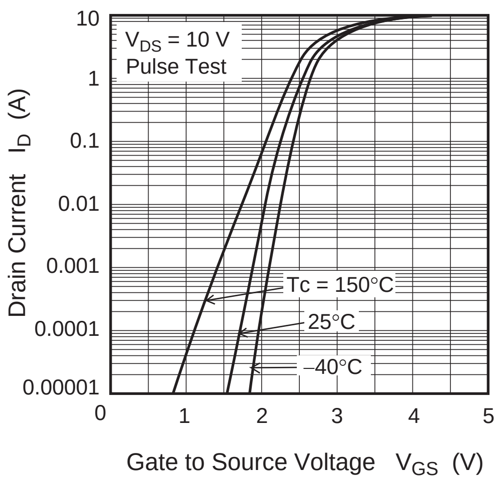


Note 6: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm)

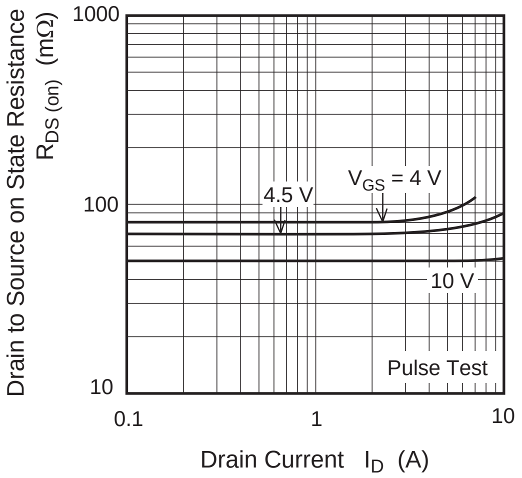
Typical Output Characteristics



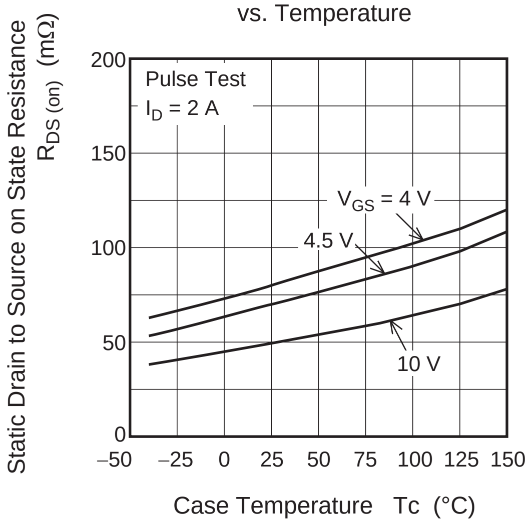
Typical Transfer Characteristics



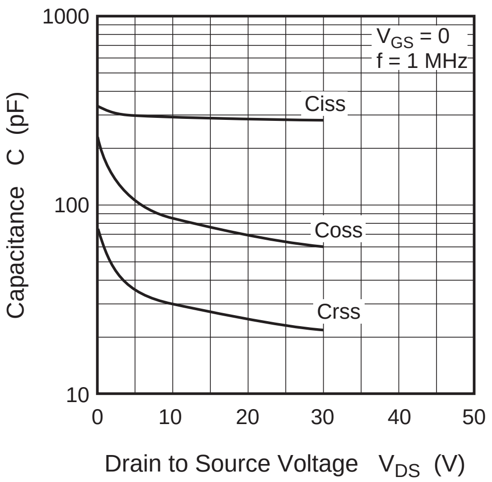
Static Drain to Source on State Resistance vs. Drain Current



Static Drain to Source on State Resistance vs. Temperature

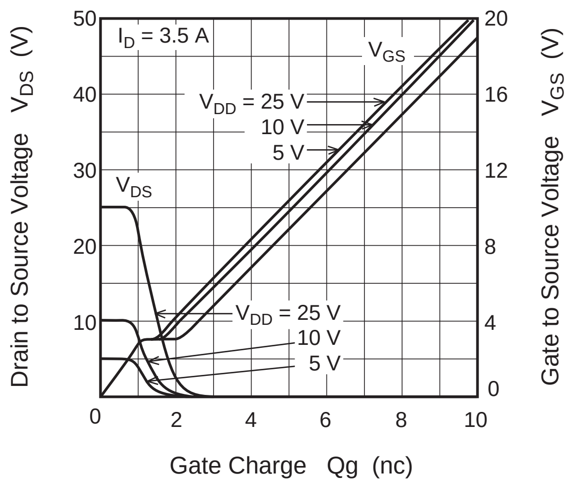


Typical Capacitance vs. Drain to Source Voltage

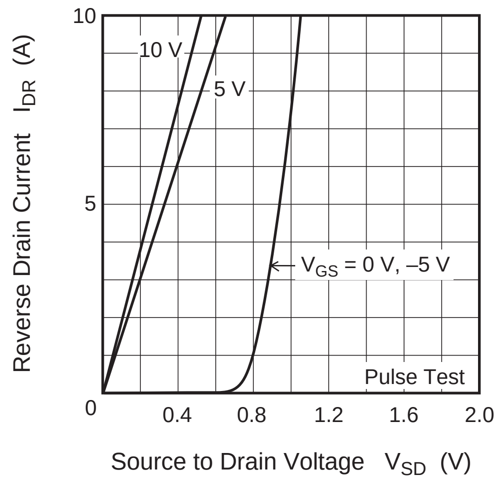


MOS1, 2 (Nch)

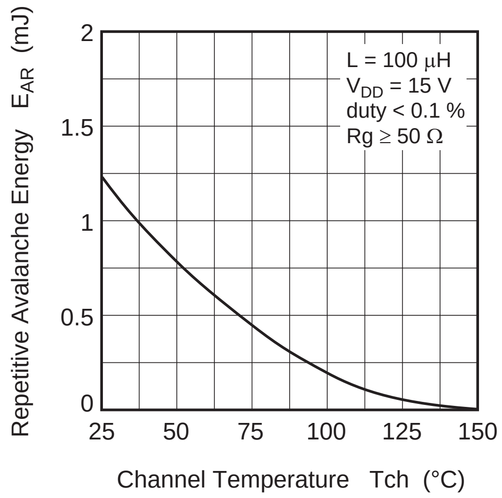
Dynamic Input Characteristics



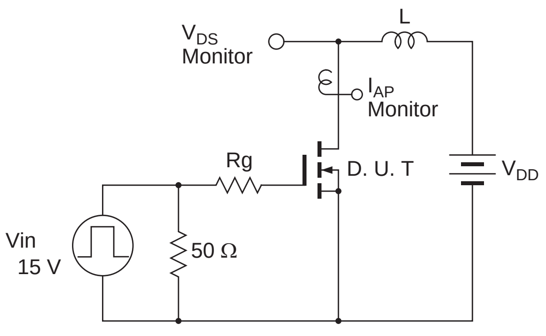
Reverse Drain Current vs. Source to Drain Voltage



Maximum Avalanche Energy vs. Channel Temperature Derating

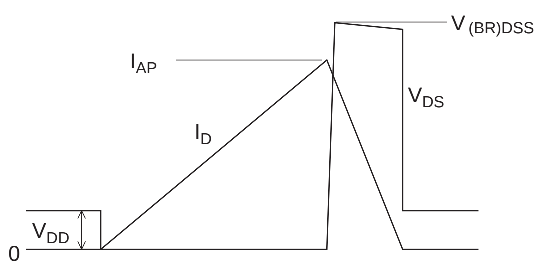


Avalanche Test Circuit



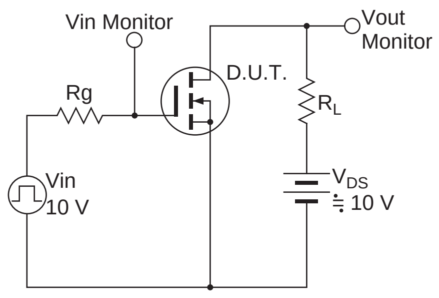
Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

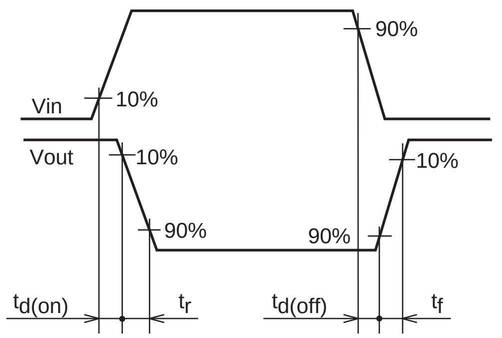


MOS1, 2 (Nch)

Switching Time Test Circuit

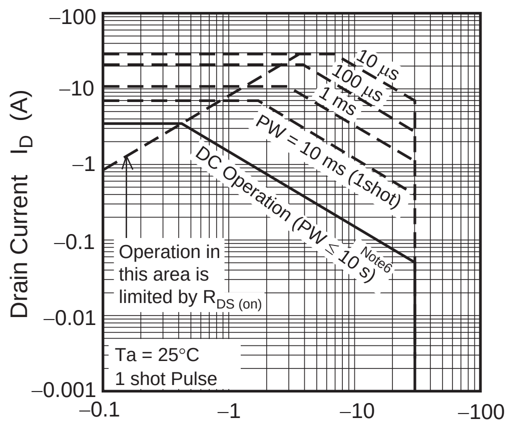


Switching Time Waveform



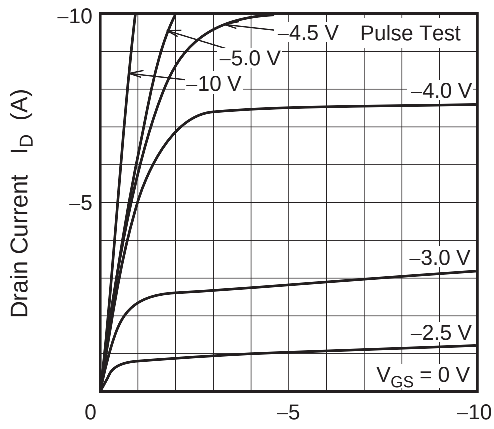
MOS3, 4 (Pch)

Maximum Safe Operation Area

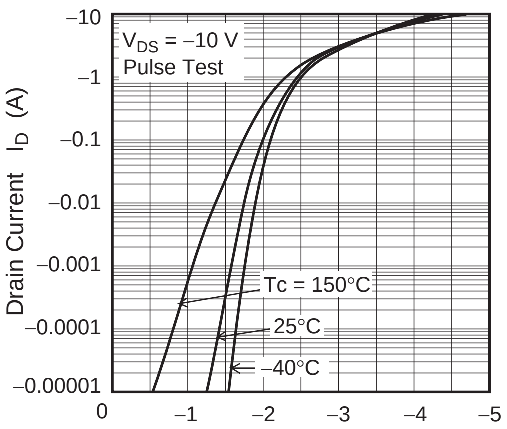


Note 6: When using the glass epoxy board (FR4 40 × 40 × 1.6 mm)

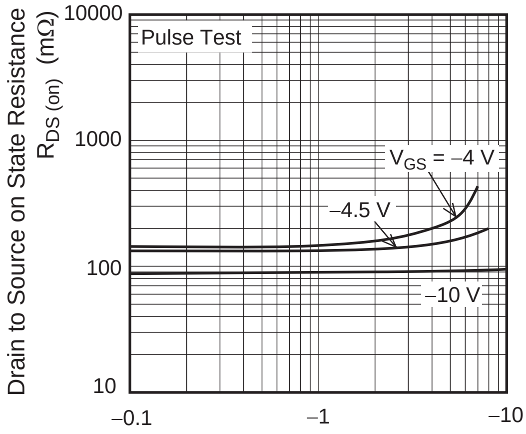
Typical Output Characteristics



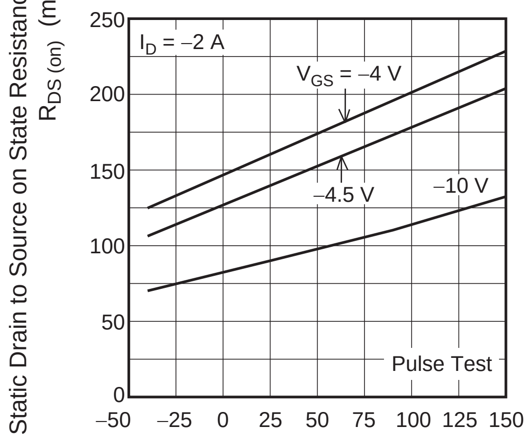
Typical Transfer Characteristics



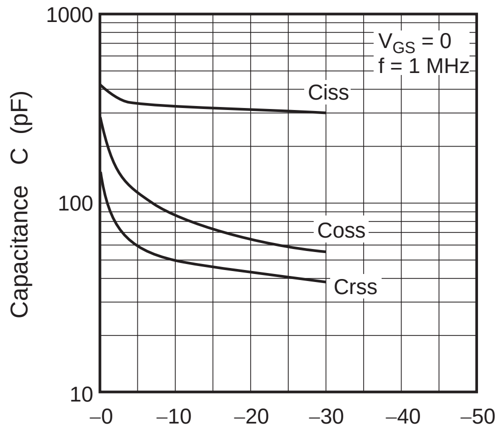
Static Drain to Source on State Resistance vs. Drain Current



Static Drain to Source on State Resistance vs. Temperature

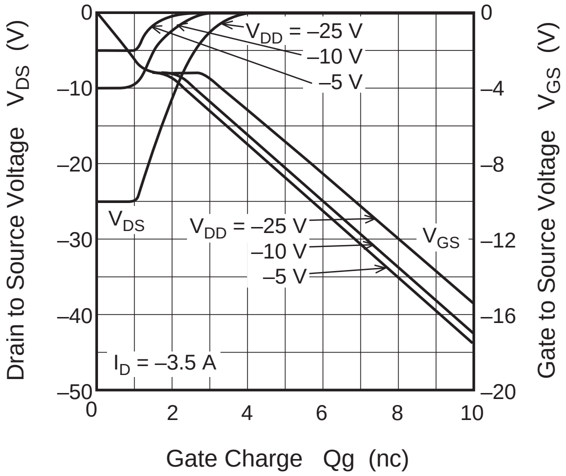


Typical Capacitance vs. Drain to Source Voltage

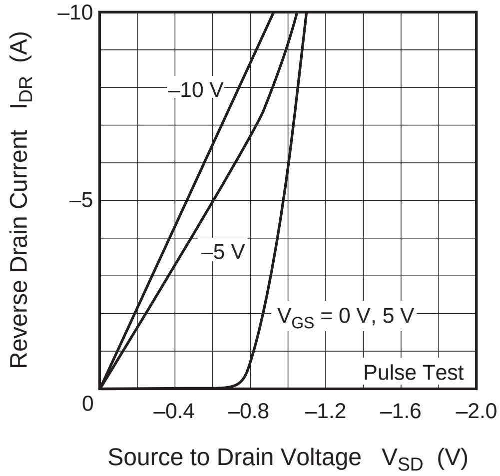


MOS3, 4 (Pch)

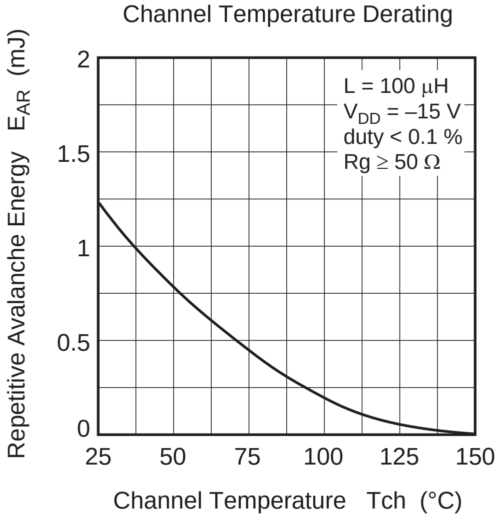
Dynamic Input Characteristics



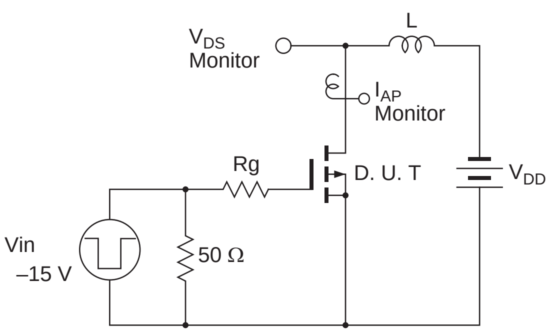
Reverse Drain Current vs. Source to Drain Voltage



Maximum Avalanche Energy vs. Channel Temperature Derating

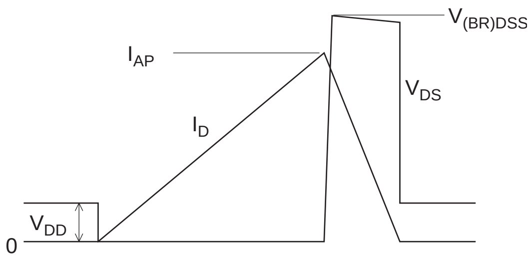


Avalanche Test Circuit



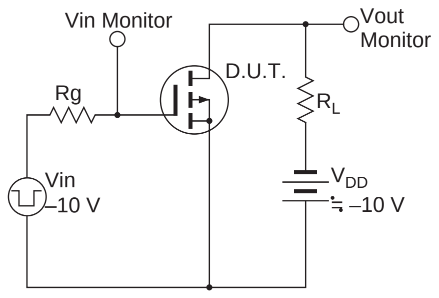
Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

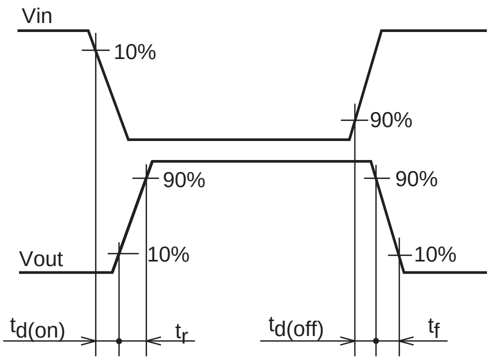


MOS3, 4 (Pch)

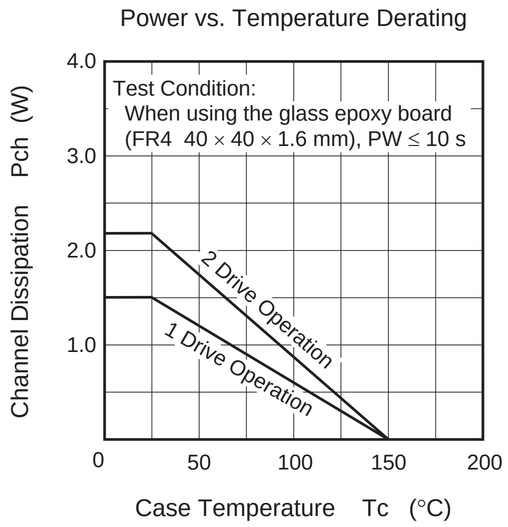
Switching Time Test Circuit

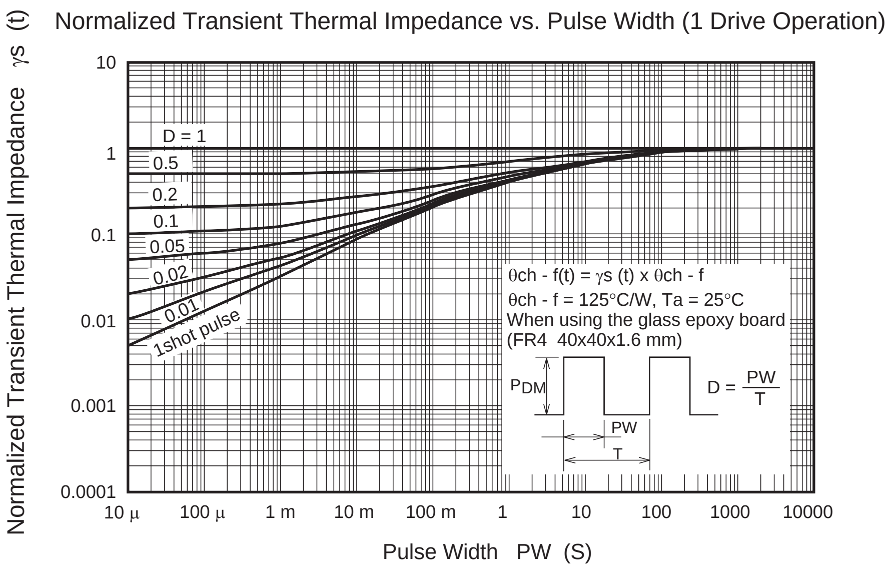


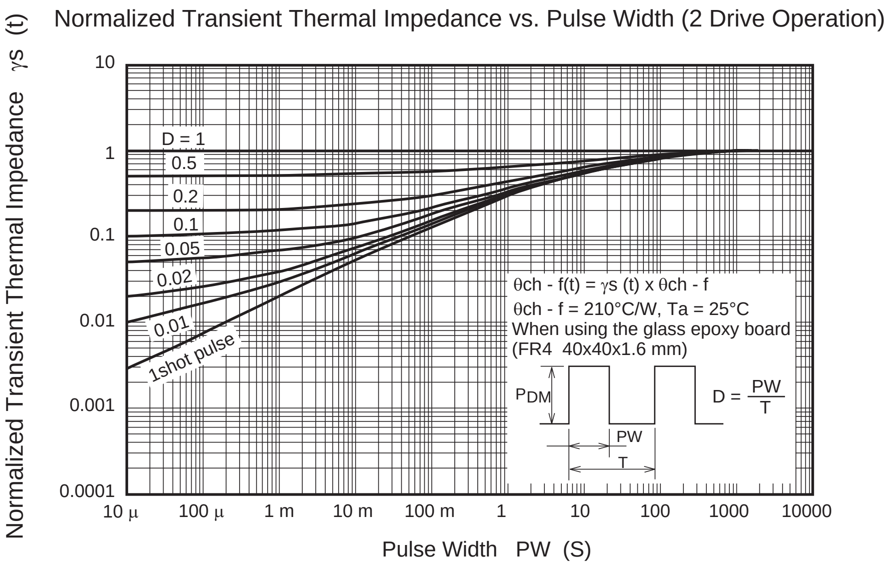
Switching Time Waveform



Common

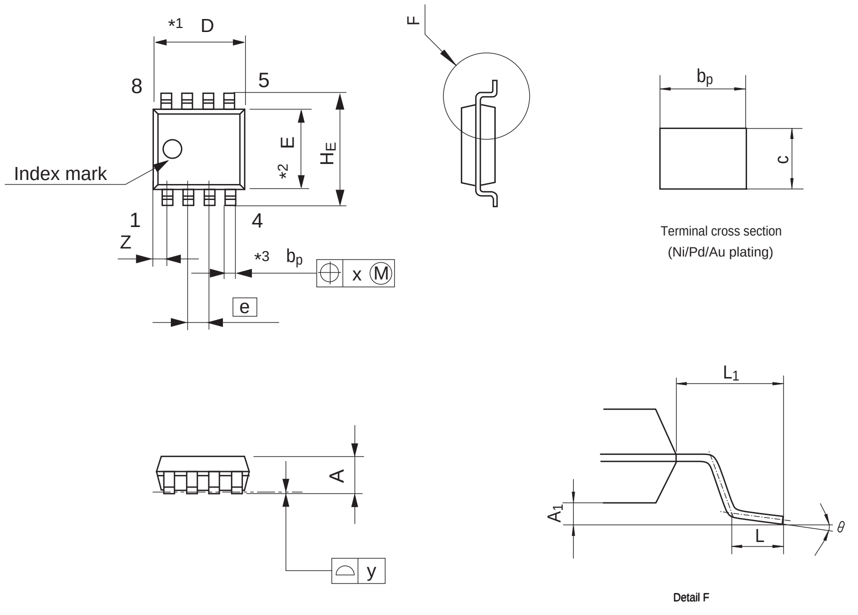

Power vs. Temperature Derating
Channel Dissipation Pch (W)
4.0
3.0
2.0
1.0
0
50
100
150
200
Case Temperature Tc (°C)
Test Condition:
When using the glass epoxy board
(FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
2 Drive Operation
1 Drive Operation


Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)
Normalized Transient Thermal Impedance γS (t)
10
1
0.1
0.01
0.001
0.0001
10 µ
100 µ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch - f(t) = γs (t) x θch - f
θch - f = 125°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40x40x1.6 mm)
PDM
D = PW / T
PW
T


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)
Normalized Transient Thermal Impedance γS (t)
10
1
0.1
0.01
0.001
0.0001
10 µ
100 µ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch - f(t) = γs (t) x θch - f
θch - f = 210°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40x40x1.6 mm)
PDM
D = PW / T
PW
T

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g



NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L_1	—	1.08	—

Ordering Information

Part No.	Quantity	Shipping Container
RJM0306JSP-00-J0	2500 pcs	Taping

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

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Colophon 1.0