CY7B160

Expandable 16,384 x 4 Static RAM

Features

- **Ultra high speed**
  - **10 ns t_{AA}**
- **Output enable ($\overline{OE}$) feature**
- **Five chip enables ($\overline{CE}_{1,2,3}$ and $CE_{4,5}$) to expand memory**
- **BiCMOS for optimum speed/power**
- **Low active power**
  - **650 mW**
- **Low standby power**
  - **200 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge.**

Functional Description

The CY7B160 is a high-performance BiCMOS static RAM organized as 16,348 x 4 bits. A memory expansion feature is provided to save access time by eliminating the need for an external decoder when stacking CY7B160s. Five chip enable inputs ($\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$, CE_4, and CE_5) make it easy to increase memory depth with up to four CY7B160s. The primary chip enable ($\overline{CE}_1$) can be used to enable or power down all four devices together while chip enables $\overline{CE}_2$, $\overline{CE}_3$, CE_4, and CE_5 can be used as extra address pins to enable or power down each device individually.

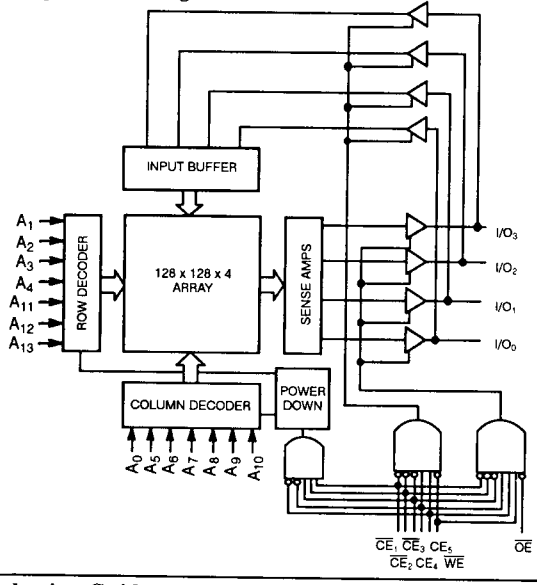
Memory expansion is facilitated by three-state drivers and an active LOW output enable ($\overline{OE}$). The device has a power-down feature, reducing the power consumption by 67% when deselected by any CE input.

Writing to the device is accomplished when $\overline{CE}_{1,2,3}$ and $\overline{WE}$ inputs are LOW while $CE_{4,5}$ inputs are HIGH. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

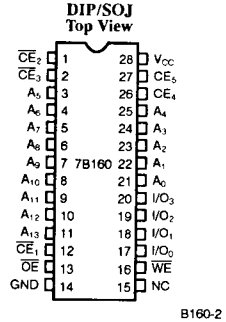
Reading the device is accomplished by taking chip enables $\overline{CE}_{1,2,3}$ LOW and $\overline{OE}$ LOW while write enable ($\overline{WE}$) and chip enables $CE_{4,5}$ remain HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

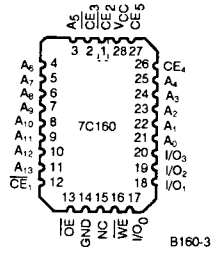
The I/O pins stay in high-impedance state when $\overline{CE}_{1,2,3}$ or $\overline{OE}$ is HIGH, or when $\overline{WE}$ or $CE_{4,5}$ are LOW.

Logic Block Diagram



Pin Configurations





Selection Guide

		7B160–10	7B160–12	7B160–15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	130	120	115
	Military		145	135
Maximum Standby Current (mA)	Commercial	40	40	40
	Military		60	50

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[1] ..... −3.0V to + 7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[2]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions			7B160-10 Min.	7B160-10 Max.	7B160-12 Min.	7B160-12 Max.	7B160-15 Min.	7B160-15 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −4.0 mA	Com'l	2.4		2.4		2.4		V
			I_{OH} = −2.0 mA	Mil							
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_O ≤ V_{CC}			−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			−10	+10	−10	+10	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA f = f max.		Com'l		130		120		115	mA
				Mil				145		135	
I_{SB}	$\overline{CE}$ Power-Down Current	($\overline{CE_1}$, or $\overline{CE_2}$, or $\overline{CE_3}$) ≥ V_{IH} or (CE_4 or CE_5) ≤ V_{IL}		Com'l		40		40		40	mA
				Mil				60		50	

Shaded area contains preliminary information.

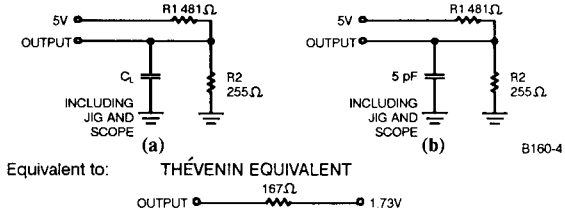
Capacitance[4]

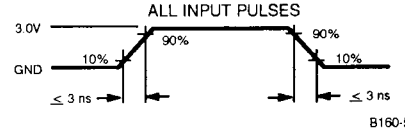
Parameters	Description	Test Conditions	Max.[5]	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

1. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except Cerdip (D22), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[2, 6]

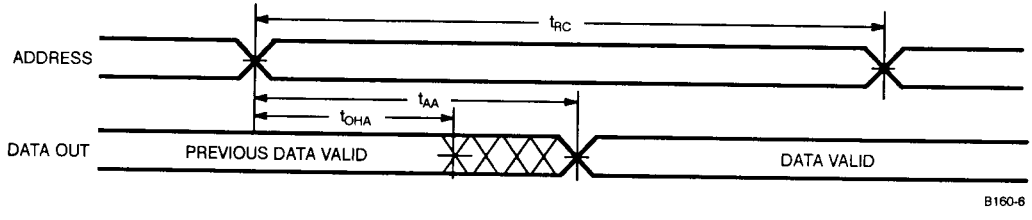
Parameters	Description	7B160-10		7B160-12		7B160-15		Units
		Max.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		5		6		7	ns
t_{LZCE}	$\overline{CE}_{1,2,3}$ LOW, $CE_{4,5}$ HIGH to Low Z[8]	2		2		3		ns
t_{HZCE}	$\overline{CE}_{1,2,3,4,5}$ HIGH to High Z[7, 8]		5		6		7	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Write End	8		8		10		ns
t_{AW}	Address Set-Up to Write End	8		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		8		10		ns
t_{SD}	Data Set-Up to Write End	5		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	2		2		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]	0	5	0	6	0	7	ns

Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and C_L = 20 pF.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
8. t_{HZCE}, t_{HZWE}, t_{HZOE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_{1,2,3}$ LOW, $CE_{4,5}$ HIGH, and $\overline{WE}$ LOW. All signals must be in this state to initiate a write and any signal can terminate a write by changing state. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O will be high-impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms

Read Cycle No. 1[10, 11]



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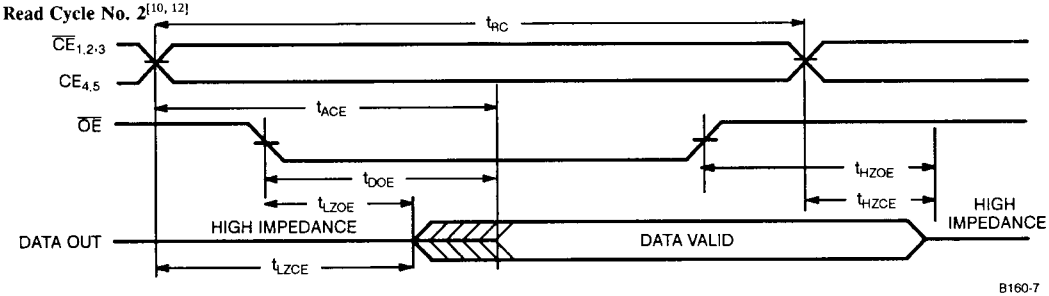
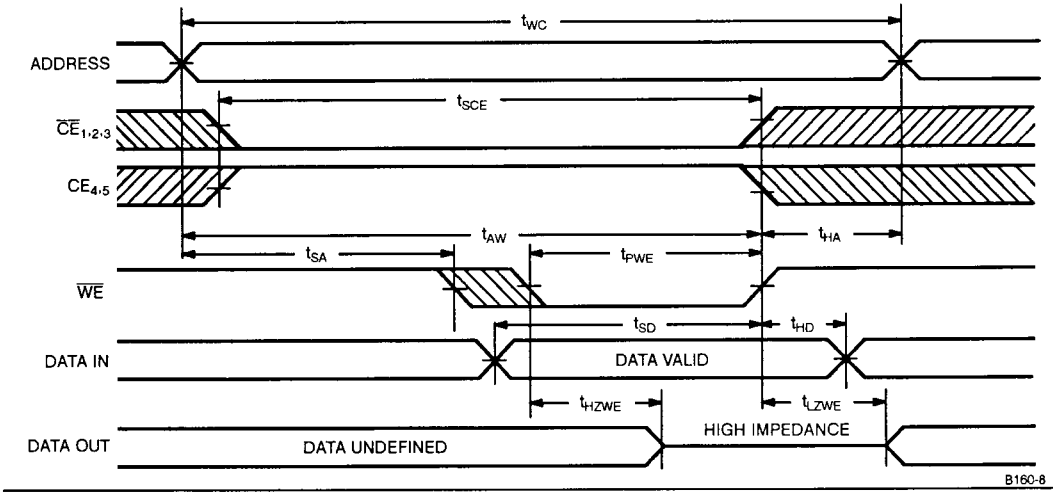
Switching Waveforms (continued)

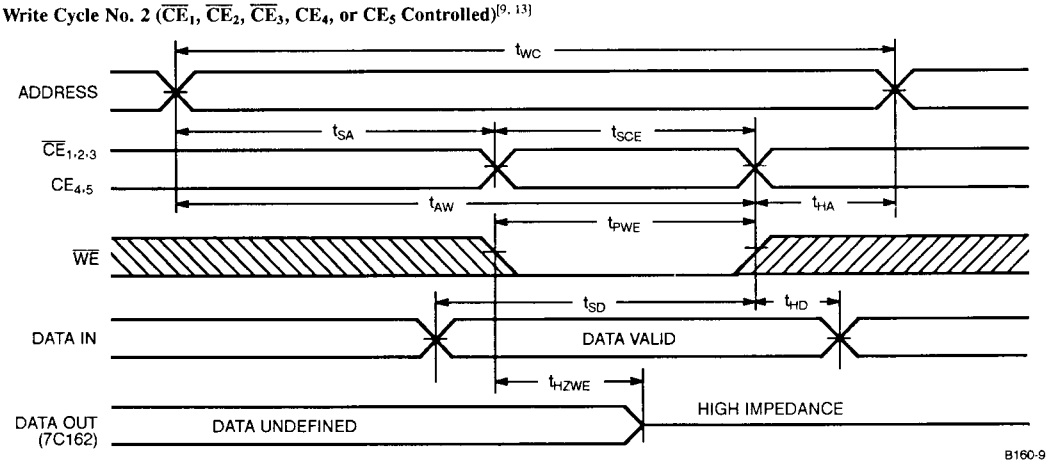
Read Cycle No. 2[10, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13]



Write Cycle No. 2 ($\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$, CE_4, or CE_5 Controlled)[9, 13]



Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$	CE_4	CE_5	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
L	L	L	H	H	H	L	Data Out	Read
L	L	L	H	H	L	X	Data In	Write
L	L	L	H	H	H	H	High Z	Deselect
H	X	X	X	X	X	X	High Z	Deselect Power-Down
X	H	X	X	X	X	X	High Z	Deselect Power-Down
X	X	H	X	X	X	X	High Z	Deselect Power-Down
X	X	X	L	X	X	X	High Z	Deselect Power-Down
X	X	X	X	L	X	X	High Z	Deselect Power-Down

2

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7B160-10VC	V21	Commercial
	CY7B160-10LC	L54	
12	CY7B160-12VC	V21	Commercial
	CY7B160-12LC	L54	
	CY7B160-12DMB	D22	Military
	CY7B160-12LMB	L54	
15	CY7B160-15VC	V21	Commercial
	CY7B160-15DMB	D22	Military
	CY7B160-15LMB	L54	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

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